

IR2171

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low IQBS allows the boot strap power supply
- High Common Mode Noise Immunity
- Input overvoltage Protection for IGBT short circuit condition
- Open Drain output

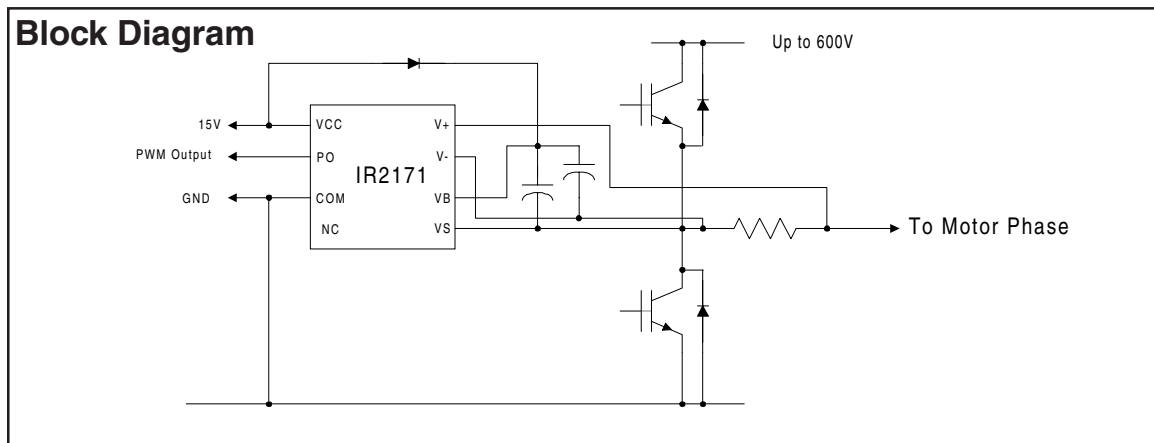
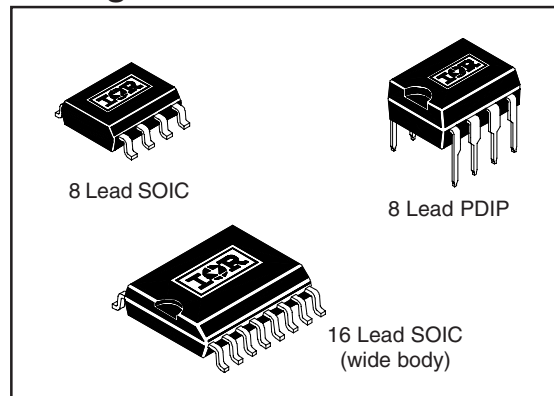
Descriptions

IR2171 is the linear current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM at 40kHz to eliminate need for the A/D input interface. It allows direct interface to uP via simple counter based measurement. The independently powered output enables easy interface to the opto coupler device for galvanic isolation if needed.

Product Summary

V_{OFFSET}	600V
I_{QBS}	1mA
V_{in}	+/-260mVmax
Gain temp. drift	20ppm/°C(typ.)
f_0	40kHz (typ.)

Packages



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	High side offset voltage	-0.3	600	V	
V _{BS}	High side floating supply voltage	V _S -0.3	25		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{IN}	Maximum input voltage between V _{IN+} and V _{IN-}	-5	5		
V _{PO}	Digital PWM output voltage	COM -0.3	V _{CC} +0.3		
V _{IN-}	V _{IN-} input voltage (note 1)	V _S -5	V _B +0.3		
dV/dt	Allowable offset voltage slew rate	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
		16 lead SOIC	—	1.25	
R _{thJA}	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
		16 lead SOIC	—	100	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Note 1: Capacitors are required between V_B and V_{in-}, and between V_B and V_S pins when bootstrap power is used. The external power supply, when used, is required between V_B and V_{in-}, and between V_B and V_S pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage	V _S +13.0	V _S +20	V
V _S	High side floating supply offset voltage	note 2	600	
V _{PO}	Digital PWM output voltage	COM	V _{CC}	
V _{CC}	Low side and logic fixed supply voltage	9.5	20	
V _{IN}	Input voltage between V _{IN+} and V _{IN-}	-260	+260	mV
T _A	Ambient temperature	-40	125	°C

Note 2: Logic operation for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}.

DC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Nominal input voltage range before saturation $ V_{IN+} - V_{IN-} $	-260	—	260	mV	$V_{IN} = 0V$ (Note 1)
V_{OS}	Input offset voltage	-10	0	10		
$\Delta V_{OS}/\Delta T_A$	Input offset voltage temperature drift	—	25	—	$\mu V/^\circ C$	
G	Gain (duty cycle % per V_{IN})	157	162	167	%/V	max gain error=5% (Note 2)
$\Delta G/\Delta T_A$	Gain temperature drift	—	20	—	ppm/ $^\circ C$	
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	—	1	2	mA	$V_S = 0V$
I_{QCC}	Quiescent V_{CC} supply current	—	—	1		
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta LIN/\Delta T_A$	Linearity temperature drift	—	.005	—	%/ $^\circ C$	
I_{O-}	Output sink current	20	—	—	mA	$V_O = 1V$
		2	—	—		$V_O = 0.1V$

Note 1: $\pm 10mV$ offset represents $\pm 1.5\%$ duty cycle fluctuation

Note 2: Gain = (full range of duty cycle in %) / (full input voltage range).

AC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
fo	Carrier frequency output	—	40	—	kHz	figure 1
$\Delta f/\Delta T_A$	Temperature drift of carrier frequency	—	500	—	ppm/ $^\circ C$	$V_{IN} = 0V$ & $5V$
Dmin	Minimum duty	—	7	—	%	$V_{IN+} = -260mV, V_{IN-} = 0$
Dmax	Maximum duty	—	93	—	%	$V_{IN+} = +260mV, V_{IN-} = 0$
BW	fo bandwidth		15		kHz	$V_{IN+} = 100mV$ pk-pk sine wave, -3dB
PHS	Phase shift at 1kHz		-10		$^\circ$	$V_{IN+} = 100mV$ pk-pk sine wave

Timing Waveforms

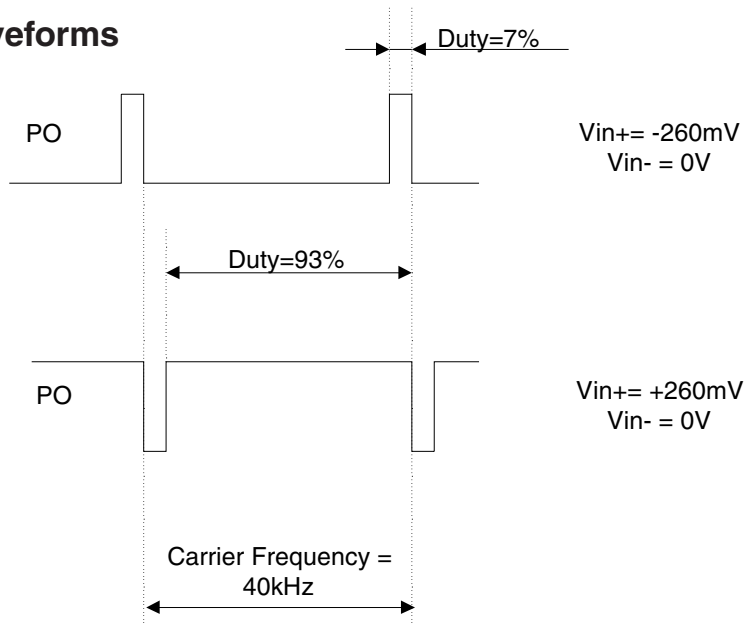


Figure 1 Output waveform

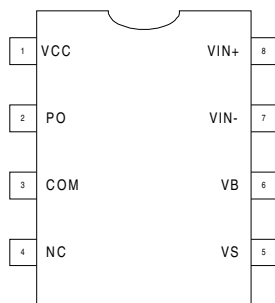
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at a same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM periods gives consistent measurement of the current feedback over the temperature drift.

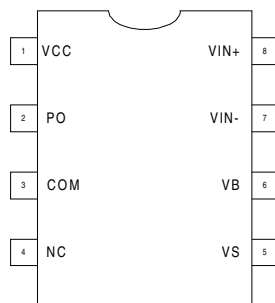
Lead Definitions

Symbol	Description
VCC	Low side and logic supply voltage
COM	Low side logic ground
VIN+	Positive sense input
VIN-	Negative sense input
VB	High side supply
VS	High side return
PO	Digital PWM output
N.C.	No connection

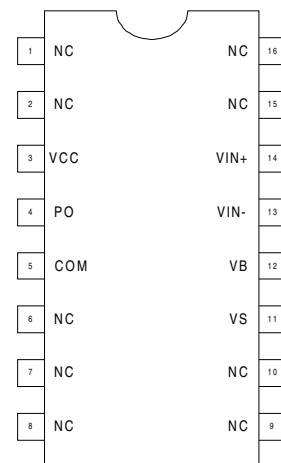
Lead Assignment



8 lead SOIC
IR2171S

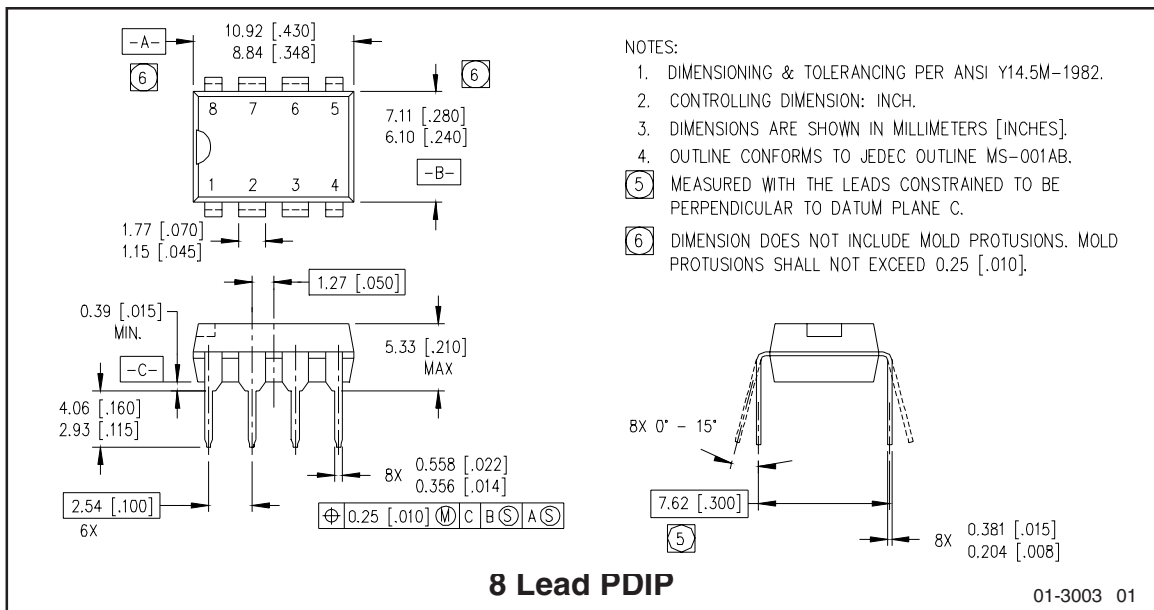
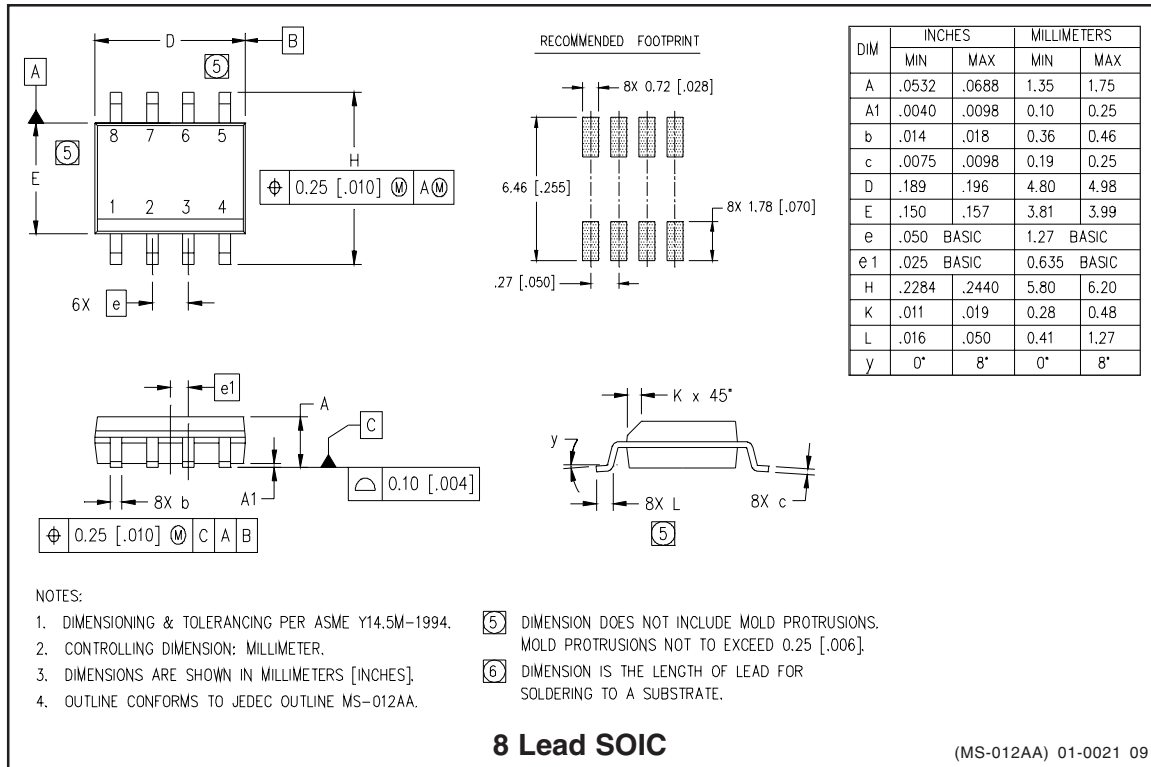


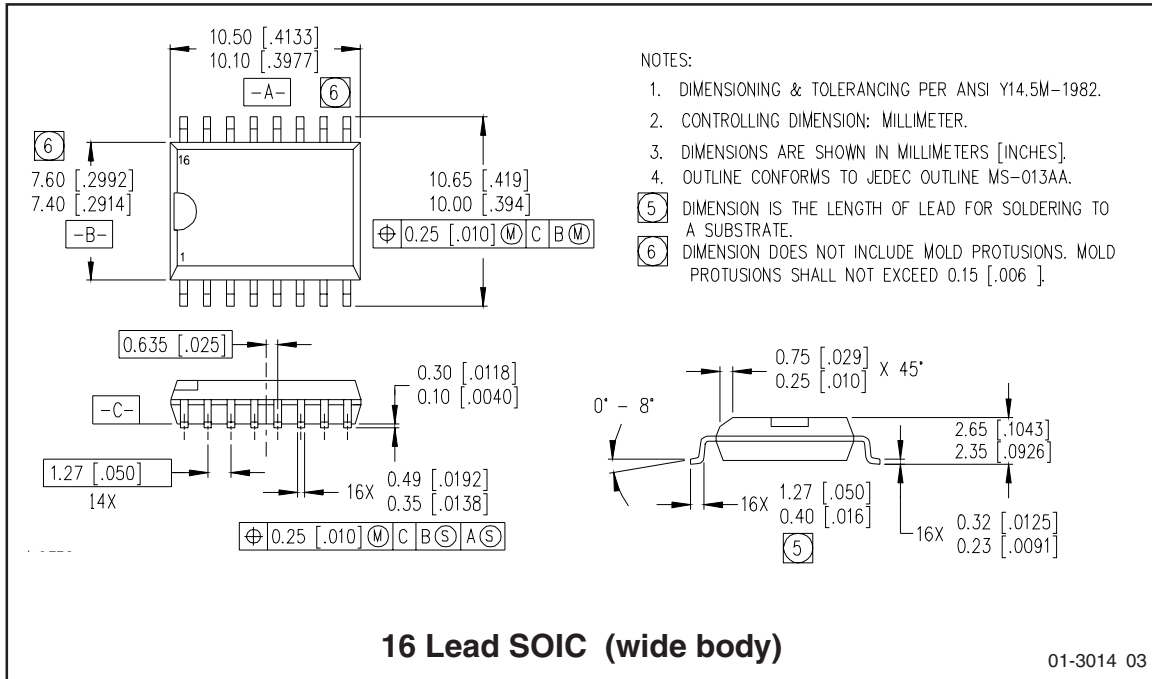
8 lead PDIP
IR2171



16 lead SOIC
IR21716S

Case Outline





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Data and specifications subject to change without notice. 6/29/2000

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