

Features

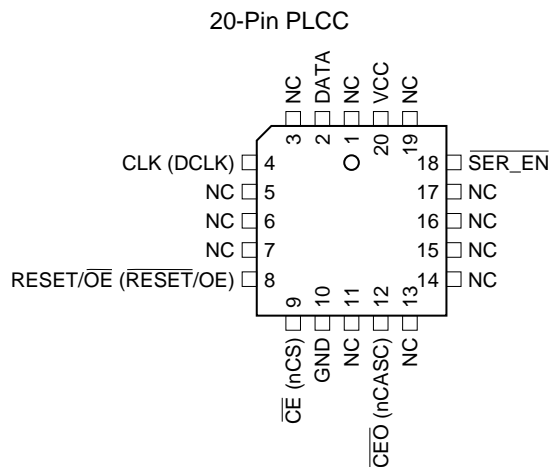
- EE Programmable 65,536 x 1, 131,072 x 1 and 262,144 x 1 bit Serial Memories Designed to Store Configuration Programs for Programmable Gate Arrays
- Simple Interface to SRAM FPGAs Requires Only One User I/O Pin
- Able to Configure with EPF6000 and EPF8000, Flex 10K FPGAs
- Cascadable To Support Additional Configurations or Future Higher-Density Arrays (17C128/256 only)
- Low-Power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in Industry-Standard Pin-Compatible PLCC Package
- In-System Programmable via 2-Wire Bus
- Emulation of 24CXX Serial EEPROMs
- Available in 3.3V and 5V Versions

Description

The AT17C65/128/256A and AT17LV65/128/256A (AT17A Series) FPGA Configuration EEPROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17A Series is packaged in the popular 20-pin PLCC. The AT17A Series family uses a simple serial-access provides to configure one or more FPGA devices. The AT17A Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17A Series, the user can select the polarity of the reset function by programming a special EEPROM bit.

The AT17A Series is pin compatible with the industry standard configurator, and can be programmed with industry standard programmers.

Pin Configurations



FPGA Configuration EEPROM

65K, 128K and 256K

AT17CxxxA
AT17LVxxxA

Rev. 0996A-07/98



Controlling The AT17A Series Serial EEPROMs

Most connections between the FPGA device and the serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17A Series drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17A Series.
- The \overline{CEO} output of any AT17C/LV128/256A drives the CE input of the next AT17C/LV65/128/256 in a cascade chain of PROMs.
- $\overline{SER_EN}$ must be connected to V_{CC} .

There are, however, two different ways to use the inputs \overline{CE} and \overline{OE} , as shown in the AC Characteristics waveforms.

Condition 1

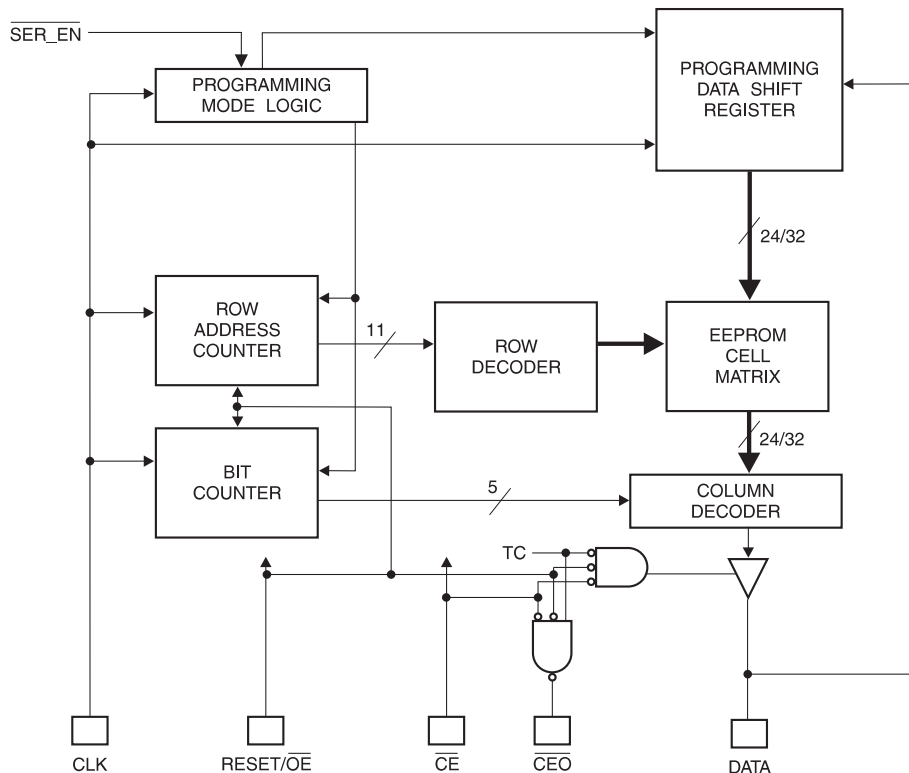
The simplest connection is to have the FPGA D/ \overline{P} output drive both \overline{CE} and RESET/ \overline{OE} in parallel (Figure 1). Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configura-

tion cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17A Series does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/ \overline{P} output drives only the \overline{CE} input of the AT17A Series, while its \overline{OE} input is driven by the inversion of the input to the FPGA RESET input pin. This connection works under all normal circumstances, even when the user aborts a configuration before D/ \overline{P} has gone high. A high level on the RESET/ \overline{OE} input to the AT17C/LVxxxA – during FPGA reset – clears the Configurator's internal address pointer, so that the reconfiguration starts at the beginning. The AT17A Series does not require an inverter since the RESET polarity is programmable.

Block Diagram



Pin Configurations

| PLCC/S OIC | DIP | | | |
|---------------|-----|------------------------|-----|--|
| Pin | Pin | Name | I/O | Description |
| 2 | 1 | DATA | I/O | Three-state DATA output for reading. Input/Output pin for programming. |
| 4 | 2 | CLK | I | Clock input. Used to increment the internal address and bit counter for reading and programming. |
| 8 | 3 | RESET/ \overline{OE} | | RESET/Output Enable input (when $\overline{SER_EN}$ is High). A low level on both the \overline{CE} and RESET/ \overline{OE} inputs enables the data output driver. A high level on RESET/ \overline{OE} resets both the address and bit counters. A logic polarity of this input is programmable as either RESET/ \overline{OE} or \overline{RESET}/OE . This document describes the pin as RESET/ \overline{OE} . |
| 9 | 4 | \overline{CE} | I | Chip Enable input. Used for device selection. A low level on both \overline{CE} and \overline{OE} enables the data output driver. A high level on \overline{CE} disables both the address and bit counters and forces the device into a low-power mode. Note this pin will not enable/disable the device in 2-wire serial mode (ie; when $\overline{SER_EN}$ is low). |
| 10 | 5 | GND | | Ground pin |
| 12 | 6 | CEO | O | Chip Enable Out output. This signal is asserted low on the clock cycle following the last bit read from the memory. It will stay low as long as CE and \overline{OE} are both low. It will then follow \overline{CE} until \overline{OE} goes high. Thereafter, CEO will stay high until the entire PROM is read again and senses the status of RESET polarity. |
| | | A2 | I | Device selection input, A2. This is used to enable (or select) the device during programming and when $\overline{SER_EN}$ is low (see Programming Guide for more details). |
| 18 | 7 | $\overline{SER_EN}$ | I | Serial enable is normally high during FPGA loading operations. Bringing $\overline{SER_EN}$ low, enables the 2-wire serial interface for programming. |
| 20 | 8 | V _{CC} | | +3.3V/+5V power supply pin. |

Absolute Maximum Ratings*

| | |
|--|---------------------------------|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -0.1V to V _{CC} + 0.5V |
| Supply Voltage (V _{CC}) | -0.5 V to + 7.0V |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.) | 260°C |
| ESD (R _{ZAP} = 1.5K, C _{ZAP} = 100 pF) | 2000V |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FPGA Master Serial Mode Summary

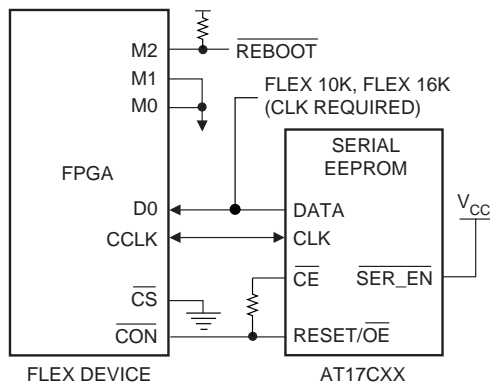
The I/O and logic functions of the FPGA and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

Cascading Serial Configuration EEPROMs (AT17C/LV256A)

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory (17C/LV128/256A only).

After the last bit from the first Configurator is read, the next clock signal to the Configurator asserts its \overline{CE} output Low and disables its DATA line. The second Configurator recognizes the low level on its \overline{CE} input and enables its DATA output.

Figure 1. Condition 1 Connection



After configuration is complete, the address counters of all cascaded Configurators are reset if the reset signal drives the $\overline{RESET}/\overline{OE}$ on each Configurator Active.

If the address counters are not to be reset upon completion, then the $\overline{RESET}/\overline{OE}$ inputs can be tied to ground. For more details, please reference the AT17C Series Programming Guide

Programming Mode

The programming mode is entered by bringing $\overline{SER_EN}$ low. In this mode the chip can be programmed by the 2-wire interface. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information. The AT17C Series parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.0V nominal.

AT17C/LVxxx Reset Polarity

The AT17C/LVxxxA lets the user choose the reset polarity as either $\overline{RESET}/\overline{OE}$ or \overline{RESET}/OE .

Standby Mode

The AT17C/LVxxxA enters a low-power standby mode whenever \overline{CE} is asserted high. In this mode, the Configurator consumes less than 1.0 mA of current. The output remains in a high-impedance state regardless of the state of the \overline{OE} input.

Operating Conditions

| Symbol | Description | | AT17Cxxx | AT17LVxxx | Units |
|----------|-------------|---|-----------|-----------|-------|
| | | | Min/Max | Min/Max | |
| V_{CC} | Commercial | Supply voltage relative to GND -0°C to +70°C | 4.75/5.25 | 3.0/3.6 | V |
| | Industrial | Supply voltage relative to GND -40°C to +85°C | 4.5/5.5 | 3.0/3.6 | V |
| | Military | Supply voltage relative to GND -55°C to +125°C | 4.5/5.5 | 3.0/3.6 | V |

DC Characteristics

$V_{CC} = 5V \pm 5\%$ Commercial / $5V \pm 10\%$ Ind./Mil.

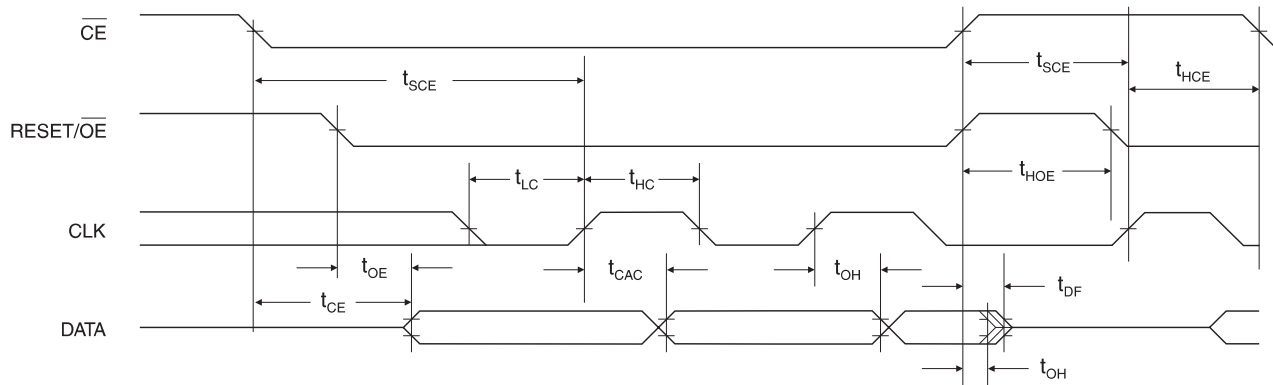
| Symbol | Description | | Min | Max | Units |
|-----------|---|---------------------|-----|----------|---------|
| V_{IH} | High-level input voltage | | 2.0 | V_{CC} | V |
| V_{IL} | Low-level input voltage | | 0 | 0.8 | V |
| V_{OH} | High-level output voltage ($I_{OH} = -4$ mA) | Commercial | 3.7 | | V |
| V_{OL} | Low-level output voltage ($I_{OL} = +4$ mA) | | | | |
| V_{OH} | High-level output voltage ($I_{OH} = -4$ mA) | Industrial | 3.6 | | V |
| V_{OL} | Low-level output voltage ($I_{OL} = +4$ mA) | | | | |
| V_{OH} | High-level output voltage ($I_{OH} = -4$ mA) | Military | 3.5 | | V |
| V_{OL} | Low-level output voltage ($I_{OL} = +4$ mA) | | | | |
| I_{CCA} | Supply current, active mode | | | 10 | mA |
| I_L | Input or output leakage current ($V_{IN} = V_{CC}$ or GND) | | -10 | 10 | μ A |
| I_{CCS} | Supply current, standby mode AT17C256 | Commercial | | 75 | μ A |
| | | Industrial/Military | | 150 | μ A |
| | Supply current, standby mode AT17C128/65 | Commercial | | 1 | mA |
| | | Industrial/Military | | 2 | mA |

DC Characteristics

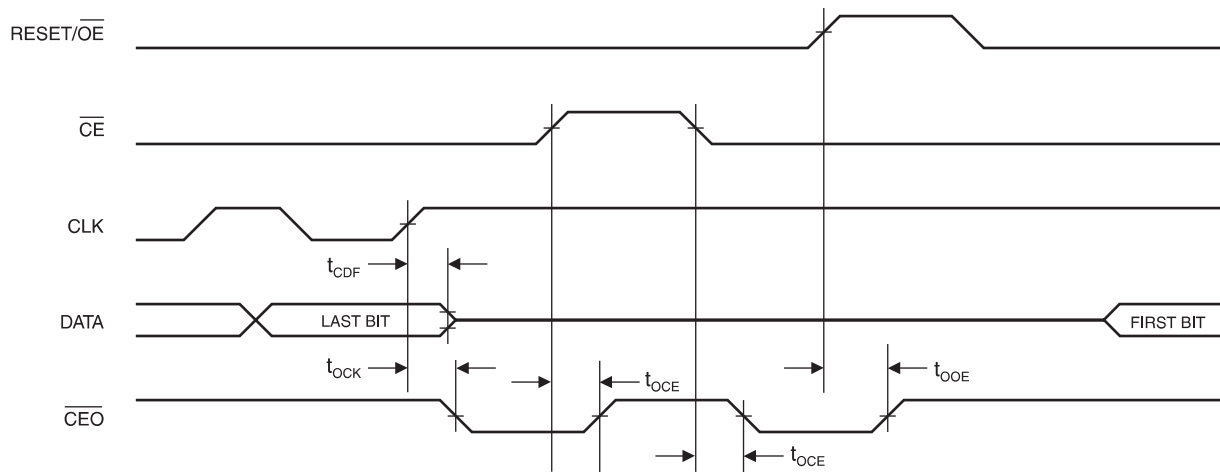
$V_{CC} = 3.3V \pm 10\%$

| Symbol | Description | | Min | Max | Units |
|-----------|---|---------------------|-----|----------|---------|
| V_{IH} | High-level input voltage | | 2.0 | V_{CC} | V |
| V_{IL} | Low-level input voltage | | 0 | 0.8 | V |
| V_{OH} | High-level output voltage ($I_{OH} = -2.5$ mA) | Commercial | 2.4 | | V |
| V_{OL} | Low-level output voltage ($I_{OL} = +3$ mA) | | | | |
| V_{OH} | High-level output voltage ($I_{OH} = -2$ mA) | Industrial | 2.4 | | V |
| V_{OL} | Low-level output voltage ($I_{OL} = +3$ mA) | | | | |
| V_{OH} | High-level output voltage ($I_{OH} = -2$ mA) | Military | 2.4 | | V |
| V_{OL} | Low-level output voltage ($I_{OL} = +2.5$ mA) | | | | |
| I_{CCA} | Supply current, active mode | | | 5 | mA |
| I_L | Input or output leakage current ($V_{IN} = V_{CC}$ or GND) | | -10 | 10 | μ A |
| I_{CCS} | Supply current, standby mode | Commercial | | 50 | μ A |
| | | Industrial/Military | | 100 | μ A |

AC Characteristics



AC Characteristics When Cascading



AC Characteristics for AT17C256A

$V_{CC} = 5V \pm 5\%$ Commercial / $V_{CC} = 5V \pm 10\%$ Ind./Mil

| Symbol | Description | Commercial | | Industrial/Military | | Units |
|-----------------|--|------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $t_{OE}^{(2)}$ | \overline{OE} to Data Delay | | 25 | | 25 | ns |
| $t_{CE}^{(2)}$ | \overline{CE} to Data Delay | | 45 | | 45 | ns |
| $t_{CAC}^{(2)}$ | CLK to Data Delay | | 50 | | 55 | ns |
| $t_{OH}^{(2)}$ | Data Hold From \overline{CE} , \overline{OE} , or CLK | 0 | | 0 | | ns |
| $t_{DF}^{(3)}$ | \overline{CE} or \overline{OE} to Data Float Delay | | 50 | | 50 | ns |
| t_{LC} | CLK Low Time | 20 | | 20 | | ns |
| t_{HC} | CLK High Time | 20 | | 20 | | ns |
| t_{SCE} | \overline{CE} Setup Time to CLK (to guarantee proper counting) | 35 | | 40 | | ns |
| t_{HCE} | \overline{CE} Hold Time to CLK (to guarantee proper counting) | 0 | | 0 | | ns |
| t_{HOE} | \overline{OE} High Time (guarantees counter is reset) | 20 | | 20 | | ns |
| F_{MAX} | MAX Input Clock Frequency | 12.5 | | 12.5 | | MHz |

AC Characteristics for AT17C256A When Cascading

$V_{CC} = 5V \pm 5\%$ Commercial / $V_{CC} = 5V \pm 10\%$ Ind./Mil

| Symbol | Description | Commercial | | Industrial/Military | | Units |
|-----------------|--|------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $t_{CDF}^{(3)}$ | CLK to Data Float Delay | | 50 | | 50 | ns |
| $t_{OCK}^{(2)}$ | CLK to \overline{CEO} Delay | | 35 | | 40 | ns |
| $t_{OCE}^{(2)}$ | CE to \overline{CEO} Delay | | 35 | | 35 | ns |
| $t_{OOE}^{(2)}$ | RESET/ \overline{OE} to \overline{CEO} Delay | | 30 | | 35 | ns |

- Notes:
1. Preliminary specifications for military operating range only.
 2. AC test load = 50 pF.
 3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics for AT17C65/128A

$V_{CC} = 5V \pm 5\%$ Commercial / $V_{CC} = 5V \pm 10\%$ Ind./Mil.

| Symbol | Description | Commercial | | Industrial/Military | | Units |
|-----------------|--|------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $t_{OE}^{(2)}$ | \overline{OE} to Data Delay | | 110 | | 150 | ns |
| $t_{CE}^{(2)}$ | \overline{CE} to Data Delay | | 50 | | 50 | ns |
| $t_{CAC}^{(2)}$ | CLK to Data Delay | | 50 | | 55 | ns |
| $t_{OH}^{(2)}$ | Data Hold From \overline{CE} , \overline{OE} , or CLK | 0 | | 0 | | ns |
| $t_{DF}^{(3)}$ | \overline{CE} or \overline{OE} to Data Float Delay | | 50 | | 50 | ns |
| t_{LC} | CLK Low Time | 30 | | 35 | | ns |
| t_{HC} | CLK High Time | 30 | | 35 | | ns |
| t_{SCE} | \overline{CE} Setup Time to CLK (to guarantee proper counting) | 45 | | 50 | | ns |
| t_{HCE} | \overline{CE} Hold Time to CLK (to guarantee proper counting) | 0 | | 5 | | ns |
| t_{HOE} | \overline{OE} High Time (guarantees counter is reset) | 50 | | 60 | | ns |
| $F_{MAX}^{(4)}$ | MAX Input Clock Frequency | | 10 | | 10 | MHz |

AC Characteristics for AT17C128/256A When Cascading

$V_{CC} = 5V \pm 5\%$ Commercial / $V_{CC} = 5V \pm 10\%$ Ind./Mil.

| Symbol | Description | Commercial | | Industrial/Military | | Units |
|-----------------|--|------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $t_{CDF}^{(3)}$ | CLK to Data Float Delay | | 50 | | 50 | ns |
| $t_{OCK}^{(2)}$ | CLK to \overline{CEO} Delay | | 65 | | 75 | ns |
| $t_{OCE}^{(2)}$ | CE to \overline{CEO} Delay | | 55 | | 60 | ns |
| $t_{OE}^{(2)}$ | RESET/ \overline{OE} to \overline{CEO} Delay | | 55 | | 55 | ns |

- Notes:
1. Preliminary specifications for military operating range only.
 2. AC test load = 50 pF.
 3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.
 4. During cascade $F_{MAX} = 8$ MHz.

AC Characteristics

$V_{CC} = 3.3V \pm 10\%$

| Symbol | Description | Commercial | | Industrial/Military | | Units |
|-----------------|--|------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $t_{OE}^{(2)}$ | \overline{OE} to Data Delay | | 40 | | 45 | ns |
| $t_{CE}^{(2)}$ | \overline{CE} to Data Delay | | 60 | | 60 | ns |
| $t_{CAC}^{(2)}$ | CLK to Data Delay | | 75 | | 80 | ns |
| $t_{OH}^{(2)}$ | Data Hold From \overline{CE} , \overline{OE} , or CLK | 0 | | 0 | | ns |
| $t_{DF}^{(3)}$ | \overline{CE} or \overline{OE} to Data Float Delay | | 55 | | 55 | ns |
| t_{LC} | CLK Low Time | 25 | | 25 | | ns |
| t_{HC} | CLK High Time | 25 | | 25 | | ns |
| t_{SCE} | \overline{CE} Setup Time to CLK (to guarantee proper counting) | 35 | | 60 | | ns |
| t_{HCE} | \overline{CE} Hold Time to CLK (to guarantee proper counting) | 0 | | 0 | | ns |
| t_{HOE} | \overline{OE} High Time (guarantees counter is reset) | 25 | | 25 | | ns |
| $F_{MAX}^{(4)}$ | MAX Input Clock Frequency | | 10 | 8 | 10 | MHz |

- Notes:
1. Preliminary specifications for military operating range only.
 2. AC test lead = 50 pf.
 3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.
 4. During cascade $F_{MAX} = 8$ MHz.

AC Characteristics When Cascading

$V_{CC} = 3.3V \pm 10\%$

| Symbol | Description | Commercial | | Industrial/Military | | Units |
|-----------------|--|------------|-----|---------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $t_{CDF}^{(3)}$ | CLK to Data Float Delay | | 60 | | 60 | ns |
| $t_{OCK}^{(2)}$ | CLK to \overline{CEO} Delay | | 55 | | 60 | ns |
| $t_{OCE}^{(2)}$ | CE to \overline{CEO} Delay | | 55 | | 60 | ns |
| $t_{OOE}^{(2)}$ | RESET/ \overline{OE} to \overline{CEO} Delay | | 40 | | 45 | ns |

Ordering Information - 5V Devices

| Memory Size (K) | Ordering Code | Package | Operation Range |
|-----------------|----------------|---------|-------------------------------|
| 64K | AT17C65A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17C65A-10JI | 20J | Industrial (-40°C to 85°C) |
| 128K | AT17C128A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17C128A-10JI | 20J | Industrial (-40°C to 85°C) |
| 256K | AT17C256A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17C256A-10JI | 20J | Industrial (-40°C to 85°C) |

Ordering Information - 3.3V Devices

| Memory Size (K) | Ordering Code | Package | Operation Range |
|-----------------|-----------------|---------|-------------------------------|
| 64K | AT17LV65A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17LV65A-10JI | 20J | Industrial (-40°C to 85°C) |
| 128K | AT17LV128A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17LV128A-10JI | 20J | Industrial (-40°C to 85°C) |
| 256K | AT17LV256A-10JC | 20J | Commercial (0°C to 70°C) |
| | AT17LV256A-10JI | 20J | Industrial (-40°C to 85°C) |

| Package Type | |
|--------------|---|
| 20J | 20-Lead, Plastic J-Leaded Chip Carrier (PLCC) |

Packaging Information

20J, 20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-018 AA

