64 k SRAM (8-kword \times 8-bit)

HITACHI

ADE-203-454B (Z) Rev. 2.0 Nov. 1997

Description

The Hitachi HM6264B is 64k-bit static RAM organized 8-kword \times 8-bit. It realizes higher performance and low power consumption by 1.5 μ m CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, 300 mil plastic DIP, is available for high density mounting.

Features

- High speed Fast access time: 85/100 ns (max)
- Low power Standby: 10 μW (typ)
 Operation: 15 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory No clock or timing strobe required
- Equal access and cycle times
- Common data input and output Three state output
- Directly TTL compatible All inputs and outputs
- Battery backup operation capability

Ordering Information

| Type No. | Access time | Package |
|-----------------------------------|-----------------|--------------------------------------|
| HM6264BLP-8L HM6264BLP-10L | 85 ns 100 ns | 600-mil, 28-pin plastic DIP (DP-28) |
| HM6264BLSP-8L HM6264BLSP-10L | 85 ns 100 ns | 300-mil, 28-pin plastic DIP(DP-28N) |
| HM6264BLFP-8LT HM6264BLFP-10LT | 85 ns 100 ns | 450-mil, 28-pin plastic SOP(FP-28DA) |

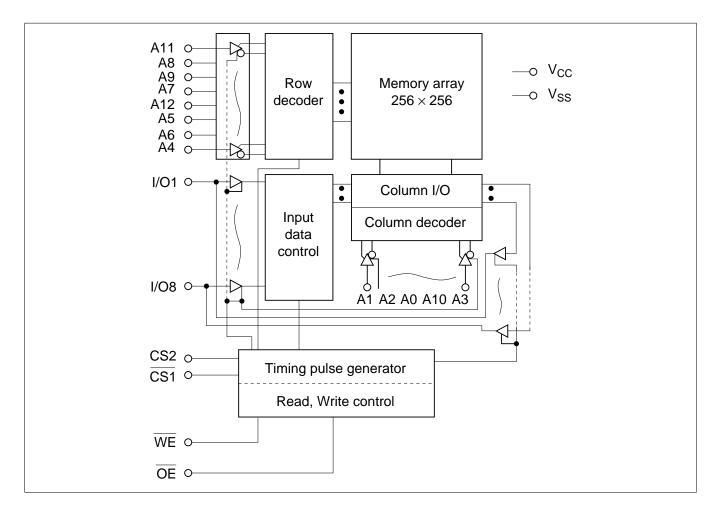
Pin Arrangement

| HM62 | 64BLP/BLSP | /BLFP Series | | | | | | |
|-----------------|------------|------------------------------------|--|--|--|--|--|--|
| NC | | 28 □ V _{CC} | | | | | | |
| A12 | <u>2</u> | 27 🟳 WE | | | | | | |
| A7 | □ 3 | 26 🗆 CS2 | | | | | | |
| A6 | □ 4 | 25 🗆 A8 | | | | | | |
| A5 | □ 5 | ²⁴ 🗋 A9 | | | | | | |
| A4 | □ 6 | 23 🗋 A11 | | | | | | |
| A3 | □ 7 | 22 🗇 OE | | | | | | |
| A2 | □ 8 | 21 🗇 A10 | | | | | | |
| A1 | □ 9 | $20 \square \overline{\text{CS1}}$ | | | | | | |
| A0 | □ 10 | 19 🗆 I/O8 | | | | | | |
| I/O1 | □ 11 | 18 🗆 I/07 | | | | | | |
| I/O2 | □ 12 | 17 🗇 I/O6 | | | | | | |
| 1/03 | □ 13 | 16 🗆 I/O5 | | | | | | |
| V _{SS} | □ 14 | 15 🗆 I/O4 | | | | | | |
| | (Top view) | | | | | | | |

Pin Description

| Pin name | name Function Pin name | | Function |
|--------------|------------------------|-----------------|---------------|
| A0 to A12 | Address input | WE | Write enable |
| I/O1 to I/O8 | Data input/output | ŌĒ | Output enable |
| CS1 | Chip select 1 | NC | No connection |
| CS2 | Chip select 2 | V _{cc} | Power supply |
| | | V _{ss} | Ground |

Block Diagram



Function Table

| WE | CS1 | CS2 | OE | Mode | V _{cc} current | I/O pin | Ref. cycle |
|----|-----|-----|----|---------------------------|------------------------------------|---------|--------------------|
| × | Н | × | × | Not selected (power down) | I_{SB}, I_{SB1} | High-Z | _ |
| × | × | L | × | Not selected (power down) | I _{SB} , I _{SB1} | High-Z | _ |
| Н | L | Н | Н | Output disable | I _{cc} | High-Z | _ |
| Н | L | Н | L | Read | I _{cc} | Dout | Read cycle (1)–(3) |
| L | L | Н | Н | Write | I _{cc} | Din | Write cycle (1) |
| L | L | Н | L | Write | I _{cc} | Din | Write cycle (2) |

Note: ×: H or L

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|------------------------------------|-----------------|--|------|
| Power supply voltage ^{*1} | V _{cc} | -0.5 to +7.0 | V |
| Terminal voltage ^{*1} | V _T | -0.5^{2} to V _{cc} + 0.3 ³ | V |
| Power dissipation | P _T | 1.0 | W |
| Operating temperature | Topr | 0 to + 70 | °C |
| Storage temperature | Tstg | -55 to +125 | °C |
| Storage temperature under bias | Tbias | -10 to +85 | °C |

Notes: 1. Relative to V_{ss}

2. V_{τ} min: -3.0 V for pulse half-width \leq 50 ns

3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions (Ta = 0 to $+70^{\circ}$ C)

| Symbol | Min | Тур | Max | Unit |
|-----------------|---|---|-----------------------------------|--|
| V _{cc} | 4.5 | 5.0 | 5.5 | V |
| V _{ss} | 0 | 0 | 0 | V |
| V _{IH} | 2.2 | _ | V _{cc} + 0.3 | V |
| V _{IL} | -0.3 ^{*1} | _ | 0.8 | V |
| | V _{cc} V _{ss} V _{IH} | $ \frac{V_{CC}}{V_{SS}} \qquad 4.5 $ $ \frac{V_{IH}}{2.2} $ | $ \frac{V_{cc}}{V_{ss}} = 0 $ | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ |

Note: 1. V_{IL} min: -3.0 V for pulse half-width \leq 50 ns

| Parameter | Symbol | Min | Typ⁺¹ | Max | Unit | Test conditions |
|--|-------------------|-----|-------|-----|------|---|
| Input leakage current | _L | | | 2 | μΑ | Vin = V_{ss} to V_{cc} |
| Output leakage current | I _{LO} | | | 2 | μA | $\overline{\frac{CS1}{WE}} = V_{H} \text{ or } CS2 = V_{IL} \text{ or } \overline{OE} = V_{H} \text{ or}$ $\overline{WE} = V_{IL}, V_{I/O} = V_{SS} \text{ to } V_{CC}$ |
| Operating power supply current | I _{CCDC} | — | 7 | 15 | mA | $\overline{CS1} = V_{IL}, CS2 = V_{IH}, I_{I/O} = 0 \text{ mA}$ others = V_{IH}/V_{IL} |
| Average operating power supply current | I _{CC1} | | 30 | 45 | mA | $\label{eq:minimum} \begin{array}{l} \underset{CS1}{\text{Min cycle, duty} = 100\%,} \\ \hline CS1 = V_{\text{IL}}, \ CS2 = V_{\text{IH}}, \ I_{\text{I/O}} = 0 \ \text{mA} \\ \text{others} = V_{\text{IH}}/V_{\text{IL}} \end{array}$ |
| | I _{CC2} | | 3 | 5 | mA | $\label{eq:constraint} \begin{array}{l} \hline Cycle \ time = 1 \ \mu s, \ duty = 100\%, \ I_{_{I\!/O}} = 0 \ mA \\ \hline CS1 \le 0.2 \ V, \ CS2 \ge V_{_{CC}} - 0.2 \ V, \\ V_{_{I\!H}} \ge V_{_{CC}} - 0.2 \ V, \ V_{_{I\!L}} \le 0.2 \ V \end{array}$ |
| Standby power supply current | I _{SB} | _ | 1 | 3 | mA | $\overline{\text{CS1}} = \text{V}_{\text{IH}}, \text{CS2} = \text{V}_{\text{IL}}$ |
| | I _{SB1} | — | 2 | 50 | μA | $\label{eq:constraint} \begin{array}{c} \overline{CS1} \geq V_{\text{CC}} - 0.2 \text{ V}, \ CS2 \geq V_{\text{CC}} - 0.2 \text{ V} \text{ or} \\ 0 \text{ V} \leq CS2 \leq 0.2 \text{ V}, \ 0 \text{ V} \leq \text{Vin} \end{array}$ |
| Output low voltage | V _{oL} | _ | | 0.4 | V | I _{oL} = 2.1 mA |
| Output high voltage | V _{OH} | 2.4 | | | V | I _{OH} = -1.0 mA |

DC Characteristics (Ta = 0 to +70°C, $V_{CC} = 5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$)

Notes: 1. Typical values are at V_{cc} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = 25° C, f = 1.0 MHz)

| Parameter | Symbol | Min | Тур | Max | Unit | Test conditions |
|---------------------------------|------------------|-----|-----|-----|------|------------------------|
| Input capacitance ^{*1} | Cin | _ | _ | 5 | рF | Vin = 0 V |
| Input/output capacitance*1 | C _{I/O} | | | 7 | pF | V _{I/O} = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, $V_{CC} = 5 \text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

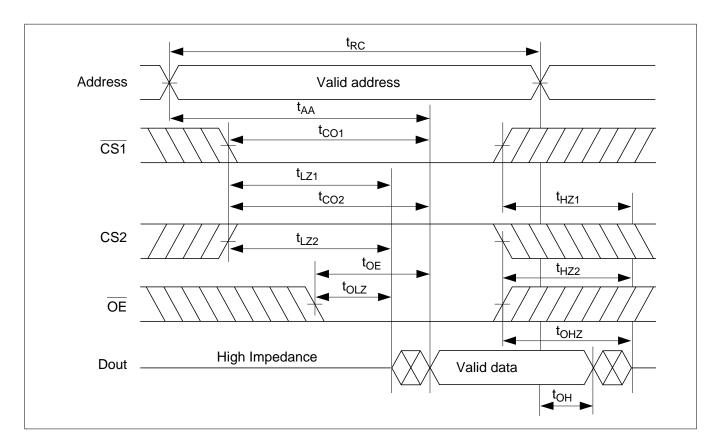
- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

| | | | HM62 | 64B-8L | HM626 | 64B-10L | | |
|---|-----|------------------|------|--------|-------|---------|------|-------|
| Parameter | | Symbol | Min | Max | Min | Max | Unit | Notes |
| Read cycle time | | t _{RC} | 85 | _ | 100 | — | ns | |
| Address access time | | t _{AA} | _ | 85 | _ | 100 | ns | |
| Chip select access time | CS1 | t _{co1} | | 85 | | 100 | ns | |
| | CS2 | t _{co2} | | 85 | | 100 | ns | |
| Output enable to output valid | | t _{oe} | | 45 | | 50 | ns | |
| Chip selection to output in low-Z | CS1 | t _{LZ1} | 10 | | 10 | | ns | 2 |
| | CS2 | t _{LZ2} | 10 | | 10 | _ | ns | 2 |
| Output enable to output in low-Z | | t _{oLZ} | 5 | | 5 | _ | ns | 2 |
| Chip deselection in to output in high-Z | CS1 | t _{HZ1} | 0 | 30 | 0 | 35 | ns | 1, 2 |
| | CS2 | t _{HZ2} | 0 | 30 | 0 | 35 | ns | 1, 2 |
| Output disable to output in high-Z | | t _{oHz} | 0 | 30 | 0 | 35 | ns | 1, 2 |
| Output hold from address change | | t _{oH} | 10 | _ | 10 | | ns | |

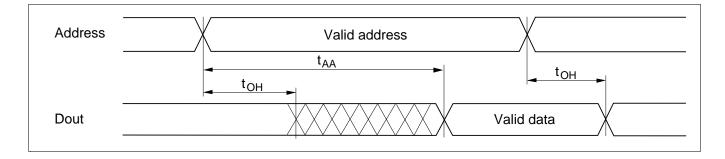
Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

 At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

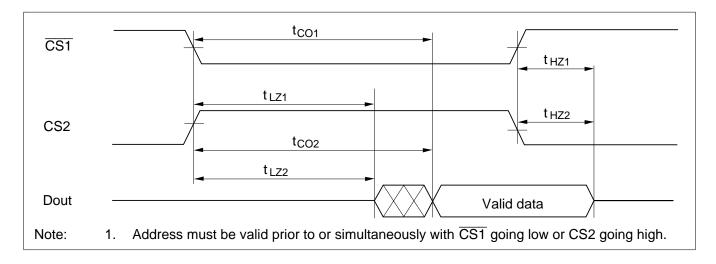


Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

Read Timing Waveform (2) $(\overline{WE} = V_{IH}, \overline{OE} = V_{IL})$



Read Timing Waveform (3) $(\overline{WE} = V_{IH}, \overline{OE} = V_{IL})^{*1}$



Write Cycle

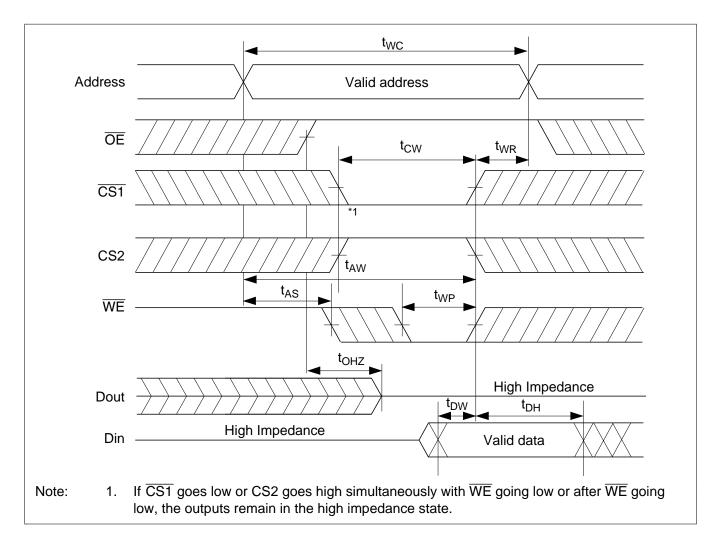
| | | HM62 | 64B-8L | HM62 | 64B-10L | | |
|------------------------------------|------------------|------|--------|------|---------|------|-------|
| Parameter | Symbol | Min | Max | Min | Max | Unit | Notes |
| Write cycle time | t _{wc} | 85 | _ | 100 | | ns | |
| Chip selection to end of write | t _{cw} | 75 | _ | 80 | | ns | 2 |
| Address setup time | t _{AS} | 0 | _ | 0 | | ns | 3 |
| Address valid to end of write | t _{AW} | 75 | | 80 | | ns | |
| Write pulse width | t _{wP} | 55 | | 60 | | ns | 1, 6 |
| Write recovery time | t _{wR} | 0 | | 0 | | ns | 4 |
| WE to output in high-Z | t _{wHZ} | 0 | 30 | 0 | 35 | ns | 5 |
| Data to write time overlap | t _{DW} | 40 | | 40 | | ns | |
| Data hold from write time | t _{DH} | 0 | | 0 | _ | ns | |
| Output active from end of write | t _{ow} | 5 | _ | 5 | | ns | |
| Output disable to output in high-Z | t _{oHZ} | 0 | 30 | 0 | 35 | ns | 5 |

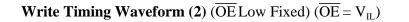
Notes: 1. A write occurs during the overlap of a low $\overline{CS1}$, and high CS2, and a high \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low,CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high CS2 going low and \overline{WE} going high. Time t_{WP} is measured from the beginning of write to the end of write.

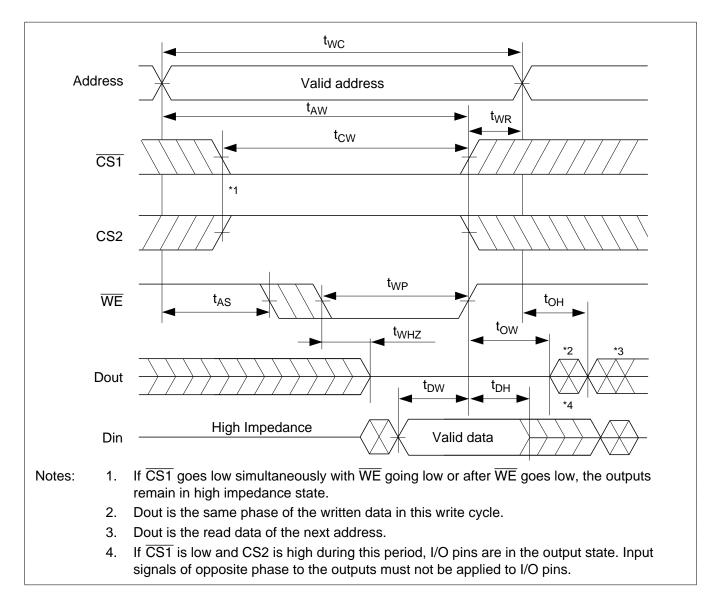
- 2. t_{cw} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
- 3. t_{AS} is measured from the address valid to the beginning of write.
- 4. t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.
- 5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
- 6. In the write cycle with \overline{OE} low fixed, t_{wP} must satisfy the following equation to avoid a problem of data bus contention

 $t_{WP} \ge t_{WHZ} \max + t_{DW} \min$.

Write Timing Waveform (1) $(\overline{\text{OE}} \operatorname{Clock})$







| Parameter | Symbol | Min | Typ⁺¹ | Max | Unit | Test conditions ^⁴ |
|--------------------------------------|-------------------|--------------------|------------------------|------------------|------|--|
| V_{cc} for data retention | V_{DR} | 2.0 | _ | _ | V | $\label{eq:constraint} \begin{array}{l} \overline{\text{CS1}} \geq \text{V}_{\text{CC}} \ -0.2 \ \text{V}, \\ \text{CS2} \geq \text{V}_{\text{CC}} \ -0.2 \ \text{V} \ \text{or} \ \text{CS2} \leq 0.2 \ \text{V} \end{array}$ |
| Data retention current | I _{CCDR} | | 1 ^{*1} | 25 ^{*2} | μΑ | $\label{eq:Vcc} \begin{array}{l} V_{cc} = 3.0 \ \text{V}, 0 \ \text{V} \leq \text{Vin} \leq \text{V}_{cc} \\ \hline CS1 \geq \text{V}_{cc} \ -0.2 \ \text{V}, \ CS2 \geq \text{V}_{cc} \ -0.2 \ \text{V} \\ \text{or} \ 0 \ \text{V} \leq CS2 \leq 0.2 \ \text{V} \end{array}$ |
| Chip deselect to data retention time | t _{CDR} | 0 | | | ns | See retention waveform |
| Operation recovery time | t _R | t _{RC} *3 | | _ | ns | _ |

| Low Y | V _{CC} Data | Retention | Characteristics | (Ta = | $0 \text{ to } +70^{\circ}\text{C})$ |
|-------|----------------------|-----------|-----------------|-------|--------------------------------------|
|-------|----------------------|-----------|-----------------|-------|--------------------------------------|

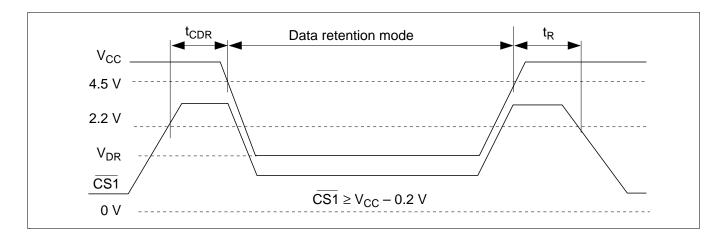
Notes: 1. Reference data at Ta = 25° C.

2. 10 μ A max at Ta = 0 to + 40°C.

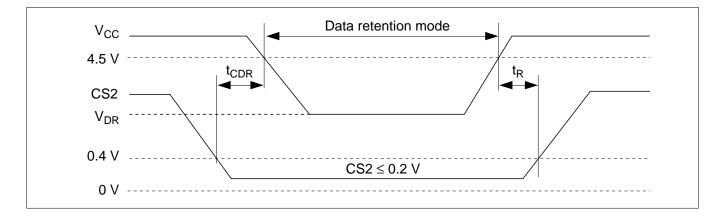
3. t_{RC} = read cycle time.

4. CS2 controls address buffer, WE buffer, CS1 buffer, OE buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE, OE, CS1, I/O) can be in the high impedance state. If CS1 controls data retention mode, CS2 must be CS2 ≥ V_{cc} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, WE, OE, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



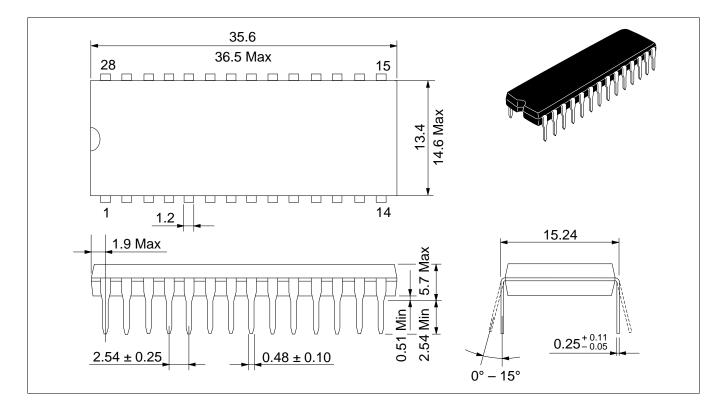
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

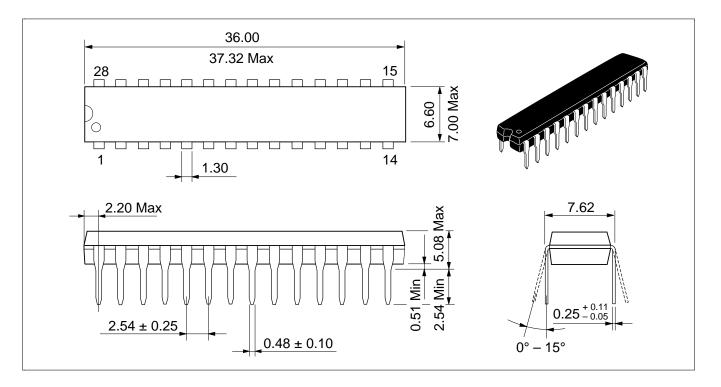
HM6264BLP Series (DP-28)

Unit: mm



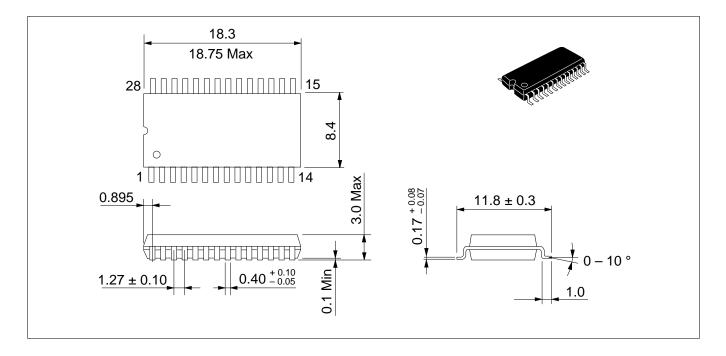
HM6264BLSP Series (DP-28N)

Unit: mm



HM6264BLTM Series (FP-28DA)

Unit: mm



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