Description

The NEC μPD416 is a 16,384-word by 1-bit dynamic MOS Random-access Memory. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer, N-channel, silicon-gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

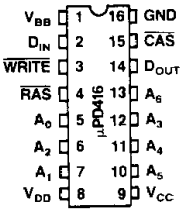
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16-pin dual-in-line package. The 16-pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

Features

- ☐ 16,384-word x 1-bit organization
- ☐ High memory density: 16-pin ceramic or plastic packages
- ☐ Multiplexed address inputs
- ☐ Standard power supplies: +12V, −5V, +5V
- ☐ Low power dissipation: 462mw active (max), 20mw standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle
- ☐ Read-modify-write, $\overline{RAS}$-only refresh, and page mode capability
- ☐ All inputs TTL-compatible and low capacitance
- ☐ 128 refresh cycles
- ☐ 3 performance ranges:

Device	Access Time	R/W Cycle	RMW Cycle
μPD416-2	200ns	375ns	375ns
μPD416-3	150ns	320ns	320ns
μPD416-5	120ns	320ns	320ns

Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	V_{BB}	−5V power supply
2	D_{IN}	Data-in
3	$\overline{WRITE}$	Read/write
4	$\overline{RAS}$	Row address strobe
5–7, 10–13	A_0–A_6	Address inputs
8	V_{DD}	+12V power supply
9	V_{CC}	+5V power supply
14	D_{OUT}	Data-out
15	$\overline{CAS}$	Column address strobe
16	GND	Ground

Absolute Maximum Ratings*

Operating Temperature, T_{OPR}	0°C to +70°C
Storage Temperature, T_{STG}	−55°C to +150°C
All Output Voltages, V_O ①	−0.5V to +20V
All Input Voltages, V_I ①	−0.5V to +20V
Supply Voltages V_{DD}, V_{CC}, GND ①	−0.5V to +20V
Supply Voltages V_{DD}, V_{CC} ②	−1.0V to +15V
Short-circuit Output Current	50mA
Power Dissipation, P_D	1w

Notes: ① Relative to V_{BB}.
② Relative to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0°C to +70°C; V_{DD} = +12V ± 10%; V_{BB} = −5V ± 10%; V_{CC} = +5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

Operational Description

Addressing

The 14 address bits required to decode 1 of 16,384-bit locations are multiplexed on to the 7 address pins and then latched on the chip with the use of the row address strobe ($\overline{RAS}$), and the column address strobe ($\overline{CAS}$). The 7-bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7-bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} max after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} max. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

Data I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early-write" cycle and data-out will remain in the high impedance state throughout the cycle. For a read, write, or read-modify-write cycle, the data output will contain the data in the selected cell after the access time. Data-out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

Page Mode

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column address with $\overline{CAS}$. This eliminates the set-up and hold times for the row address resulting in faster operation.

Refresh

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128-row addresses every 2 milliseconds or less. Because data-out is not latched, $\overline{RAS}$-only cycles can be used for a simple refresh operation.

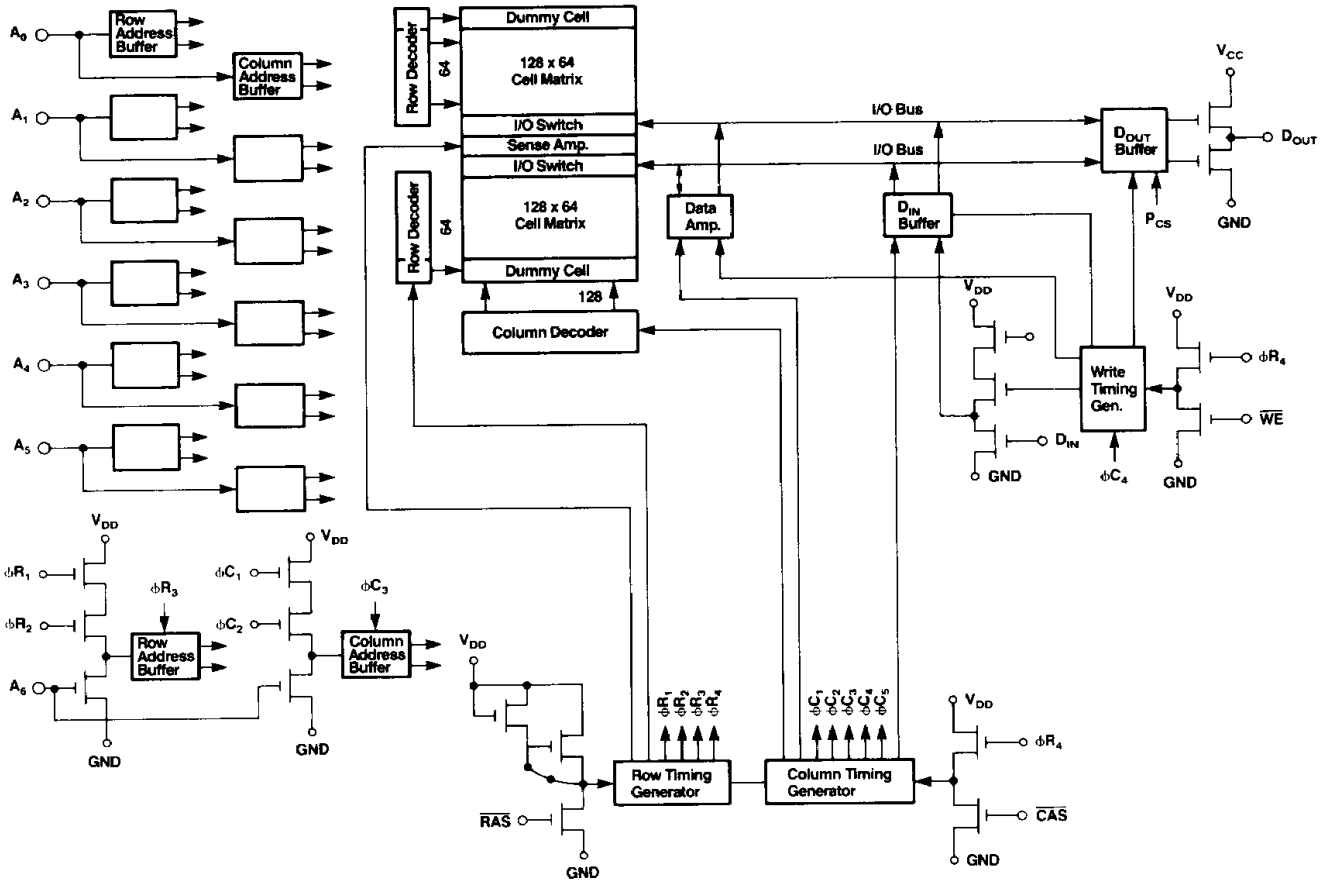
Chip Selection

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip-select function. Unselected chip outputs will remain in the high impedance state.

Power Sequencing

In order to assure long-term reliability, V_{BB} should be applied first during power-up and removed last during power-down.

Block Diagram



AC Characteristics

T_A = 0°C to +70°C; V_{DD} = +12V ± 10%; V_{CC} = +5V ± 10%; V_{BB} = −5V ± 10%; GND = 0V

Parameter	Symbol	Limits μPD416-2 Min	Limits μPD416-2 Max	Limits μPD416-3 Min	Limits μPD416-3 Max	Limits μPD416-5 Min	Limits μPD416-5 Max	Unit	Test Conditions
Random Read or Write Cycle Time	t_{RC}	375		320		320		ns	②
Read-Write Cycle Time	t_{RWC}	375		375		320		ns	②
Page Mode Cycle Time	t_{PC}	225		170		160		ns	
Access Time from $\overline{RAS}$	t_{RAC}		200		150		120	ns	③ ④
Access Time from $\overline{CAS}$	t_{CAC}		135		100		80	ns	④ ⑤
Output Buffer Turn-off Delay	t_{OFF}	0	50	0	40	0	35	ns	⑥
Transition Times (rise and fall)	t_T	3	50	3	35	3	35	ns	⑦
$\overline{RAS}$ Precharge Time	t_{RP}	120		100		100		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	135		100		80		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20		−20		0		ns	
Row Address Set-up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	25		20		15		ns	
Column Address Set-up Time	t_{ASC}	−10		−10		−10		ns	
Column Address Hold Time	t_{CAH}	55		45		40		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120		95		80		ns	
Read Command Set-up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		ns	
Write Command Hold Time	t_{WCH}	55		45		40		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120		95		80		ns	
Write Command Pulse Width	t_{WP}	55		45		40		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	70		50		50		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	70		50		50		ns	
Data-in Set-up Time	t_{DS}	0		0		0		ns	⑨
Data-in Hold Time	t_{DH}	55		45		40		ns	⑨
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120		95		80		ns	
CAS Precharge Time (for page mode cycle only)	t_{CP}	80		60		60		ns	
Refresh Period	t_{REF}		2		2		2	ms	
Write Command Set-up Time	t_{WCS}	−20		−20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	160		120		120		ns	⑩

Notes: ① AC measurements assume t_T = 5ns.
② The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
③ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
④ Measured with a load equivalent to 2 TTL loads and 100pF.
⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).
⑥ t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
⑦ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RDC} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
⑨ These parameters are referenced to CAS leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data-out pin will remain open circuit (high impedance); if $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data-out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data-out (at access time) is indeterminate.

DC Characteristics

T_A = 0°C to +70°C; ① V_{DD} = +12V ± 10%; V_{CC} = +5V ± 10%; V_{BB} = −5V ± 10%; GND = 0V

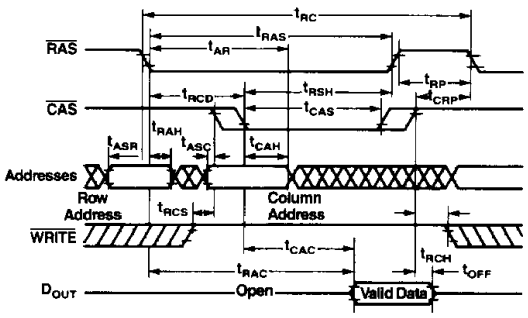
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage	GND	0	0	0	V	②
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	②
Input High Voltage (Logic 1), $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	②
Input High Voltage (Logic 1), (all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	V_{IH}	2.4		7.0	V	②
Input Low Voltage (Logic 0), (all inputs)	V_{IL}	−1.0		0.8	V	②
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$, cycling; t_{RC} = t_{RC} min ④
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}; D_{OUT} = high impedance
Refresh V_{DD} Current (μPD416-5)	I_{DD3}			27	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IHC}; t_{RC} = 375ns ④
Refresh V_{DD} Current (all speeds except μPD416-5)	I_{DD3}			25	mA	
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = 225ns ④
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375ns ⑤
Standby V_{CC} Current	I_{CC2}	−10		10	μA	$\overline{RAS}$ = V_{IHC}; D_{OUT} = high impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IHC}; t_{RC} = 375ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = 225ns ⑤
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}; D_{OUT} = high impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IHC}; t_{RC} = 375ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = 225ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V; 0V ≤ V_{IN} ≤ +7V; all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = −5mA ③
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2mA

Notes: ① T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, provided AC operating parameters are met. See Figure 1 for derating curve.
② All voltages referenced to GND
③ Output voltage will swing from GND to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to GND without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.
⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high-level data V_{CC} is connected through a low impedance (135Ω typ) to data-out. At all other times I_{CC} consists of leakage currents only.

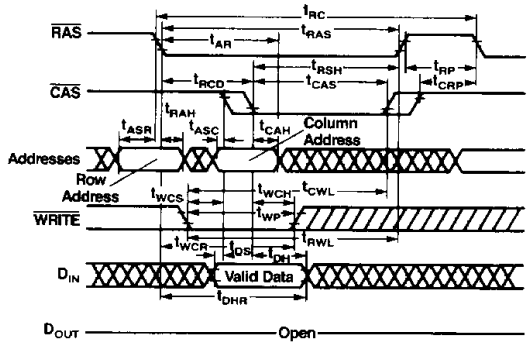
3

Timing Waveforms

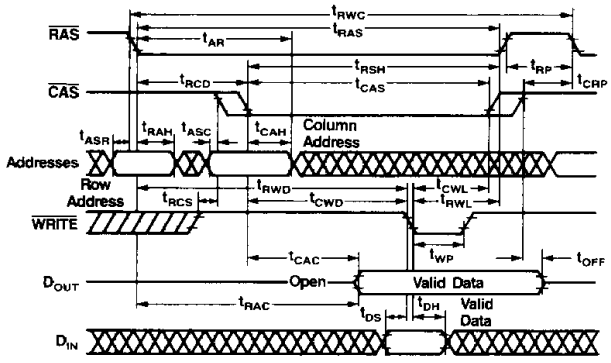
Read Cycle



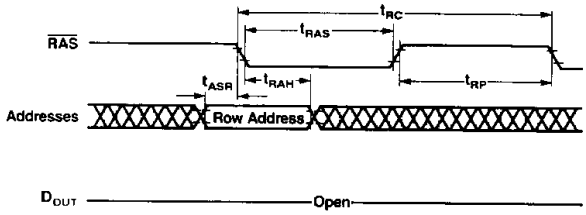
Write Cycle



Read-Write/Read-Modify-Write Cycle

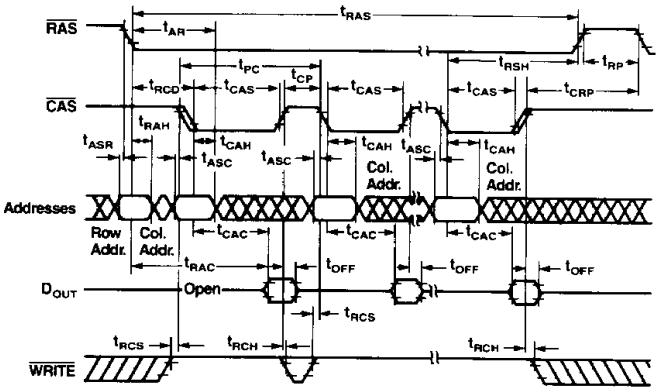


RAS-only Refresh Cycle

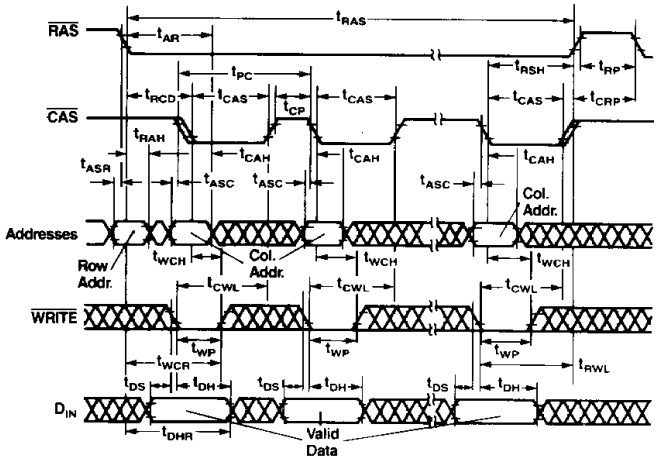


Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't care.

Page Mode Read Cycle



Page Mode Write Cycle



Derating Curves

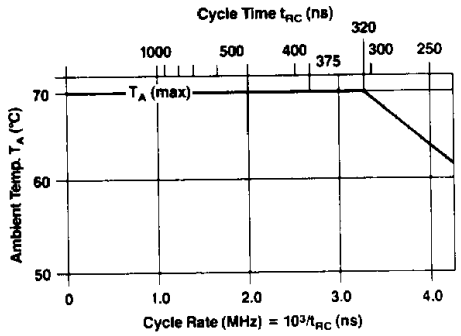


Figure 1. Maximum Ambient Temperature versus Cycle Rate for Extended Frequency Operation

Note: T_A (max) for operation at cycling rates greater than 2.66MHz (t_{CYC} < 375ns) is determined by T_A (max) [°C] = 70 − 9.0 x (cycle rate [MHz] − 2.66). For μPD416-5, it is T_A (max) [°C] = 70 − 9.0 x (cycle rate [MHz] − 3.125).

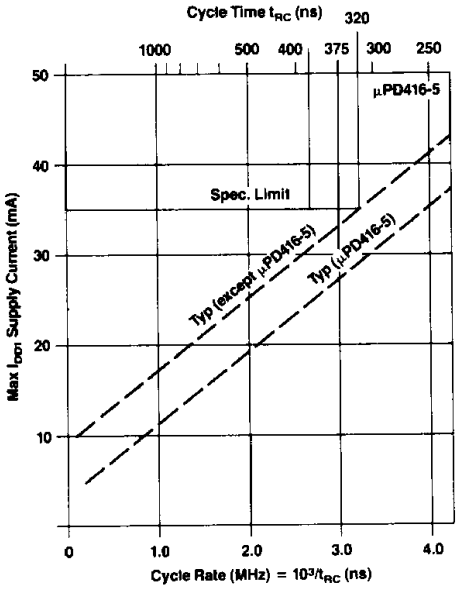


Figure 2. Maximum I_{DD1} versus Cycle Rate for Device Operation at Extended Frequencies

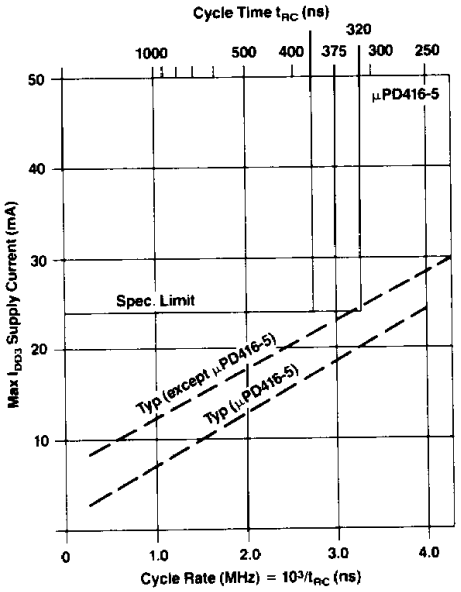


Figure 3. Maximum I_{DD3} versus Cycle Rate for Device Operation at Extended Frequencies

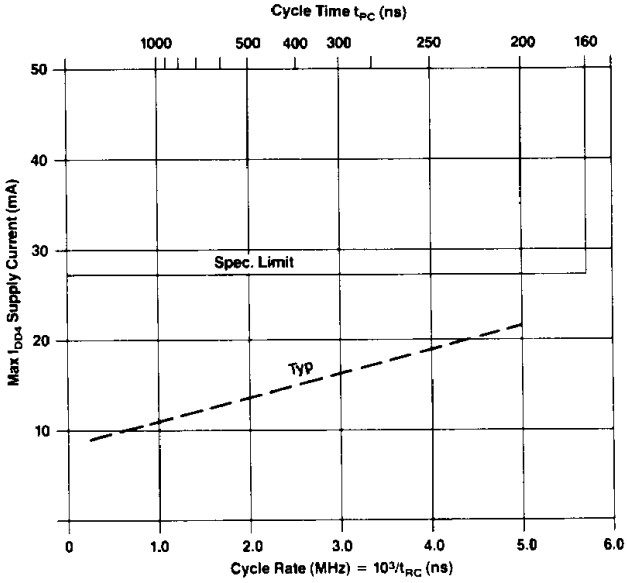


Figure 4. Maximum I_{DD4} versus Cycle Rate for Device Operation in Page Mode

Package Outlines

For information, see Section 9.

Plastic, μPD416C
Ceramic, μPD416D