Features

- **Single 2.7V - 3.6V Supply**
- **Serial Interface Architecture**
- **Page Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **8192 Pages (528 Bytes/Page) Main Memory**
- **Optional Page and Block Erase Operations**
- **Two 528-Byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming of Nonvolatile Memory**
- **Internal Program and Control Timer**
- **Fast Page Program Time – 7 ms Typical**
- **120 µs Typical Page to Buffer Transfer Time**
- **Low-Power Dissipation**
  - **4 mA Active Read Current Typical**
  - **3 µA CMOS Standby Current Typical**
- **13 MHz Max Clock Frequency**
- **Hardware Data Protection Feature**
- **Serial Peripheral Interface (SPI) Compatible – Modes 0 and 3**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Commercial and Industrial Temperature Ranges**

Description

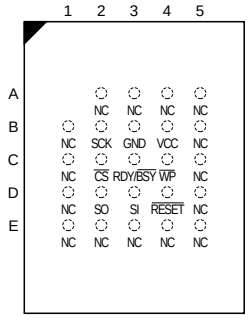
The AT45DB321 is a 2.7-volt only, serial interface Flash memory suitable for in-system reprogramming. Its 34,603,008 bits of memory are organized as 8192 pages of 528 bytes each. In addition to the main memory, the AT45DB321 also contains two SRAM data buffers of 528 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Unlike conventional Flash memo-

(continued)

Pin Configurations

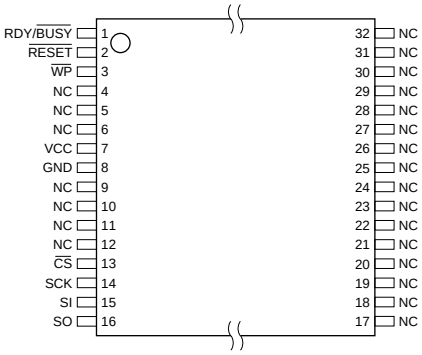
Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy

CBGA Top View Through Package



TSOP Top View

Type 1



32-Megabit 2.7-volt Only Serial DataFlash®

AT45DB321 Preliminary

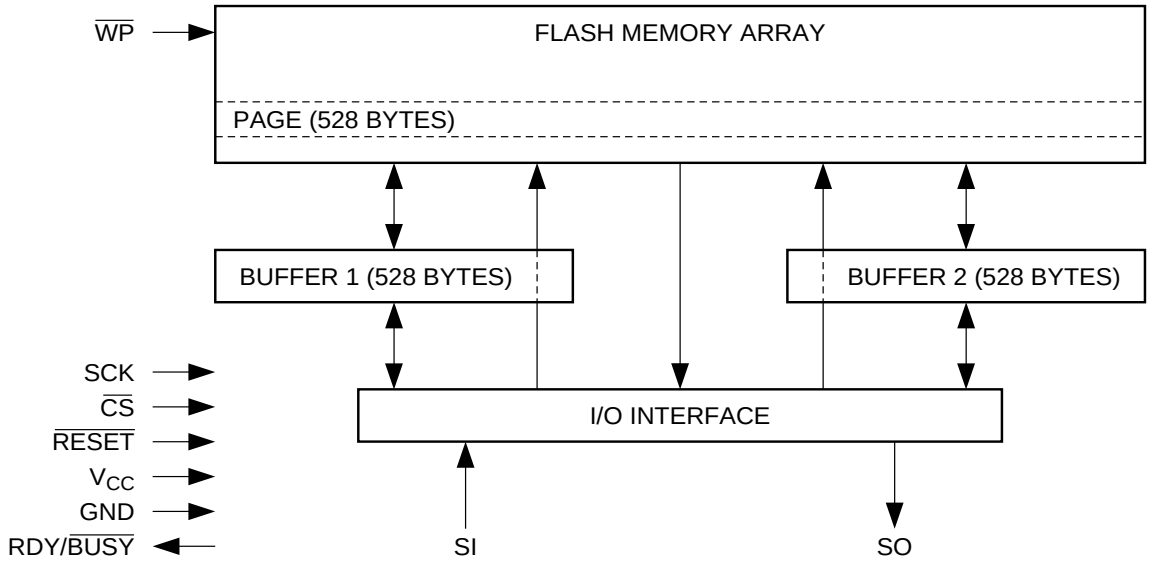
Rev. 1121A–09/98

ries that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. Typical applications for the DataFlash are digital voice storage, image storage, and data storage. The device operates at clock frequencies up to 13 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB321 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB321 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming cycles are self-timed, and no separate erase cycle is required before programming.

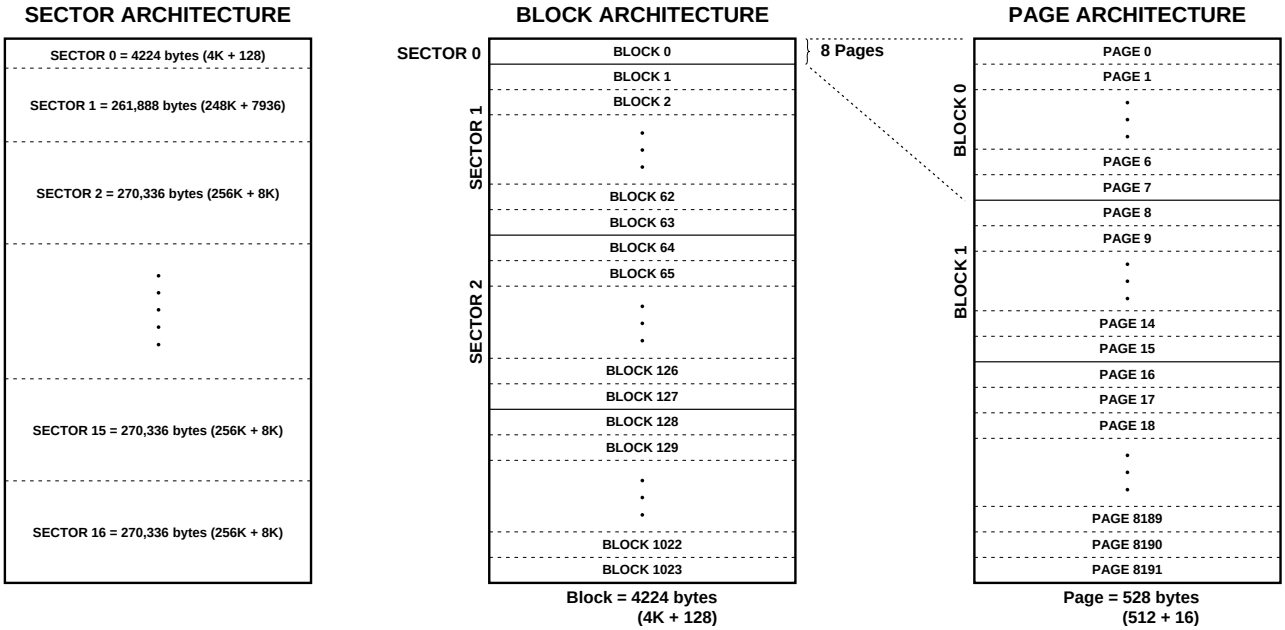
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45DB321 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page by page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 1 and Table 2. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Read

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

MAIN MEMORY PAGE READ: A main memory read allows the user to read data directly from any one of the 8192 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, the 8-bit opcode, 52H, is followed by 24 address bits and 32 don't care bits. In the AT45DB321, the first address bit is reserved for larger density devices (see Notes on page 10), the next 13 address bits (PA12-PA0) specify the page address, and the next 10 address bits (BA9-BA0) specify the starting byte address within the page. The 32 don't care bits which follow the 24 address bits are sent to initialize the read operation. Following the 32 don't care bits, additional pulses on SCK result in serial data being output on the SO (serial output) pin. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, and the reading of data. When the end of a page in main memory is reached during a main memory page read, the device will continue reading at the beginning of the same page. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H is used to read data from buffer 1, and an opcode of 56H is used to read data from buffer 2. To perform a buffer read, the eight bits of the opcode must be followed by 14 don't care bits, 10 address bits, and eight don't care bits. Since the buffer size is 528-bytes, 10 address bits (BFA9-BFA0) are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bits, the don't care bits, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low to high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the SO pin.

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. An 8-bit opcode, 53H for buffer 1 and 55H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) which specify the page in main memory that is to be transferred, and 10 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read to determine whether the transfer has been completed or not.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. An 8-bit opcode, 60H for buffer 1 and 61H for buffer 2, is followed by 24 address bits consisting of one reserved bit, 13 address bits (PA12-PA0) which specify the page in the main memory that is to be compared to the buffer, and 10 don't care bits. The loading of the opcode and the address bits is the same as described previously. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode, the address bits, and the don't care bits from the SI pin. On the low to high transition of the $\overline{CS}$ pin, the 528 bytes in the selected main memory page will be compared with the 528 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

Program

BUFFER WRITE: Data can be shifted in from the SI pin into either buffer 1 or buffer 2. To load data into either buffer, an 8-bit opcode, 84H for buffer 1 or 87H for buffer 2, is followed by 14 don't care bits and 10 address bits (BFA9-BFA0). The 10 address bits specify the first byte in the buffer to be written. The data is entered following the address bits. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low to high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. An 8-bit opcode, 83H for buffer 1 or 86H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. An 8-bit opcode, 88H for buffer 1 or 89H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) that specify the page in the main memory to be written, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased. The programming of the page is internally self timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the part is busy.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device, followed by one reserved bit, 13 address bits (PA12-PA0), and 10 don't care bits. The 13 address bits are used to specify which page of the memory array is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-In Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a Block Erase, an opcode of 50H must be loaded into the device, followed by one reserved bit, 10 address bits (PA12-PA3), and 13 don't care bits. The 10 address bits are used to specify which block of eight pages is to be erased. When a low to high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register will indicate that the part is busy.

Block Erase Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	0	0	X	X	X	1020
1	1	1	1	1	1	1	1	0	1	X	X	X	1021
1	1	1	1	1	1	1	1	1	0	X	X	X	1022
1	1	1	1	1	1	1	1	1	1	X	X	X	1023

MAIN MEMORY PAGE PROGRAM: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations. Data is first shifted into buffer 1 or buffer 2 from the SI pin and then programmed into a specified page in the main memory. An 8-bit opcode, 82H for buffer 1 or 85H for buffer 2, is followed by one reserved bit and 23 address bits. The 13 most significant address bits (PA12-PA0) select the page in the main memory where data is to be written, and the next 10 address bits (BFA9-BFA0) select the first byte in the buffer to be written. After all address bits are shifted in, the part will take data from the SI pin and store it in one of the data buffers. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low to high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. An 8-bit opcode, 58H for buffer 1 or 59H for buffer 2, is followed by one reserved bit, 13 address bits (PA12-PA0) that specify the page in main memory to be rewritten, and 10 additional don't care bits. When a low to high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 is recommended.

STATUS REGISTER: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK once bit 7 has been output. The status of bit 7 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 0 to 1. There are eight operations which can

cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-In Erase, Buffer to Main Memory Page Program without Built-In Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, and 3 of the status register. For the AT45DB321, the three bits are 1, 1, and 0. The decimal value of these three binary bits does not equate to the device density; the three bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of eight different density configurations.

Read/Program Mode Summary

The modes listed above can be separated into two groups — modes which make use of the flash memory array (Group A) and modes which do not make use of the flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page Read
2. Main Memory Page to Buffer 1 (or 2) Transfer
3. Main Memory Page to Buffer 1 (or 2) Compare
4. Buffer 1 (or 2) to Main Memory Page Program With Built-In Erase
5. Buffer 1 (or 2) to Main Memory Page Program Without Built-In Erase
6. Page Erase
7. Block Erase
8. Main Memory Page Program
9. Auto Page Rewrite

Group B modes consist of:

1. Buffer 1 (or 2) Read
2. Buffer 1 (or 2) Write
3. Status Register Read

If a Group A mode is in progress (not fully completed) then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the Serial DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

HARDWARE PAGE WRITE PROTECT: If the $\overline{WP}$ pin is held low, the first 256 pages of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{WP}$ pin is internally pulled high; therefore, connection of the $\overline{WP}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{WP}$ pin be driven high externally whenever possible.

$\overline{RESET}$: A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. The $\overline{RESET}$ pin is also internally pulled high; therefore, connection of the $\overline{RESET}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{RESET}$ pin be driven high externally whenever possible.

READY/$\overline{BUSY}$: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming operations, compare operations, and during page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

Power On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI mode 3. In addition, the SO pin will be in a high impedance state, and a high to low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	1	0	X	X	X

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB321
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified data sheet value, the system should wait 20 ms before an operational mode is started.

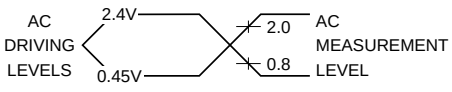
DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		3	10	µA
I_{CC1}	Active Current, Read Operation	f = 13 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

AC Characteristics

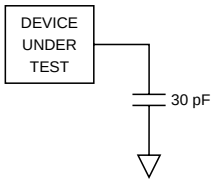
Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			13	MHz
t_{WH}	SCK High Time	35			ns
t_{WL}	SCK Low Time	35			ns
t_{CS}	Minimum $\overline{CS}$ High Time	250			ns
t_{CSS}	$\overline{CS}$ Setup Time	250			ns
t_{CSH}	$\overline{CS}$ Hold Time	250			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			200	ns
t_{SU}	Data In Setup Time	10			ns
t_H	Data In Hold Time	20			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			25	ns
t_V	Output Valid			30	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		120	200	µs
t_{EP}	Page Erase and Programming Time		10	20	ms
t_P	Page Programming Time		7	15	ms
t_{PE}	Page Erase Time		6	10	ms
t_{BE}	Block Erase Time		7	15	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load

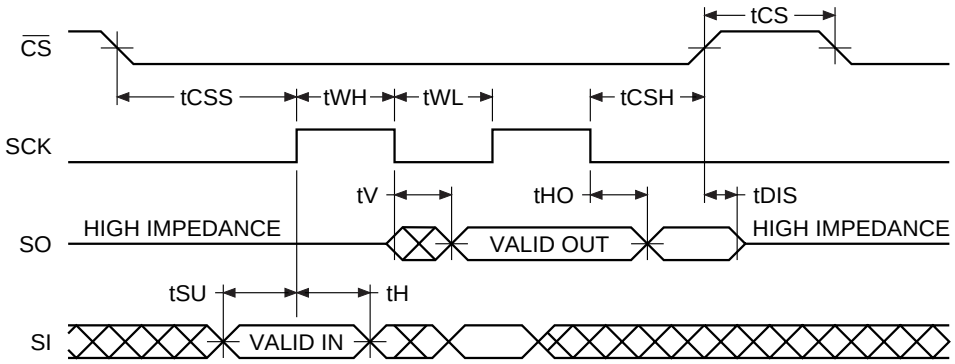


AC Waveforms

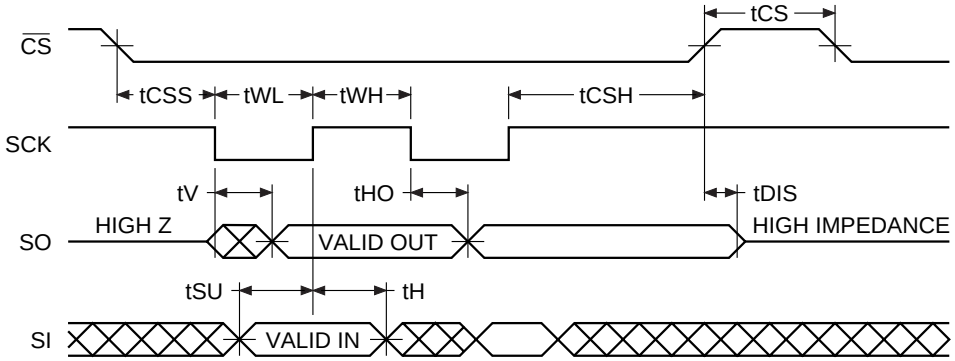
Two different timing diagrams are shown below. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3

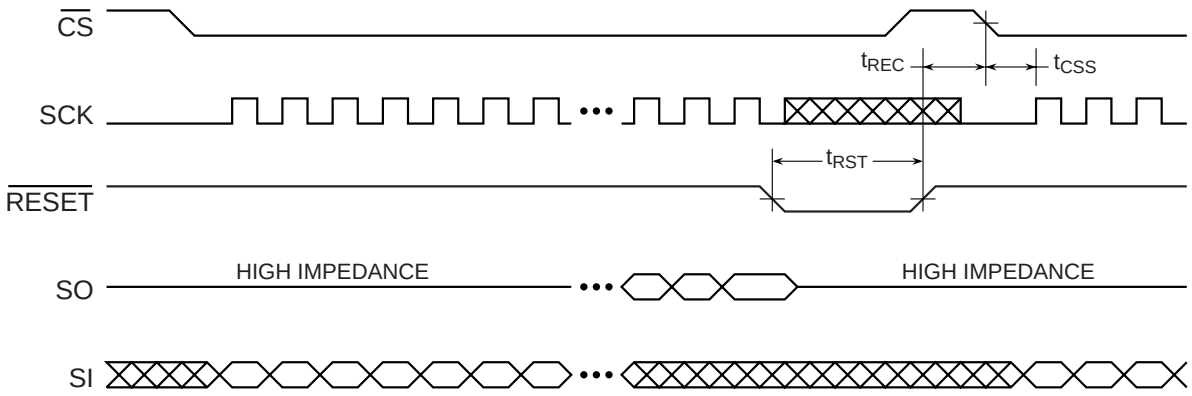
Waveform 1 – Inactive Clock Polarity Low



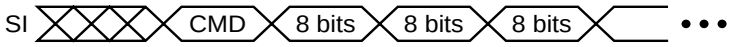
Waveform 2 – Inactive Clock Polarity High

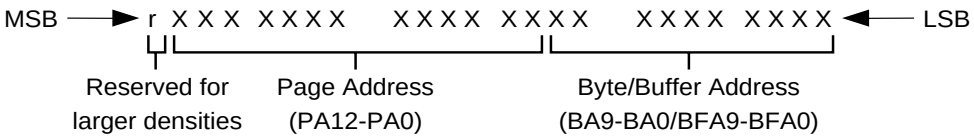


Reset Timing (Inactive Clock Polarity Low Shown)



Command Sequence for Read/Write Operations (Except Status Register Read)

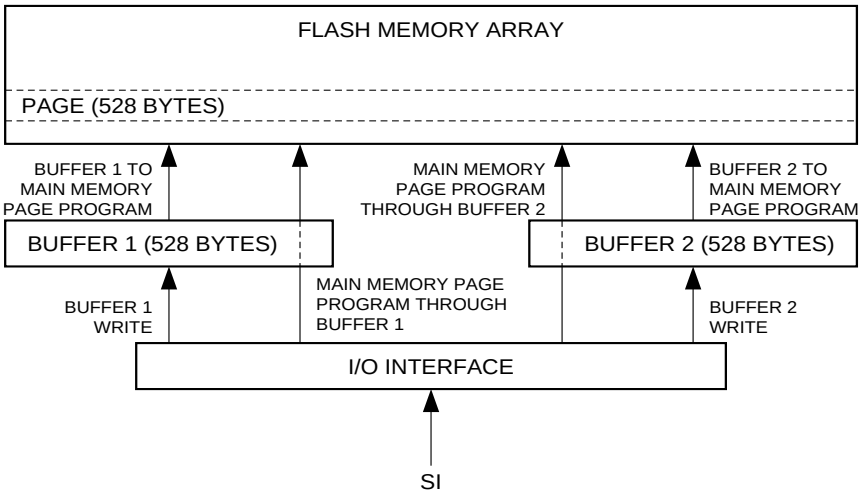




Notes: 1. "r" designates bits reserved for larger densities.
2. It is recommended that "r" be a logical "0" for densities of 32M bit or smaller.
3. For densities larger than 32M bit, the "r" bits become the most significant Page Address bit for the appropriate density.

Write Operations

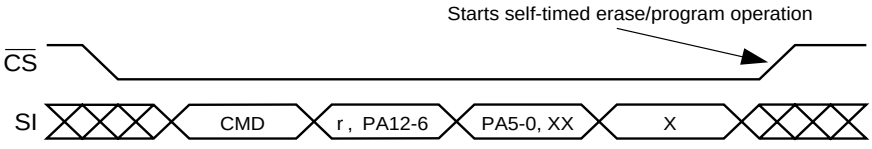
The following block diagram and waveforms illustrate the various write sequences available.

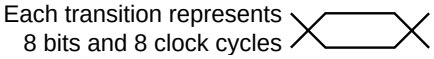


Main Memory Page Program through Buffers

Buffer Write

Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

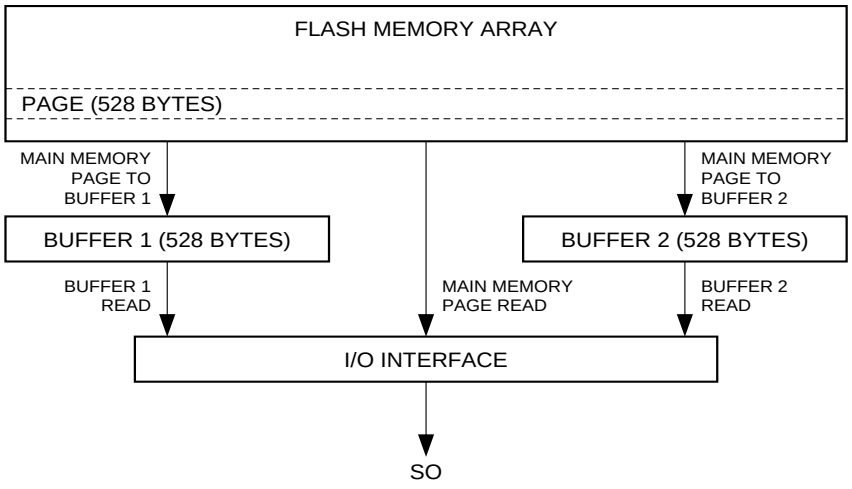




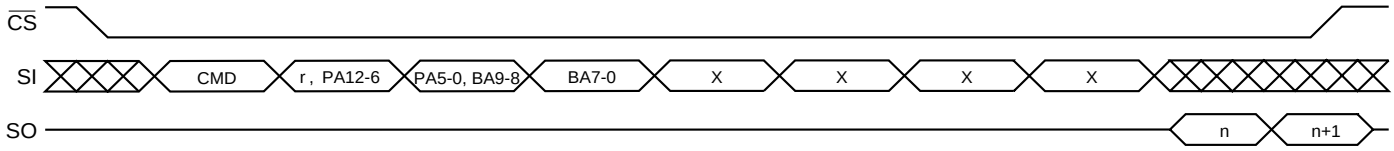
n = 1st byte written
n+1 = 2nd byte written

Read Operations

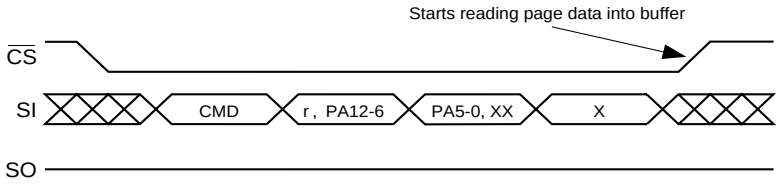
The following block diagram and waveforms illustrate the various read sequences available.



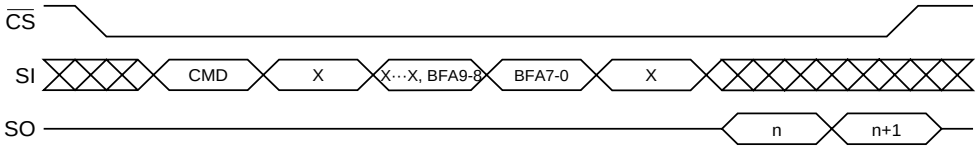
Main Memory Page Read



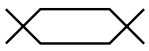
Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read



Each transition represents 8 bits and 8 clock cycles

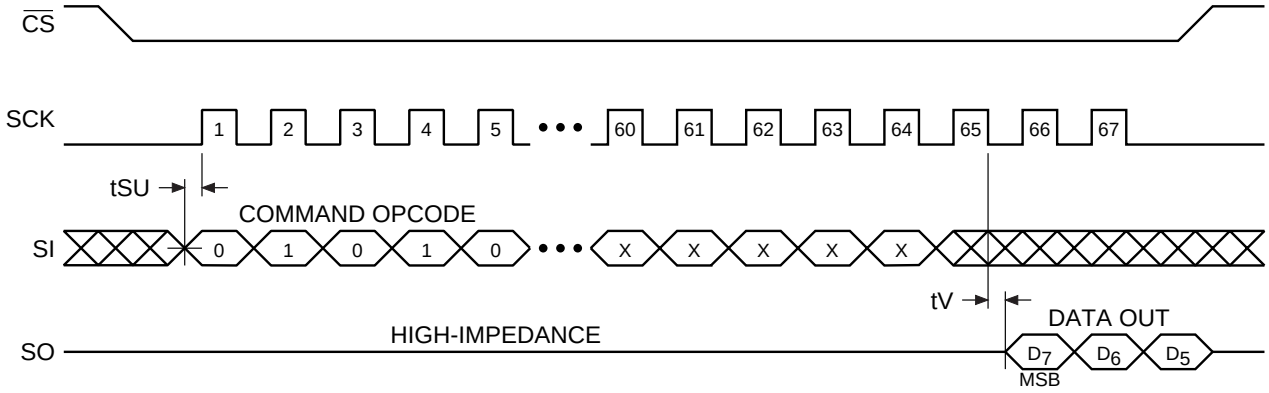


n = 1st byte read

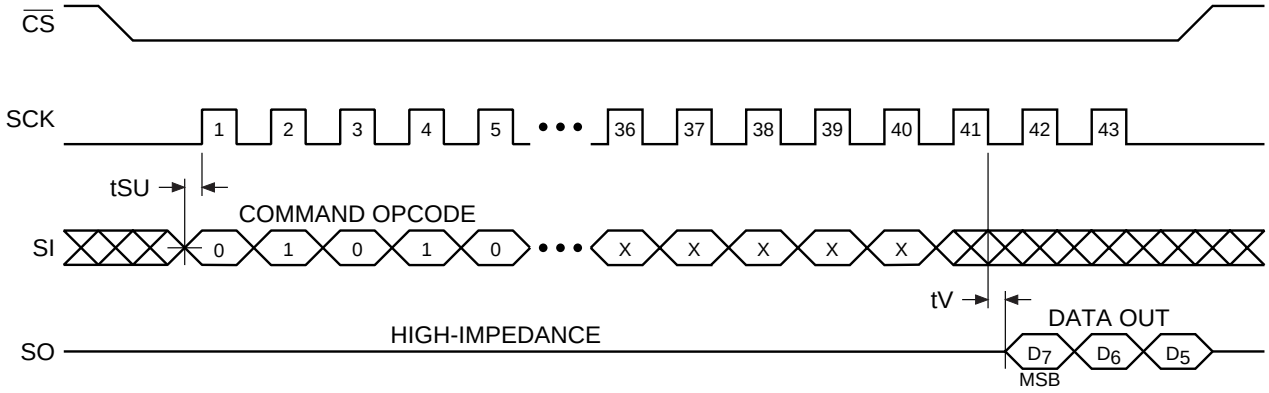
n+1 = 2nd byte read

Detailed Bit-Level Read Timing – Inactive Clock Polarity Low

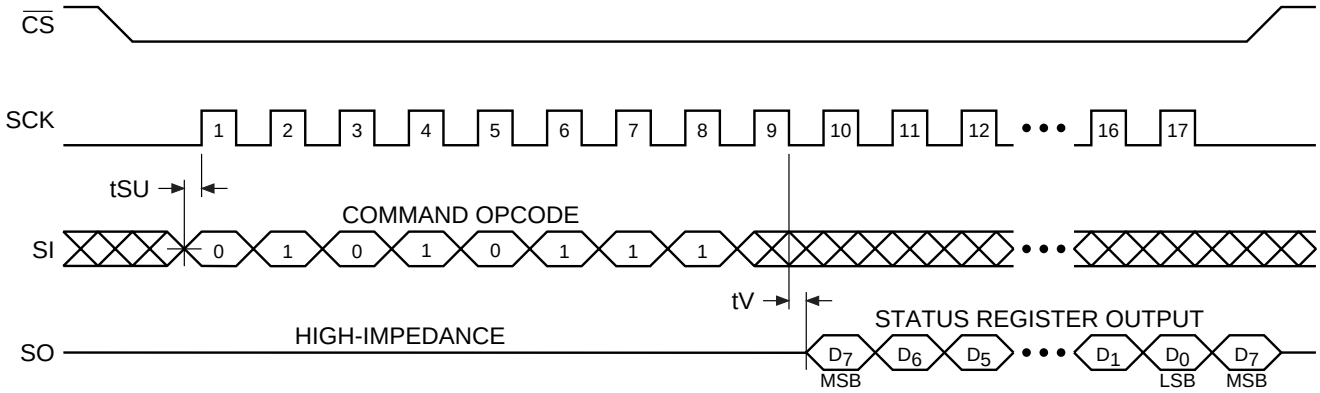
Main Memory Page Read



Buffer Read

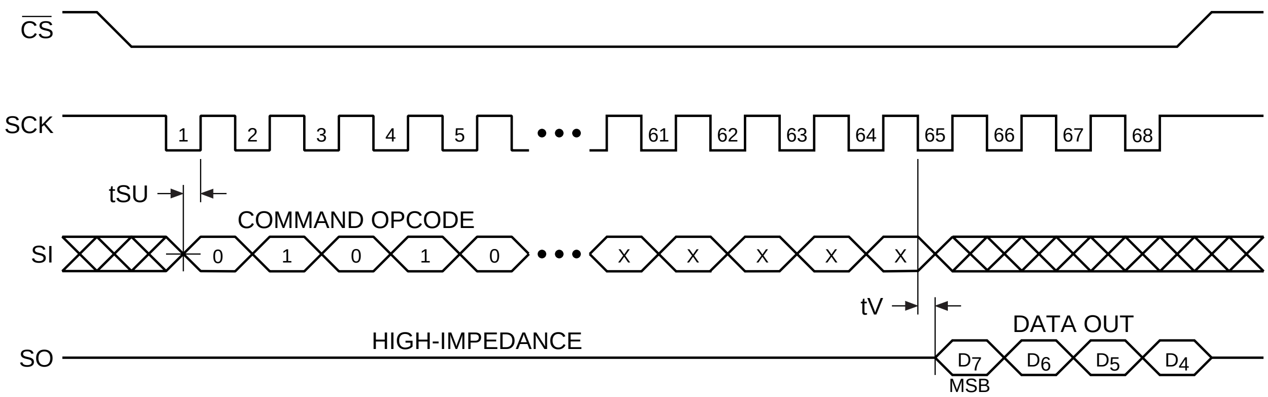


Status Register Read

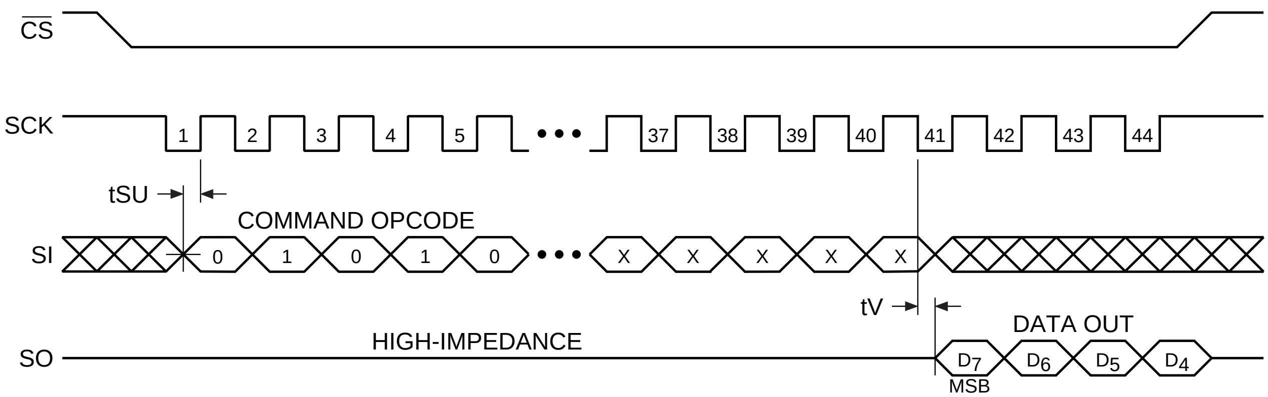


Detailed Bit-Level Read Timing – Inactive Clock Polarity High

Main Memory Page Read



Buffer Read



Status Register Read

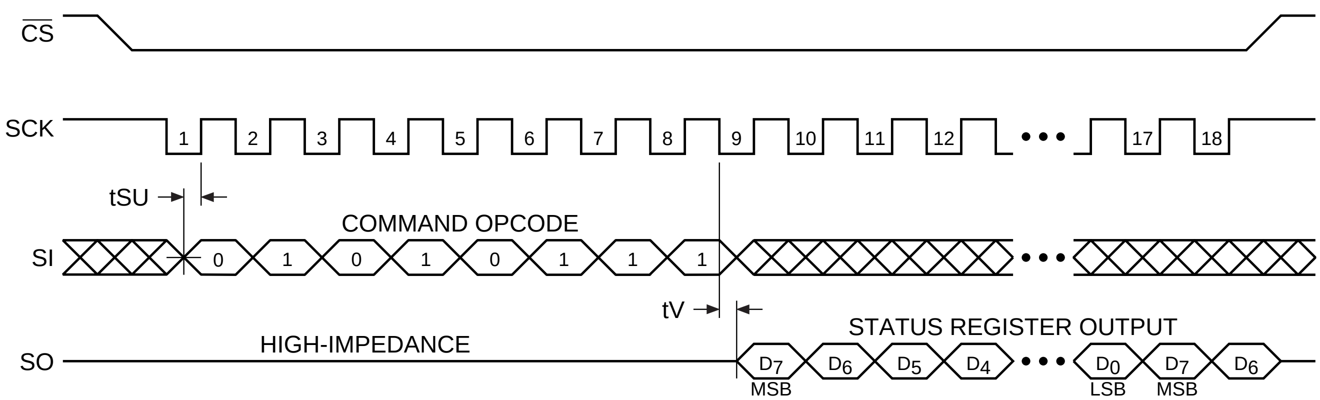


Table 1.

Main Memory Page Read	Buffer 1 Read	Buffer 2 Read	Main Memory Page to Buffer 1 Transfer	Main Memory Page to Buffer 2 Transfer	Main Memory Page to Buffer 1 Compare	Main Memory Page to Buffer 2 Compare	Buffer 1 Write	Buffer 2 Write
Opcode								
52H	54H	56H	53H	55H	60H	61H	84H	87H
0	0	0	0	0	0	0	1	1
1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	1	0	0
1	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	1
0	0	0	1	1	0	1	0	1
r	X	X	r	r	r	r	X	X
PA12	X	X	PA12	PA12	PA12	PA12	X	X
PA11	X	X	PA11	PA11	PA11	PA11	X	X
PA10	X	X	PA10	PA10	PA10	PA10	X	X
PA9	X	X	PA9	PA9	PA9	PA9	X	X
PA8	X	X	PA8	PA8	PA8	PA8	X	X
PA7	X	X	PA7	PA7	PA7	PA7	X	X
PA6	X	X	PA6	PA6	PA6	PA6	X	X
PA5	X	X	PA5	PA5	PA5	PA5	X	X
PA4	X	X	PA4	PA4	PA4	PA4	X	X
PA3	X	X	PA3	PA3	PA3	PA3	X	X
PA2	X	X	PA2	PA2	PA2	PA2	X	X
PA1	X	X	PA1	PA1	PA1	PA1	X	X
PA0	X	X	PA0	PA0	PA0	PA0	X	X
BA9	BFA9	BFA9	X	X	X	X	BFA9	BFA9
BA8	BFA8	BFA8	X	X	X	X	BFA8	BFA8
BA7	BFA7	BFA7	X	X	X	X	BFA7	BFA7
BA6	BFA6	BFA6	X	X	X	X	BFA6	BFA6
BA5	BFA5	BFA5	X	X	X	X	BFA5	BFA5
BA4	BFA4	BFA4	X	X	X	X	BFA4	BFA4
BA3	BFA3	BFA3	X	X	X	X	BFA3	BFA3
BA2	BFA2	BFA2	X	X	X	X	BFA2	BFA2
BA1	BFA1	BFA1	X	X	X	X	BFA1	BFA1
BA0	BFA0	BFA0	X	X	X	X	BFA0	BFA0
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
X	X	X						
•								
•								
•								
X (64th bit)								

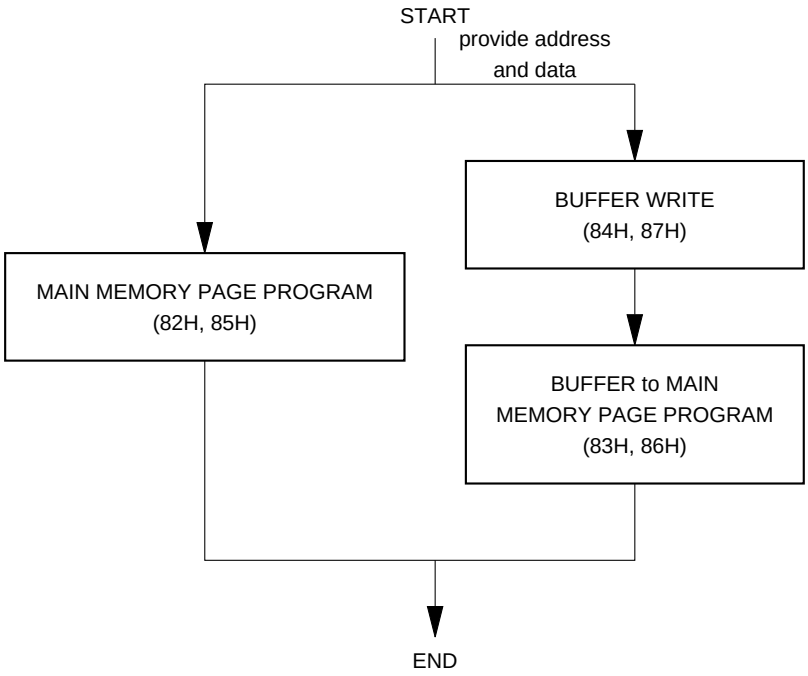
X (Don't Care)
r (reserved bits)

Table 2.

Buffer 1 to Main Memory Page Program with Built In Erase	Buffer 2 to Main Memory Page Program with Built-In Erase	Buffer 1 to Main Memory Page Program without Built-In Erase	Buffer 2 to Main Memory Page Program without Built-In Erase	Page Erase	Block Erase	Main Memory Page Program Through Buffer 1	Main Memory Page Program Through Buffer 2	Auto Page Rewrite Through Buffer 1	Auto Page Rewrite Through Buffer 2	Status Register
Opcode										
83H	86H	88H	89H	81H	50H	82H	85H	58H	59H	57H
1	1	1	1	1	0	1	1	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	1	1
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1	1
r	r	r	r	r	r	r	r	r	r	
PA12	PA12	PA12	PA12	PA12	PA12	PA12	PA12	PA12	PA12	
PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	PA11	
PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	PA10	
PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	PA9	
PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	PA8	
PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	PA7	
PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	PA6	
PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	PA5	
PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	PA4	
PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	PA3	
PA2	PA2	PA2	PA2	PA2	X	PA2	PA2	PA2	PA2	
PA1	PA1	PA1	PA1	PA1	X	PA1	PA1	PA1	PA1	
PA0	PA0	PA0	PA0	PA0	X	PA0	PA0	PA0	PA0	
X	X	X	X	X	X	BFA9	BFA9	X	X	
X	X	X	X	X	X	BFA8	BFA8	X	X	
X	X	X	X	X	X	BFA7	BFA7	X	X	
X	X	X	X	X	X	BFA6	BFA6	X	X	
X	X	X	X	X	X	BFA5	BFA5	X	X	
X	X	X	X	X	X	BFA4	BFA4	X	X	
X	X	X	X	X	X	BFA3	BFA3	X	X	
X	X	X	X	X	X	BFA2	BFA2	X	X	
X	X	X	X	X	X	BFA1	BFA1	X	X	
X	X	X	X	X	X	BFA0	BFA0	X	X	

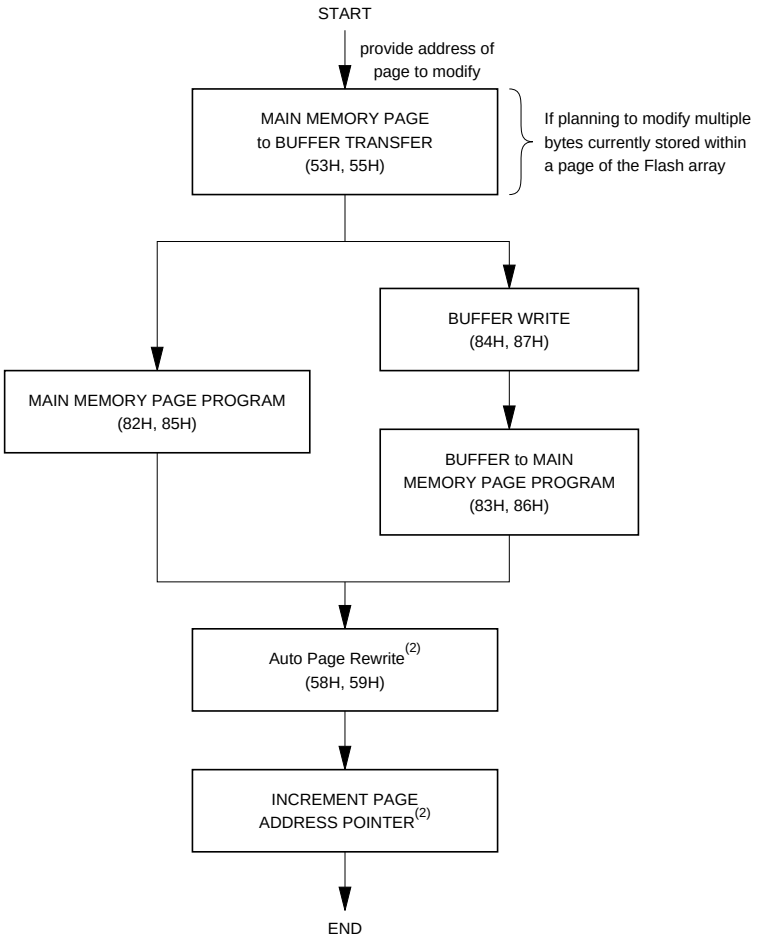
X (Don't Care)
r (reserved bits)

Figure 1. Algorithm for Programming or Reprogramming of an Entire Sector Sequentially



Notes:
1. This type of algorithm is used for applications in which an entire sector is programmed sequentially, filling the sector page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire sector.

Figure 2. Algorithm for Randomly Modifying Data



Notes: 1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations within that sector.

2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.

3. Other algorithms can be used to rewrite portions of the Flash array. Low power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

Sector Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	Sector
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	X	X	X	X	X	X	1
0	0	0	1	X	X	X	X	X	X	2
0	0	1	0	X	X	X	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
1	1	0	0	X	X	X	X	X	X	13
1	1	0	1	X	X	X	X	X	X	14
1	1	1	0	X	X	X	X	X	X	15
1	1	1	1	X	X	X	X	X	X	16

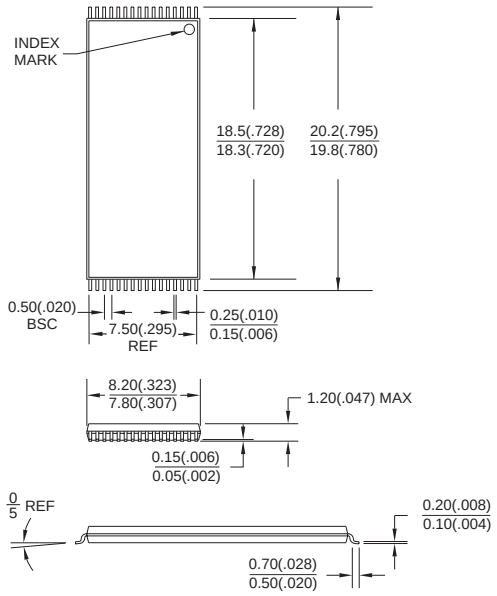
Ordering Information

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
13	10	0.01	AT45DB321-TC AT45DB321-CC	32T 24C3	Commercial (0°C to 70°C)
13	10	0.01	AT45DB321-TI AT45DB321-CI	32T 24C3	Industrial (-40°C to 85°C)

Package Type	
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)
24C3	24-Ball, 5 x 5 Array Plastic Chip-Scale Ball Grid Array (CBGA)

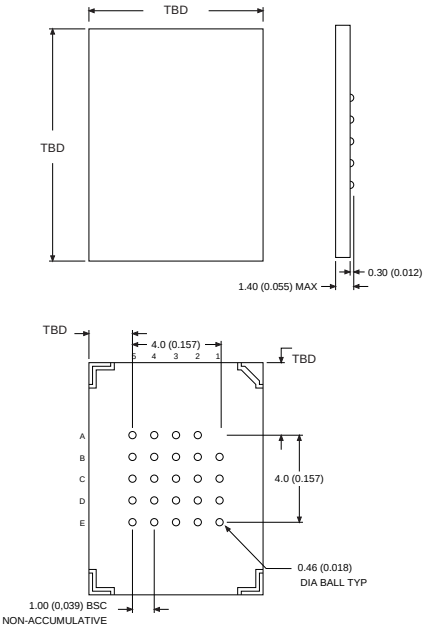
Packaging Information

32T, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 BD



*Controlling dimension: millimeters

24C3, 24-Ball (5 x 5 array), 1.0mm Pitch, Plastic Chip-scale Ball Grid Array (CBGA)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

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