



**PRELIMINARY**

**CY62256V**

**32K x 8 Static RAM**

**Features**

- 55, 70 ns access time
- CMOS for optimum speed/power
- Wide voltage range: 2.7V–3.6V
- Low active power (70 ns, LL version) — 108 mW (max.)
- Low standby power (70 ns, LL version) — 18 μW (max.)
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

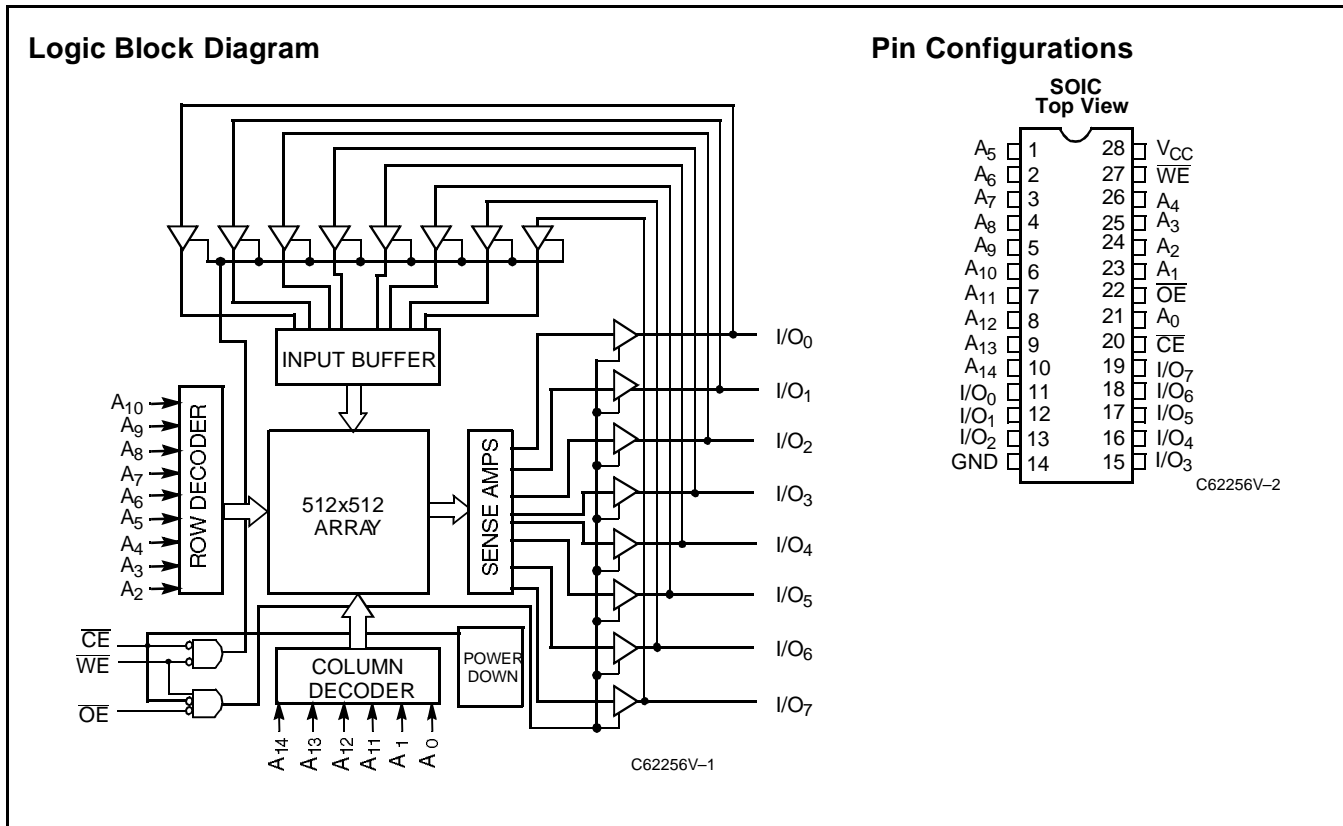
**Functional Description**

The CY62256V is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active

LOW output enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 98% when deselected. The CY62256V is in the standard 450-mil-wide (300-mil body width) SOIC, TSOP, and reverse TSOP packages.

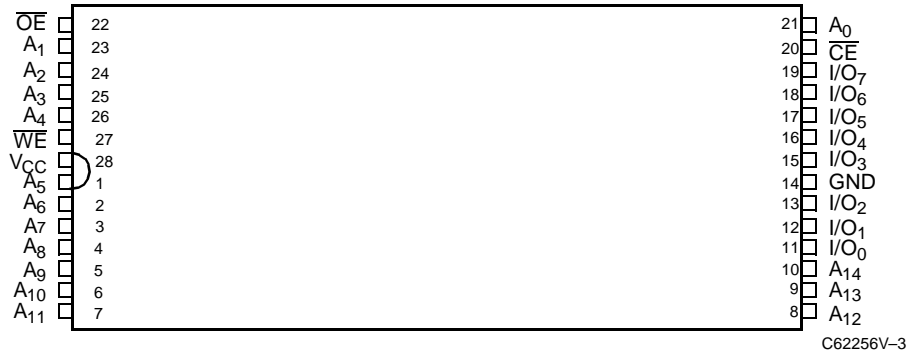
An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to ensure alpha immunity.

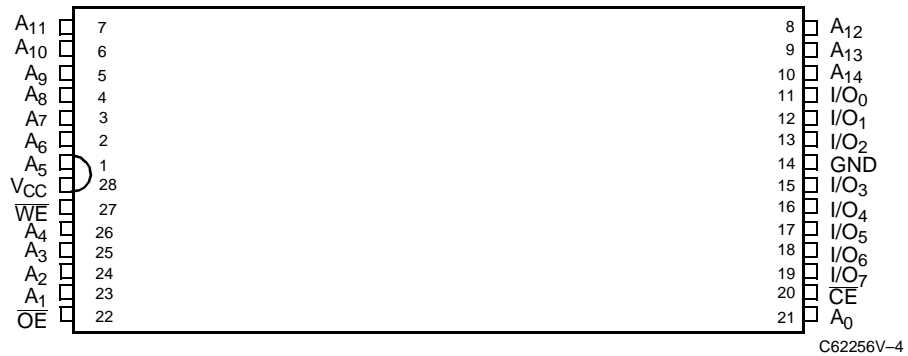


**Pin Configurations** (continued)

**TSOP  
Top View**



**TSOP Reversed  
Top View**



**Selection Guide**

		<b>CY62256V-55</b>	<b>CY62256V-70</b>
Maximum Access Time (ns)		55	70
Maximum Operating Current (mA)		50	50
	L	50	50
	LL	30	30
Maximum Standby Current (µA)		500	500
	L	50	50
	LL	5	5

Shaded area contains advanced information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... 0°C to +70°C
- Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- DC Input Voltage<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> + 0.5V
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	2.7V to 3.6V

**Note:**

- 1. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62256V-55		CY62256V-70		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> +0.3V	2.2	V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[2]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-200		-200	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		50		50	mA
			L	50		50	mA
			LL	30		30	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		5		5	mA
			L	3		3	mA
			LL	1		1	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		500		500	μA
			L	50		50	μA
			LL	5		5	μA

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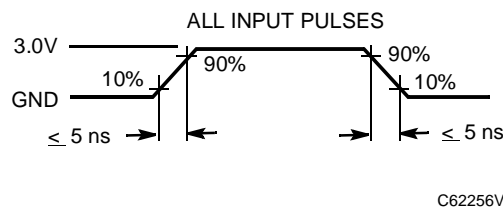
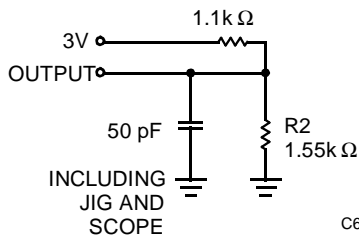
**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

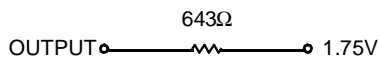
**Notes:**

- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



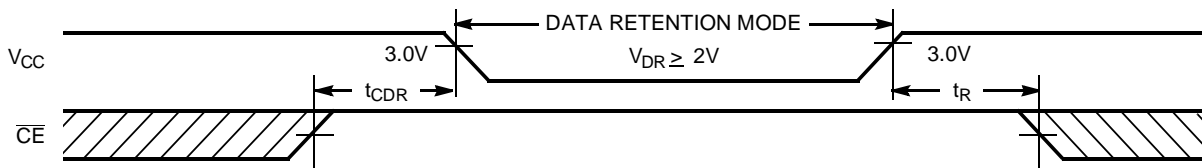
Equivalent to: THÉVENIN EQUIVALENT



**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions <sup>[4]</sup>	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0		V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> = 3.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		200	μA
			L	20	μA
			LL	5	μA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0		ns
t <sub>R</sub> <sup>[3]</sup>	Operation Recovery Time		t <sub>RC</sub>		ns

**Data Retention Waveform**



C62256V-7

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

Parameter	Description	CY62256V-55		CY62256V-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	CE LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	OE LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>PU</sub>	CE LOW to Power-Up	0		0		ns
t <sub>PD</sub>	CE HIGH to Power-Down		55		70	ns

Shaded area contains advanced information.

**Notes:**

- No input may exceed V<sub>CC</sub>+0.3V.
- Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>; t<sub>HZOE</sub> is less than t<sub>LZOE</sub>; and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.

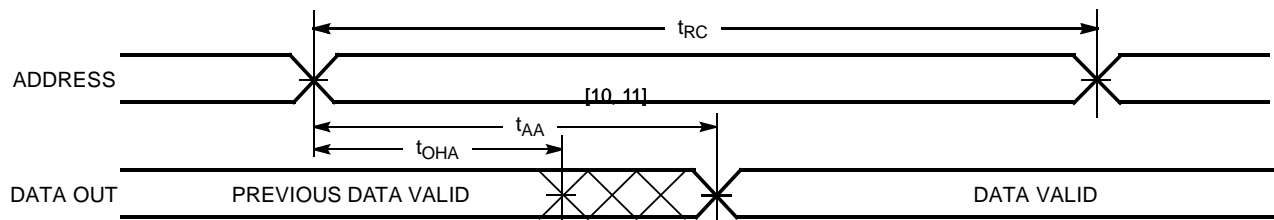
**Switching Characteristics** Over the Operating Range<sup>[5]</sup> (continued)

Parameter	Description	CY62256V-55		CY62256V-70		Unit
		Min.	Max.	Min.	Max.	
<b>WRITE CYCLE<sup>[8,9]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	45		60		ns
$t_{AW}$	Address Set-Up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		50		ns
$t_{SD}$	Data Set-Up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High $Z$ <sup>[6, 7]</sup>		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low $Z$ <sup>[6]</sup>	3		3		ns

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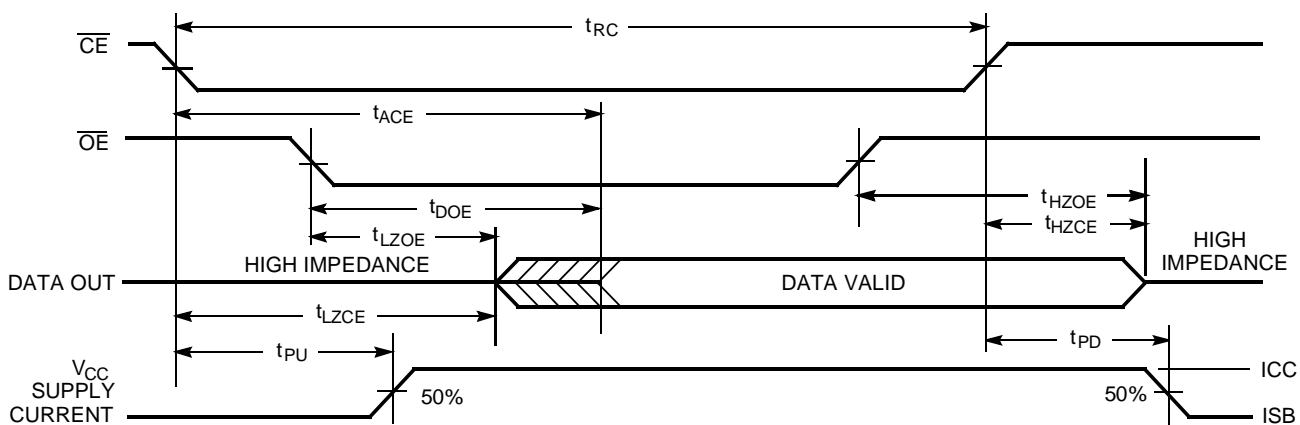
**Switching Waveforms**

**Read Cycle No. 1<sup>[10, 11]</sup>**



C62256V-8

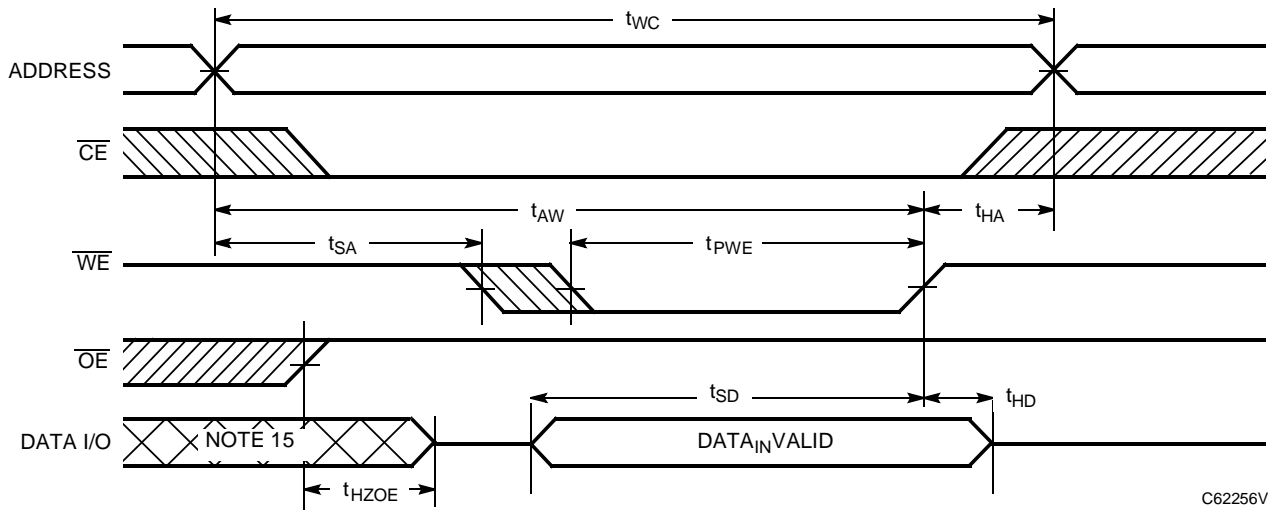
**Read Cycle No. 2<sup>[11, 12]</sup>**



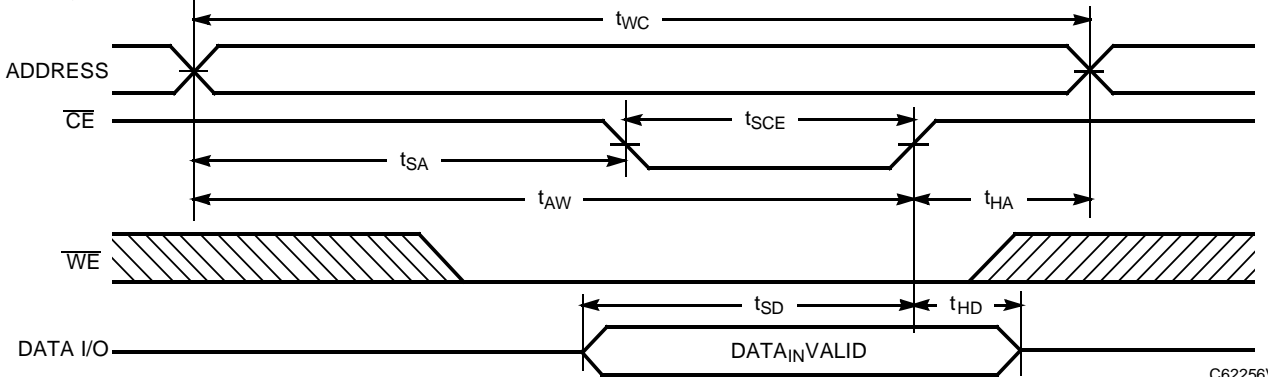
C62256V-9

**Notes:**

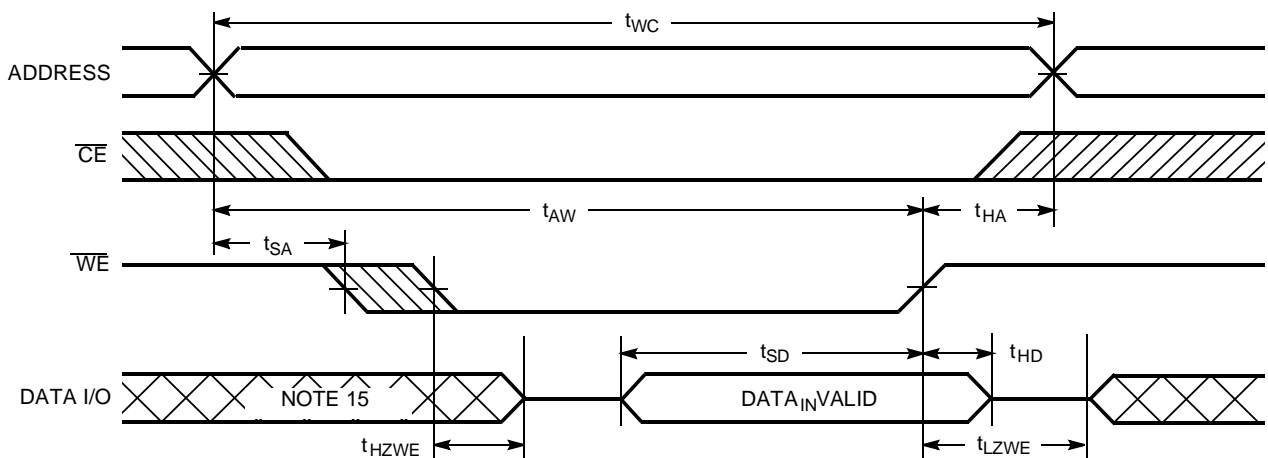
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 (WE Controlled)** [8, 13, 14]


C62256V-10

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** [8, 13, 14]


C62256V-11

**Write Cycle No. 3 (WE Controlled,  $\overline{OE}$  LOW)** [9, 14]


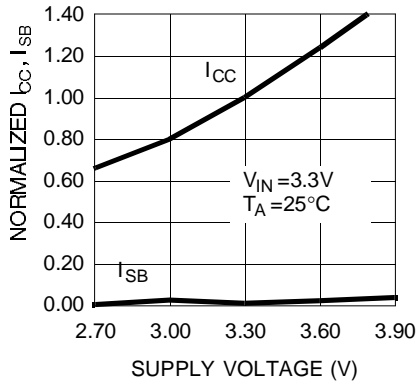
C62256V-12

**Notes:**

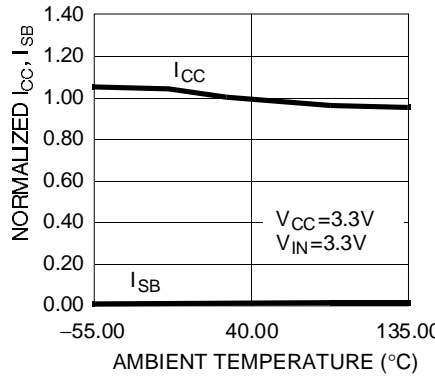
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Typical DC and AC Characteristics**

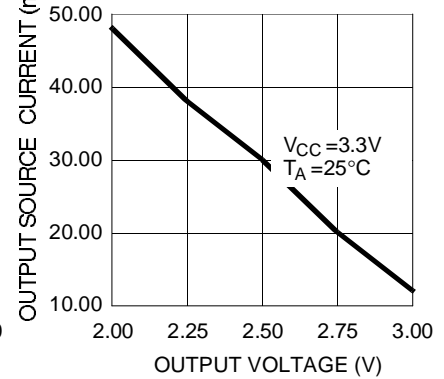
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



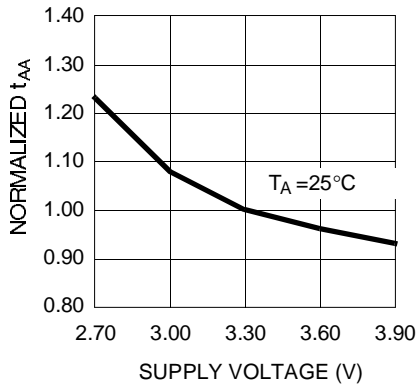
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



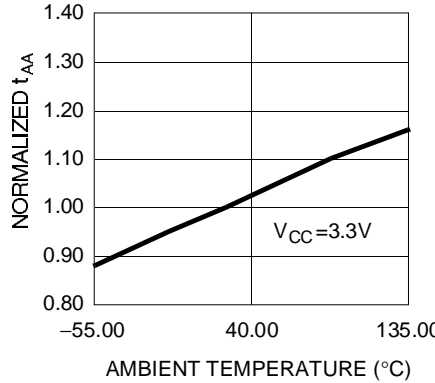
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



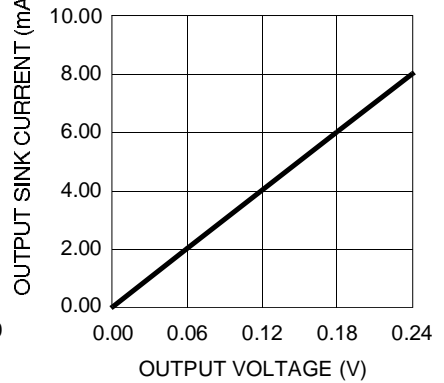
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



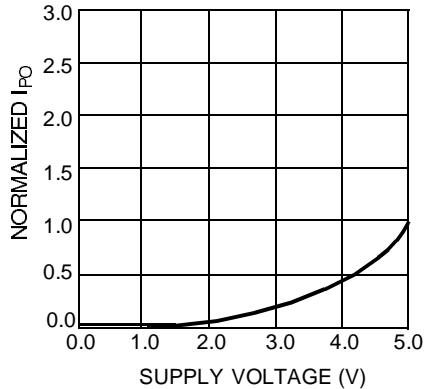
**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**



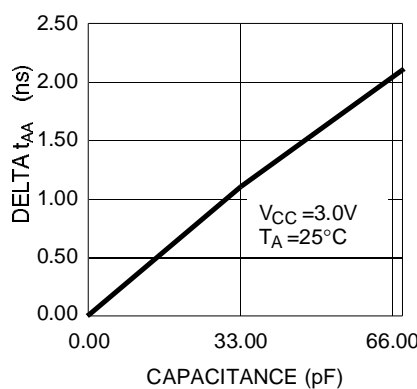
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



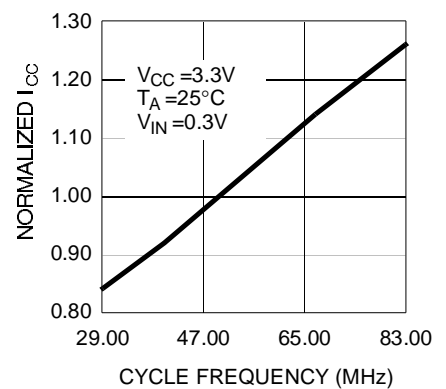
**TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE**



**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**



**NORMALIZED I<sub>CC</sub> vs. CYCLE TIME**



**Truth Table**

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62256V-55SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	<b>Commercial</b>
	CY62256VL-55SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256VLL-55SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256V-55RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VL-55RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VLL-55RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256V-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256VL-55ZC	Z28	28-Lead Thin Small Outline Package	
70	CY62256V-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	<b>Commercial</b>
	CY62256VL-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256VLL-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256V-70RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VL-70RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VLL-70RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256V-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256VL-70ZC	Z28	28-Lead Thin Small Outline Package	
CY62256VLL-70ZC	Z28	28-Lead Thin Small Outline Package		

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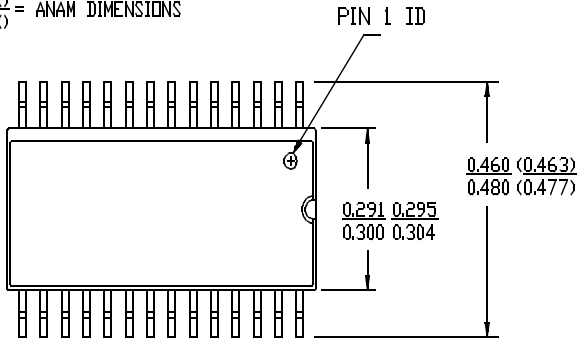


**Package Diagrams**

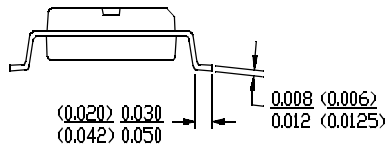
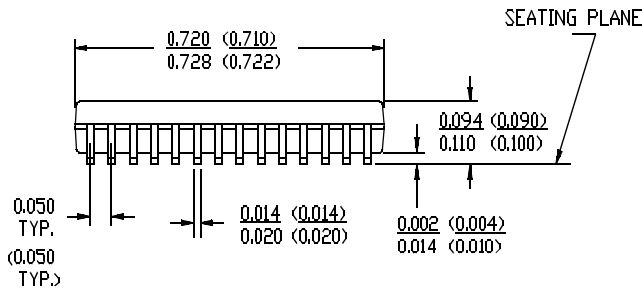
**28-Lead 450-Mil (300-Mil Body Width) SOIC S22**

$\frac{XXX}{.XXX}$  = HYUNDAI DIMENSIONS

$\frac{<XXX>}{<XXX>}$  = ANAM DIMENSIONS



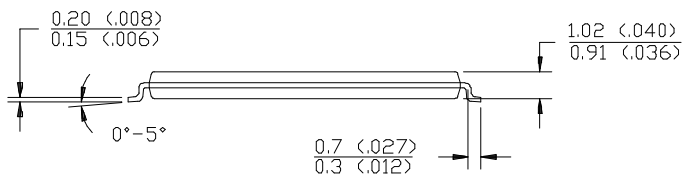
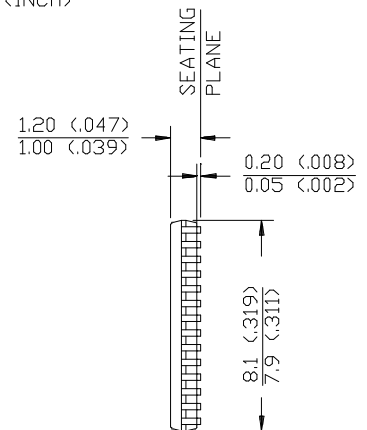
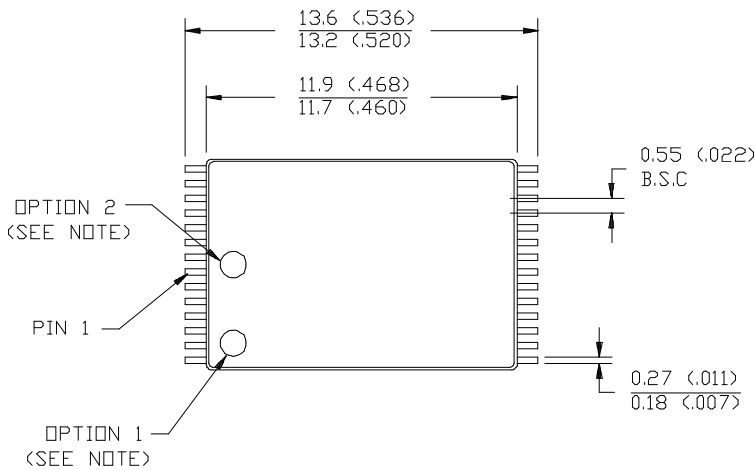
DIMENSIONS IN INCHES MIN.  
MAX.  
LEAD COPLANARITY 0.004 MAX.



**28-Lead Reverse Thin Small Outline Package RZ28**

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (<INCH>  
MAX.  
MIN.



**Package Diagrams (continued)**
**28-Lead Thin Small Outline Package Z28**

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)  
MAX.  
MIN.

