64K (8K x 8) High Speed CMOS E^{2}PROM with Page Write and Software Data Protection

Features

- Fast Read Access Time - 55 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Description

The AT28HC64B is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

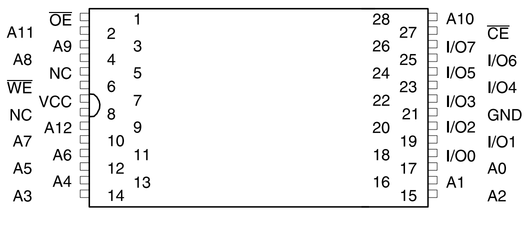
The AT28HC64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow

(continued)

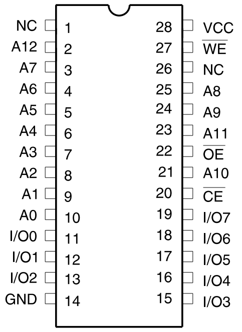
Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

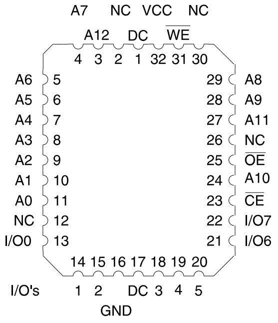
TSOP
Top View



PDIP, SOIC
Top View



PLCC
Top View



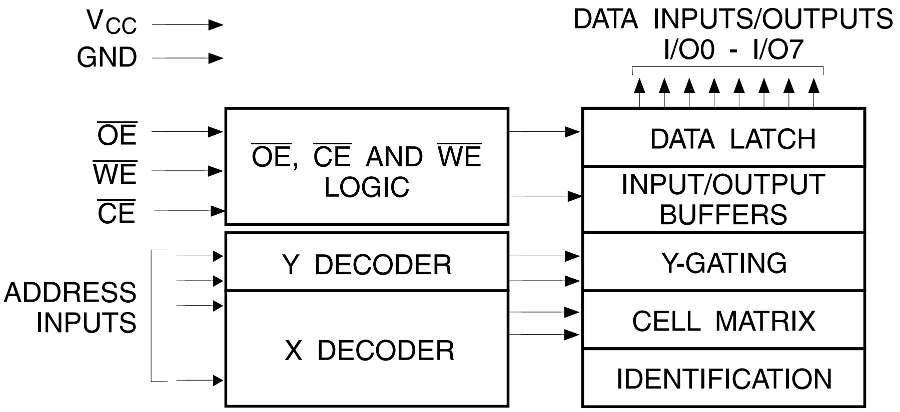
Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28HC64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28HC64B is accessed like a Static RAM. When CE and OE are low and WE is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either CE or OE is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the WE or CE input with CE or WE low (respectively) and OE high initiates a write cycle. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC64B allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28HC64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each WE high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28HC64B features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to DATA Polling, the AT28HC64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64B in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical), the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of OE low, CE high or WE high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software-controlled data protection feature has been implemented on the AT28HC64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the *Software Data Protection Algorithm* diagram in this data sheet). After writing the 3-byte command sequence and waiting t_{WC}, the entire AT28HC64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28HC64B. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28HC64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device, however. For the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 64-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28HC64B-55	AT28HC64B-70	AT28HC64B-90	AT28HC64B-120
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to the *AC Write Waveforms* diagrams in this data sheet.
3. V_H = 12.0V ± 0.5V.

DC Characteristics

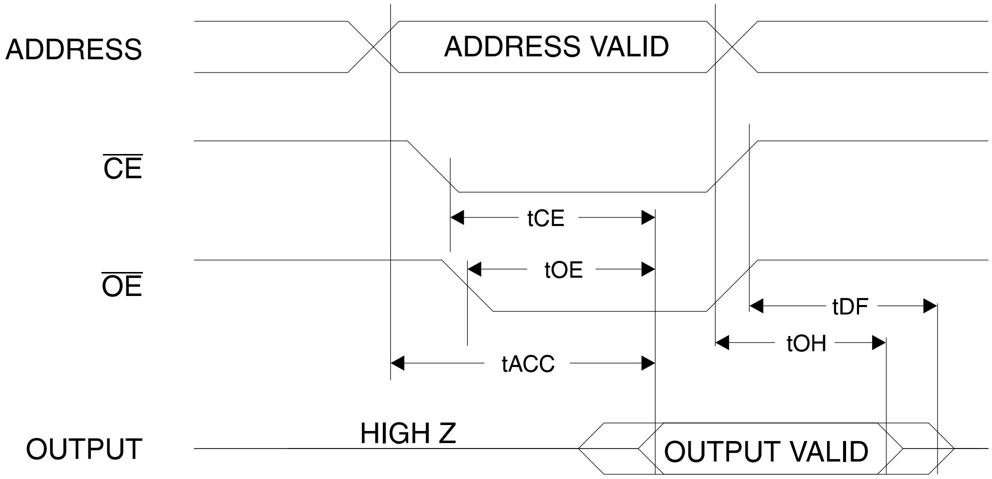
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com., Ind.		100 (1)	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V			2 (1)	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

Note: 1. I_{SB1} and I_{SB2} for the 55 ns part is 40 mA maximum.

AC Read Characteristics

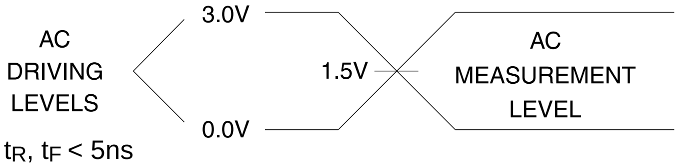
		AT28HC64B-55		AT28HC64B-70		AT28HC64B-90		AT28HC64B-120		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	Min	Max	**Units**
t_{ACC}	Address to Output Delay		55		70		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	30	0	35	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{OE}$ to Output Float	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)

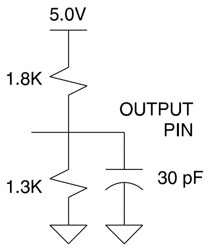


Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

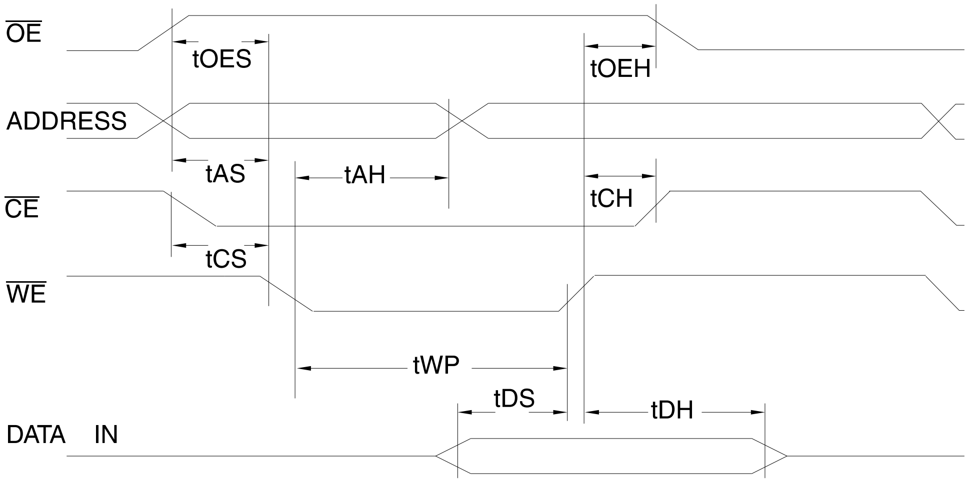
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

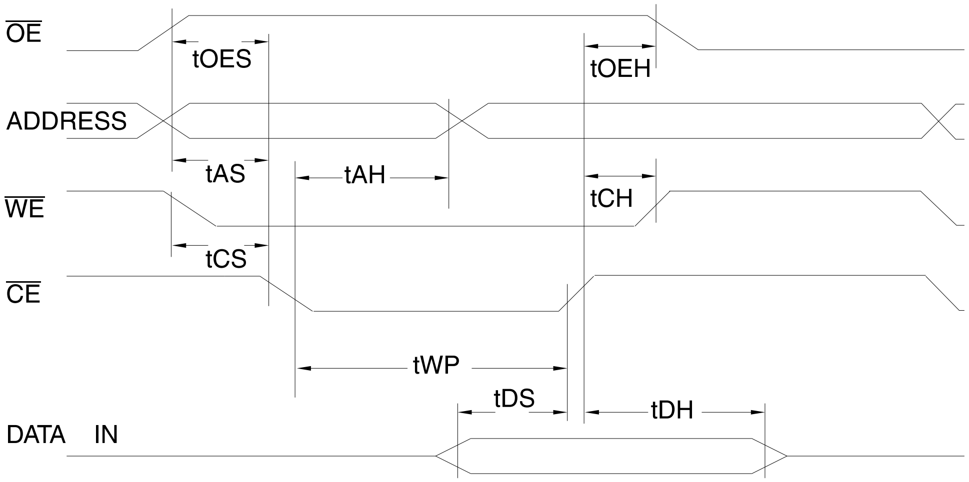
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{\text{OE}}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{\text{WE}}$ or $\overline{\text{CE}}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{\text{OE}}$ Hold Time	0		ns

AC Write Waveforms

$\overline{\text{WE}}$ Controlled



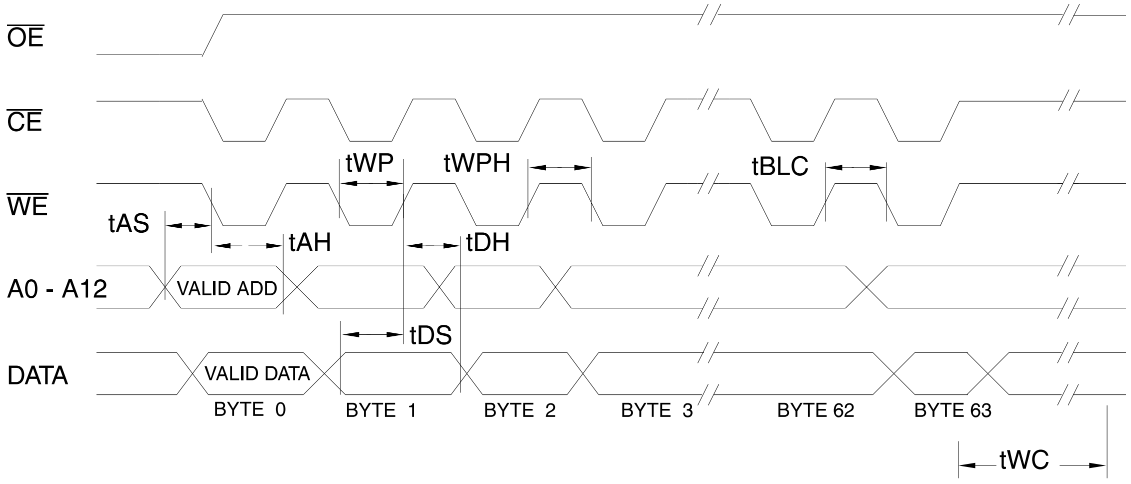
$\overline{\text{CE}}$ Controlled



Page Mode Characteristics

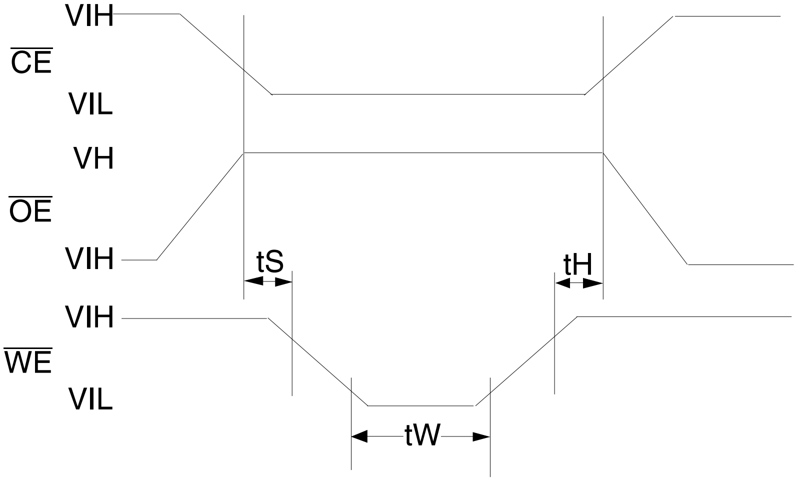
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms (1, 2)



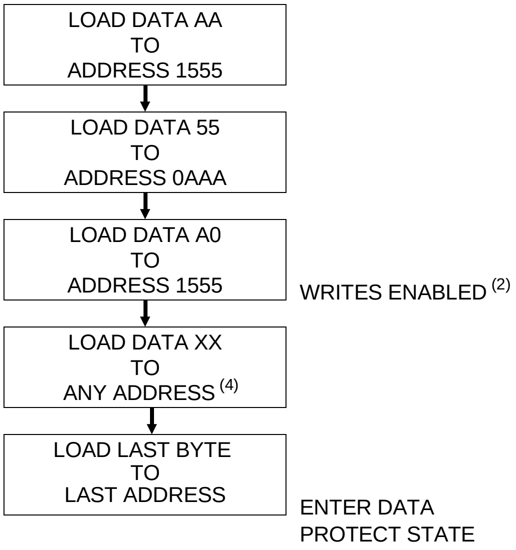
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

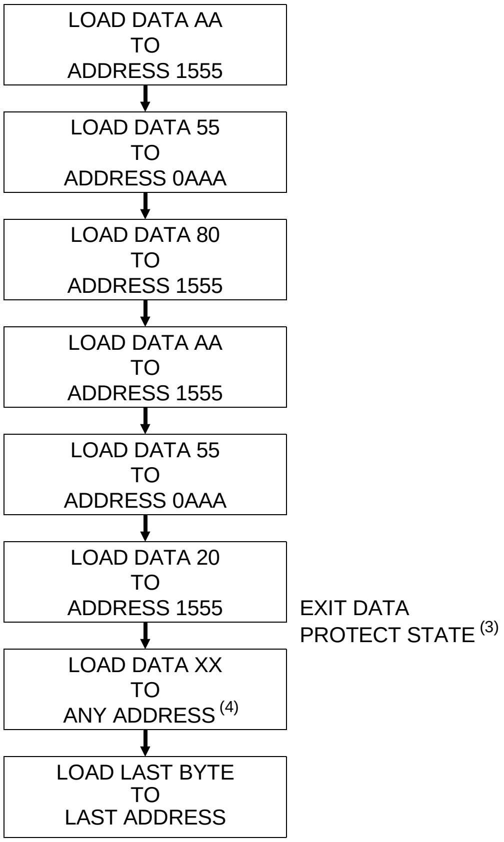


$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm (1)



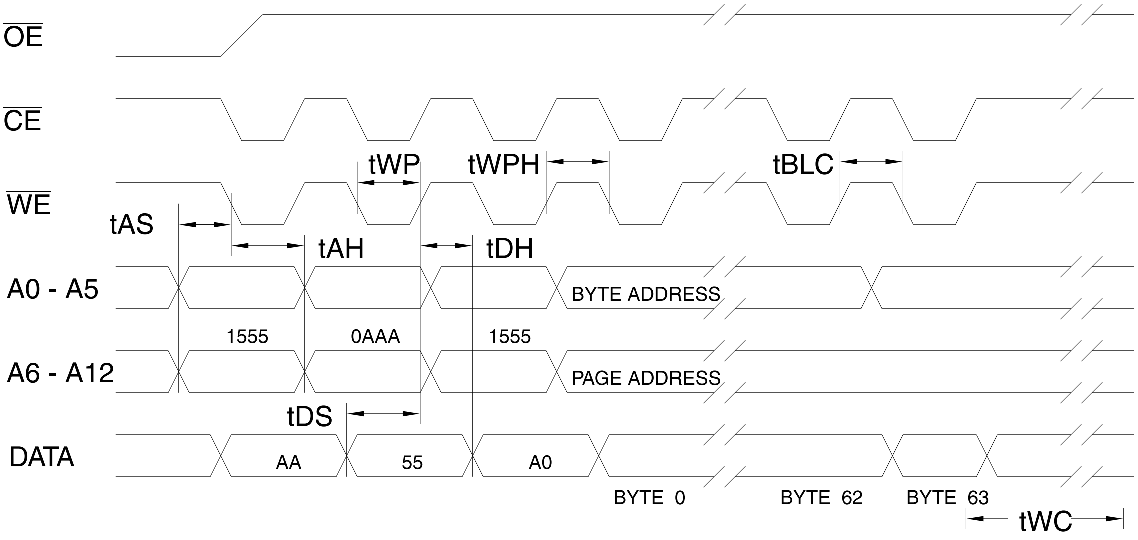
Software Data Protection Disable Algorithm (1)



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64-bytes of data are loaded.

Software Protected Write Cycle Waveforms (1, 2)



Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

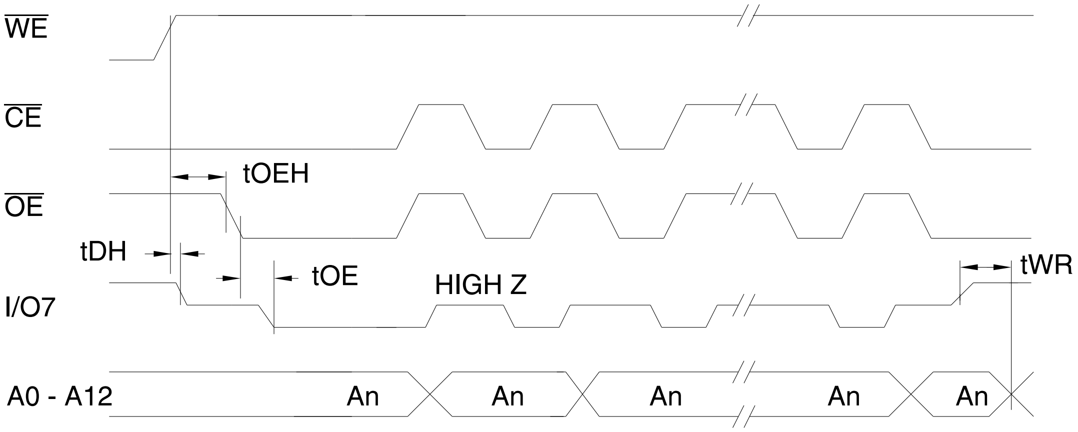
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	0			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

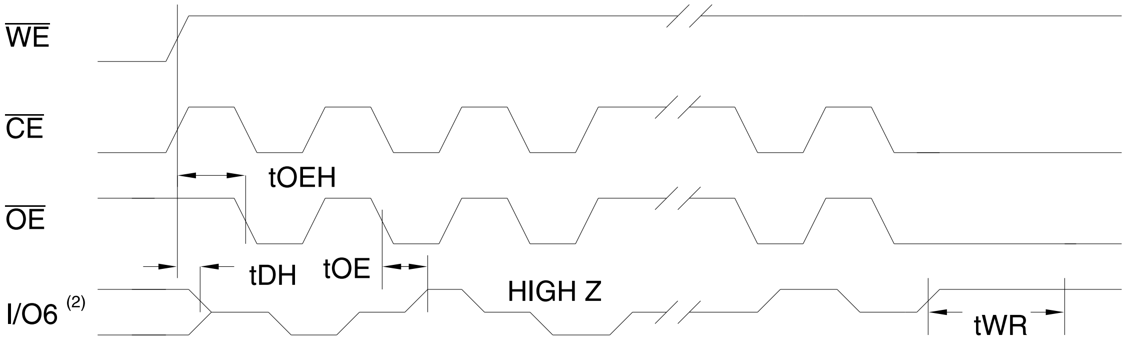


Toggle Bit Characteristics (1)

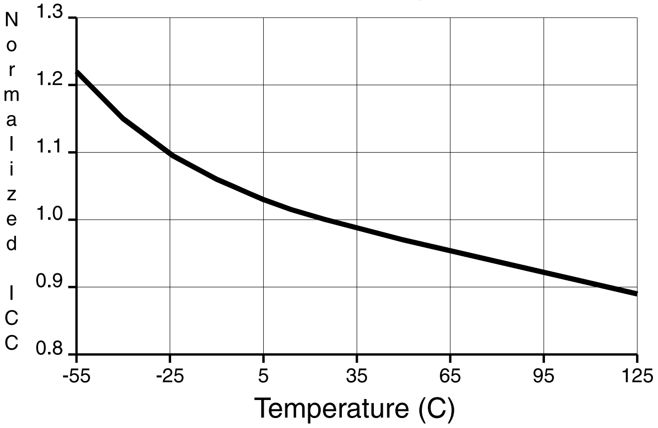
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{\text{OE}}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

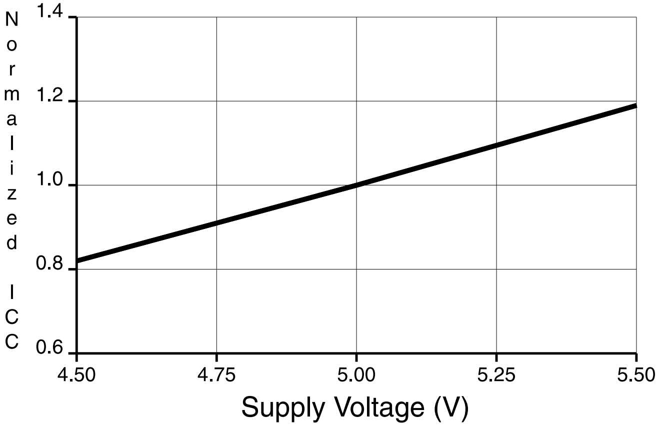
Toggle Bit Waveforms (1, 2, 3)



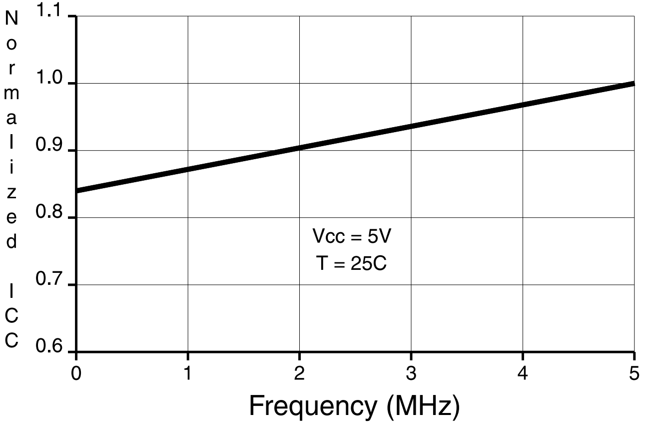
Notes:
1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used, but the address should not vary.



NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY

Ordering Information (1)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	40	0.1	AT28HC64B-55JC AT28HC64B-55PC AT28HC64B-55SC	32J 28P6 28S	Commercial (0°C to 70°C)
70	40	0.1	AT28HC64B-70JC AT28HC64B-70PC AT28HC64B-70SC AT28HC64B-70TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	40	0.1	AT28HC64B-70JI AT28HC64B-70PI AT28HC64B-70SI AT28HC64B-70TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
90	40	0.1	AT28HC64B-90JC AT28HC64B-90PC AT28HC64B-90SC AT28HC64B-90TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	40	0.1	AT28HC64B-90JI AT28HC64B-90PI AT28HC64B-90SI AT28HC64B-90TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
120	40	0.1	AT28HC64B-12JC AT28HC64B-12PC AT28HC64B-12SC AT28HC64B-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	40	0.1	AT28HC64B-12JI AT28HC64B-12PI AT28HC64B-12SI AT28HC64B-12TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28HC64B	55	PC, SC
AT28HC64B	70	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	90	JI, PC, PI, SC, SI, TC, TI
AT28HC64B	12	JI, PC, PI, SC, SI, TC, TI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)