

□ MN101D09E

Type	MN101D09E	MN101DF09G
Internal ROM type	Mask ROM	FLASH
ROM (byte)	80K	128K
RAM (byte)	2K	4K
Package (Lead-free)	QFP100-P-1818B	
Minimum Instruction Execution Time	[With main clock operated] 0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V, 14.32 MHz internal frequency di Vision) [When sub-clock operated] 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V, 14.32 MHz internal frequency di Vision) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)

■ Interrupts

RESET, Runaway, External 0 to 4, Timer 0 to 3, Timer 6, Capstan FG, Control, HSW, Cylinder(Drum) FG, Servo V-sync, Synchronous output, OSD, XDS, Serial 1, Serial 2, PWM 4, OSD V-sync

■ Timer Counter

Timer counter 0 : 8-bit × 1 (timer function)

Clock source..... 1/4, 1/16 of system clock frequency

Interrupt source overflow of timer counter 0

Timer counter 1 : 8-bit × 1 (timer function, linear timer counter function)

Clock source..... 1/4 of system clock frequency; CTL signal

Interrupt source overflow of timer counter 1

Timer counter 2 : 16-bit × 1 (timer function, input capture (CTL specified edge), duty judgment of CTL signal)

Clock source..... 1/4, 1/16, 1/24 of system clock frequency

Interrupt source overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register

Timer counter 3 : 16-bit × 1 (timer function)

Clock source..... 1/4, 1/16 of system clock frequency

Interrupt source overflow of timer counter 3

Timer counter 5 : 19-bit × 1 (watchdog, stable oscillation waiting function)

Clock source..... system clock

Watchdog interrupt source... 1/2¹⁶, 1/2¹⁹ of timer counter 5 frequency

Clear by stable oscillation ... after 256 counts by timer counter 5 (2¹⁸ counts of OSC oscillation clock)

Timer counter 6 : 16-bit × 1 (clock function [max. 2 s])

Clock source..... 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/8, 1/128 of system clock frequency

Interrupt source 1/2¹³, 1/2¹⁴, 1/2¹⁵ overflow of timer counter 6

■ Serial interface

Serial 1 : 8-bit × 1 (synchronous type)

(transfer direction of MSB/LSB selectable, start condition function)

Clock source..... 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; NSBT1 pin input

Serial 2 : 8-bit × 1 (I²C)

(master transmission/reception, slave transmission/reception)

Clock source..... 1/144 to 1/252 of system clock; SCK pin input

■ OSD

Display mode Menu(Internal synchronized) display, super impose(external synchronized) display
 Applicable broadcasting system..... NTSC, PAL, PAL-M, PAL-N
 Screen configuration 24 characters × 2n rows (n = 1 to 6)
 Character type max. 128 character types (variable, include special characters)
 Character size 12 × 18 dots (Vertical direction : 1 dot for 2H at not enlargement)
 Enlarged characters each × 2 settings in horizontal and vertical
 Character interpolation..... none
 Line background color 8-hue settable in the row unit at menu display
 Line background intensity..... 8 gradations settable in the row unit
 Screen background color..... 8-hue settable at omenu display
 Character color white
 Character intensity 8 gradations settable in the row unit
 Frame function 1-dot frame in 4 directions
 Frame intensity..... 4 gradations settable in the row unit
 Blinking..... none (covered by software)
 Inverted character..... settable in the character unit
 Halftone..... none
 Input composite video signal input (output level : 1 V[p-p] / 2 V[p-p])
 Clamp method sync tip clamp, clamp level in 4 levels
 Output composite video output
 Measure against image fluctuation..... built-in AFC circuit
 Dot clock 1/2 of OSC oscillation clock (automatic phase adjustment)

■ XDS

Built-in U.S. closed caption data slicer (optional 1 line data can be extracted.)

■ I/O Pins

I/O	56	Common use : 45
Input	1	Common use : 1

■ A/D converter

8-bit × 11-ch. (without S/H)

■ PWM

13-bit × 2-ch. (at repetition cycle 572 ms at 14.32 MHz),

8-bit × 1-ch. (at repetition cycle 71.5 ms, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)

■ ICR

16-bit × 2-ch.(Speed system),

18-bit × 4-ch.(Phase system)

■ OCR

16-bit × 3 (Synchronous output × 2, Rec CTL × 1)

■ Special Ports

3-state output (PTO) VLP pin; CTL input; Capstan FG input; Cylinder(Drum) PG/FG inputs; HSW output; Head amp/ Rotary control outputs; output of 1/4 OSC oscillation clock (1 V[p-p])

■ ROM Correction

Correcting address designation : up to 3 addresses possible

Correction method : correction program being saved in internal RAM

■ Electrical Characteristics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		50	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

(Ta = 25°C±2°C, VSS = 0 V)

■ Electrical Characteristics (A/D converter characteristics)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				±3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

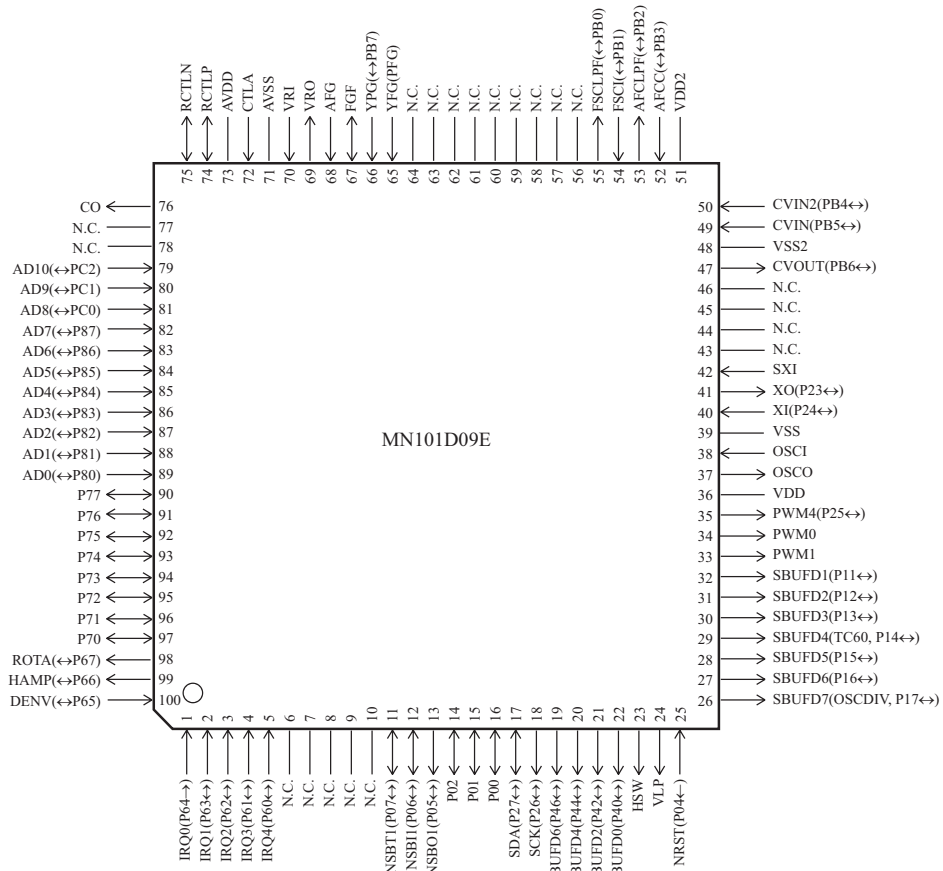
(Ta = 25°C±2°C, VDD = 5.0 V, VSS = 0 V)

■ Development tools

In-circuit Emulator

PX-ICE101C/D + PX-PRB101D08-QFP100-P-1818B-M

■ Pin Assignment



QFP100-P-1818B

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