☐ MN101D06F , MN101D06G , MN101D06H

Type	MN101D06F	MN101D06G	MN101D06H
ROM (×8-bit)	96 K	128 K	160 K
RAM (×8-bit)	3 K	4 K	5 K
Package	QFP100-P-1818B *Lead-free		

Minimum Instruction Execution Time	With main clock operated	0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)
		71.5 µs (at 3.0 V to 5.5 V fixed to 14.32 MHz internal frequency division)
	When sub-clock operated	61 µs (at 2.2 V to 5.5 V, 32.768 kHz)

Interrupts
- RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4 • key input (P50 to 54)
- Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW
- Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2
- A/D (common with PWM 4 reference frequency) • OSD V-sync

Timer Counter

Timer counter 0: 16-bit × 1
(timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6])
    Clock source ···················· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; overflow of timer counter 6;
                                                 1/512 of XI oscillation clock or OSC oscillation clock frequency
    Interrupt source ··············· overflow of timer counter 0

Timer counter 1: 16-bit × 1 (timer function, linear timer counter function)
    Clock source ···················· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; CTL signal
    Interrupt source ··············· overflow of timer counter 1

Timer counter 2: 16-bit × 1 (timer function, input capture, duty judgment of CTL signal(VISS/VASS detection function))
    Clock source ···················· 1/2, (1/4,) 1/8, (1/16,) 1/12, (1/24) of system clock frequency
    Interrupt source ··············· overflow of timer counter 2; input of CTL specified edge; underflow of timer 2
                                                 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2
                                                 shift register compare register

Timer counter 3: 16-bit × 1
(timer function, detection of serial indexing, generation of remote control output carrier frequency)
    Clock source ···················· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; XI oscillation clock
    Interrupt source ··············· overflow of timer counter 3

Timer counter 4: 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock)
    Clock source ···················· 1/8, (1/16) of system clock frequency; external clock input
    Interrupt source ··············· overflow of timer counter 4; coincidence of timer counter 4 with OCR4

Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)
    Clock source ···················· system clock
    Watchdog interrupt source ·· $1/2^{16}$, $1/2^{19}$ of timer counter 5 frequency
    Clear by stable oscillation ·· after 256 counts by timer counter 5 (2^{18} counts of OSC oscillation clock)

Timer counter 6: 16-bit × 1 (clock function [max. 2 s])
    Clock source ···················· 1/512 of OSC oscillation clock frequency; XI oscillation clock;
                                                   1/4, (1/8,) 1/64, (1/128) of system clock frequency
    Interrupt source ··············· $1/2^{13}$, $1/2^{14}$, $1/2^{15}$ overflow of timer counter 6

Timer counter 7: 8-bit × 1 or 4-bit × 2 (timer function, event count)
    Clock source ···················· 1/4, (1/8,) 1/16, (1/32) of system clock frequency; external clock input
    Interrupt source ··············· overflow of timer counter 7 (although when 4-bit × 2, there is one interrupt vector.)

Serial Interface

Serial 0: 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable)
    Synchronous type clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency;
                                                   2-division timer 4 output; NSBT0 pin input
    Clock for UART ············· 8-division of above clock; 2-division timer 4 output; NSBT0 pin input

■ **Serial Interface (Continue)**

Serial 1: 8-bit × 1

(synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function)

    Clock source ···················· 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency;

                                   2-division timer 4 output; NSBT1 pin input

    Remote control clock ····· 2-division timer 4 output

Serial 2: 8-bit × 1 (I^2C) (master transmission/reception, slave transmission/reception)

    Clock source ···················· 1/144 to 1/252 of system clock; SCK pin input

■ **OSD**

OSD mode: Accommodation with menu(internal synchronous) or super impose(external synchronous) display

    Applicable broadcasting system:NTSC, PAL, PAL-M, PAL-N

Screen configuration	: 24 characters × 2n rows (n = 1 to 6)
Character type	: max. 512 character types (variable, incude special characters)
Character size	: 12 × 18 dots (Vertical direction: 1 dot for 2H at not enlargement)
Enlarged characters	: each × 2, × 3 or × 4 settings in horizontal and vertical
Character interpolation	: none
Line background color	: 8-hue settable (settable in the row unit at menu display)
Line background intensity	: 8 gradations settable in the row unit (at output of composite video signal)
Screen background color	: 8-hue settable (at output of composite video signal)
Character color	: white (at output of composite video signal)
Character intensity	: 8 gradations settable in the row unit (at output of composite video signal)
Frame function	: 1-dot frame in 4 or 8 directions
Frame intensity	: 4 gradations settable in the row unit (at output of composite video signal)
Box shade function	: settable in the character unit (at output of composite video signal with 129 or more characters (character types))
Blinking	: none (covered by software)
Inverted character	: settable in the character unit
Halftone	: settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)

CCD mode: Supports Closed Caption in the U.S.A.

Screen configuration	: 32 characters × 16 rows
Character type	: max. 128 character types (variable)
Character size	: 12 × 26 dots (Vertical direction: 1 dot for 1H, including 8 dots in the underlined area)
Enlarged characters	: none
Character interpolation	: none
Line background color	: 8-hue settable
Line background intensity	: 8 gradations settable in the screen unit (at output of composite video signal)
Screen background color	: 8-hue settable (at output of composite video signal)
Character color	: 8 colors (at RGB output)
	: White (at output of composite video signal)
Character intensity	: 8 gradations settable in the screen unit (at output of composite video signal)
Frame function	: none
Box shade function	: none
Inverted character	: none
Halftone	: settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)
Others	: Underline, italic, blinking function and scroll
Input	: composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
Clamp method	: sync tip clamp, clamp level in 4 levels
Output	: composite video output
	: digital output (6 pins)
Measure against image fluctuation	: built-in AFC circuit
Dot clock	: 1/2 of OSC oscillation clock (automatic phase adjustment)

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■ **XDS**		Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)	
■ **ROM Correction**		Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM	
■ **I/O Pins**	**I/O**	75	• Common use: 66
	Input	2	• Common use: 2
■ **A/D Inputs**		8-bit × 13-ch. (without S/H)	
■ **PWM**		13-bit × 2-ch. (at repetition cycle 572 µs at 14.32 MHz), 10-bit × 2-ch. (at repetition cycle 71.5 µs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 71.5 µs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)	
■ **ICR**		18-bit × 6-ch.	
■ **OCR**		16-bit × 2 (8-bit synchronous output; 4-bit 3-state synchronous output), 16-bit × 1 (weak electric field V-sync backup), 16-bit × 1 (Rec CTL)	
■ **Special Ports**		Buzzer output; 3-state output VLP pin; remote control receive; CTL signal input terminal; Capstan FG inputterminal; Sylinder(Durm) PG/FG input terminals; HSW output terminal; Head Amp/Rortary control output terminals; output of 1/2 OSC oscillation clock (2 V[p-p]); output of 1/4 OSC oscillation clock (1 V[p-p])	

■ **Electrical Characteristics**

Supply current

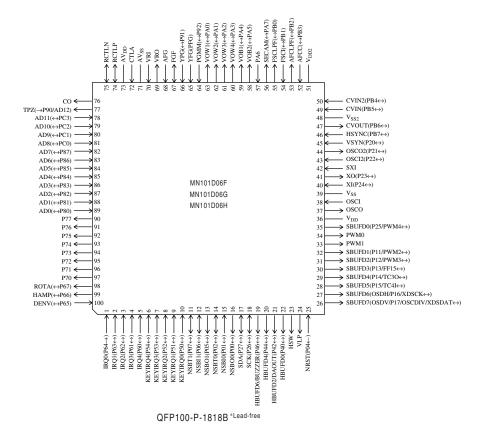| Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 3.0 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	µA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V, Ta = 55 °C			10	µA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	µ A

(Ta = 25 °C ± 2 °C , VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		µ s
Analog Input Voltage					5	V

(Ta = 25 °C ± 2 °C , VDD = 5.0 V , VSS = 0 V)

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Pin Assignment

Top pins (75 → 51):
- 75 RCTLN
- 74 RCTLP
- 73 AV$_{DD}$
- 72 CTLA
- 71 AV$_{SS}$
- 70 VRI
- 69 VRO
- 68 AFG
- 67 FGF
- 66 YPG(↔P91)
- 65 YPFG(PFG)
- 64 PGMM(↔P92)
- 63 VOW1(↔PA0)
- 62 VOW2(↔PA1)
- 61 VOW3(↔PA2)
- 60 VOW4(↔PA3)
- 59 VOB1(↔PA4)
- 58 VOB2(↔PA5)
- 57 PA6
- 56 SECAM(↔PA7)
- 55 FSCLPF(↔PB0)
- 54 FSCI(↔PB1)
- 53 AFCLPF(↔PB2)
- 52 AFCC(↔PB3)
- 51 V$_{DD2}$

Left side (76 → 100):
- 76 CO
- 77 TPZ(→P90/AD12)
- 78 AD11(↔PC3)
- 79 AD10(↔PC2)
- 80 AD9(↔PC1)
- 81 AD8(↔PC0)
- 82 AD7(↔P87)
- 83 AD6(↔P86)
- 84 AD5(↔P85)
- 85 AD4(↔P84)
- 86 AD3(↔P83)
- 87 AD2(↔P82)
- 88 AD1(↔P81)
- 89 AD0(↔P80)
- 90 P77
- 91 P76
- 92 P75
- 93 P74
- 94 P73
- 95 P72
- 96 P71
- 97 P70
- 98 ROTA(↔P67)
- 99 HAMP(↔P66)
- 100 DENV(↔P65)

Center:
MN101D06F
MN101D06G
MN101D06H

Right side (50 → 26):
- 50 CVIN2(PB4↔)
- 49 CVIN(PB5↔)
- 48 V$_{SS2}$
- 47 CVOUT(PB6↔)
- 46 HSYNC(PB7↔)
- 45 VSYN(P20↔)
- 44 OSCO2(P21↔)
- 43 OSCI2(P22↔)
- 42 SXI
- 41 XO(P23↔)
- 40 XI(P24↔)
- 39 V$_{SS}$
- 38 OSCI
- 37 OSCO
- 36 V$_{DD}$
- 35 SBUFD0(P25/PWM4↔)
- 34 PWM0
- 33 PWM1
- 32 SBUFD1(P11/PWM2↔)
- 31 SBUFD2(P12/PWM3↔)
- 30 SBUFD3(P13/FF15↔)
- 29 SBUFD4(P14/TC3O↔)
- 28 SBUFD5(P15/TC4I↔)
- 27 SBUFD6(OSDH/P16/XDSCK↔)
- 26 SBUFD7(OSDV/P17/OSCDIV/XDSDAT↔)

Bottom pins (1 → 25):
- 1 IRQ0(P64→)
- 2 IRQ1(P63↔)
- 3 IRQ2(P62↔)
- 4 IRQ3(P61↔)
- 5 IRQ4(P60↔)
- 6 KEYIRQ4(P54↔)
- 7 KEYIRQ3(P53↔)
- 8 KEYIRQ2(P52↔)
- 9 KEYIRQ1(P51↔)
- 10 KEYIRQ0(P50↔)
- 11 NSBT1(P07↔)
- 12 NSBI1(P06↔)
- 13 NSBO1(P05↔)
- 14 NSBT0(P02↔)
- 15 NSBI0(P01↔)
- 16 NSBO0(P00↔)
- 17 SDA(P27↔)
- 18 SCK(P26↔)
- 19 HBUFD6/BUZZER(P46↔)
- 20 HBUFD4(P44↔)
- 21 HBUFD2/DAOUT(P42↔)
- 22 HBUFD0(P40↔)
- 23 HSW
- 24 VLP
- 25 NRST(P04↔)

QFP100-P-1818B *Lead-free

Support Tool

In-circuit Emulator	PX-ICE101C / D + PX-PRB101D06-QFP100-P-1818B-M	
Flash Memory Built-in Type	Type	MN101DF06ZAF
	ROM (× 8-bit)	224 K
	RAM (× 8-bit)	6 K
	Minimum instruction execution time	0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)
		71.5 µs (at 3.0 V to 5.5 V, fixed to 14.32 MHz internal division)
		61 µs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	QFP100-P-1818B *Lead-free

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