

□ MN101C93 Series

Type	MN101C93K	MN101CF93K
Internal ROM type	Mask ROM	FLASH
ROM (byte)	224K	
RAM (byte)	6K	
Package (Lead-free)	LQFP100-P-1414	
Minimum Instruction Execution Time	0.125 μ s (at 3.0 V to 3.6 V, 8 MHz) 62.5 μ s (at 3.0 V to 3.6 V, 32 kHz)	0.167 μ s (at 3.0 V to 3.6 V, 6 MHz) 62.5 μ s (at 3.0 V to 3.6 V, 32 kHz)

■ Interrupts

RESET. Watchdog. External 0 to 5. External 6 (key interrupt dedicated). Timer 0 to 3. Timer 6. Timer 7 (2 systems). Timer 8 (2 systems). Time base. Serial 0 (2 systems). Serial 1 (2 systems). Serial 3 (1 systems). A/D conversion finish. Automatic transfer finish. USB interrupts

■ Timer Counter

8-bit timer \times 5

Timer 0Square-wave/8-bit PWM output. Event count. Remote control carrier output. Simple pulse width measurement. Added pulse (2-bit) type PWM output. Square-wave/PWM output to large current terminal PC3 possible

Timer 1Square-wave output. Event count. Serial transfer clock output. Synchronous output event

Timer 2Square-wave output. Added pulse (2-bit) type PWM output. PWM output. Serial transfer clock output. Event count. Synchronous output event. Simple pulse width measurement. Square-wave/PWM output to large current terminal PC5 possible

Timer 3Square-wave output. Event count. Serial transfer clock output

Timer 68-bit freerun timer

Timer 0, 1 can be cascade-connected

Timer 2, 3 can be cascade-connected

16-bit timer \times 2

Timer 7Square-wave output. 16-bit PWM output (cycle/duty continuous variable). Event count. Synchronous output event. Pulse width measurement. Input capture. Real time output control. High performance IGBT output. Square-wave/PWM output to large current terminal PC4 possible

Timer 8Square-wave/16-bit PWM output (duty continuous variable). Event count. Pulse width measurement. Input capture. Square-wave/PWM output to large current terminal PC6 possible

Timer 7, 8 can be cascade-connected: Square-wave output, PWM is possible as a 32-bit timer

Time base timer: One-minute count setting

Watchdog timer \times 1

■ Serial interface

Synchronous type/UART (full-duplex) \times 2: Serial 0, 1

Synchronous type/Single-master I²C \times 1: Serial 3

■ DMA controller

Maximum transfer cycles: 255

Starting factor: External request. Various types of interrupt. Software

Transfer mode: 1-byte transfer. Word transfer. Burst transfer

■ USB Functions

Conforms to USB 1.1: Full-speed (12 Mbps) supported

USB transceiver built-in. 5 end points (FIFO built-in independently)

FIFO size: EP0 = 16 bytes. EP1 = 128 bytes. EP2 = 128 bytes. EP3 = 64 bytes. EP4 = 64 bytes

EP0: Control transfer. IN/OUT (two ways)

EP1 to EP4: Interrupt/Bulk/Isochronous transfer supported. Settable to IN or OUT. Double Buffering function supported

When the MAXP size is set to a half or less of the MAXFIFO size for each EP, the Double Buffering function is made valid automatically

■ I/O Pins

I/O 84: Common use. Specified pull-up resistor available. Input/output selectable (bit unit)

■ A/D converter

10-bit \times 12 channels (with S/H)

■ Display control function

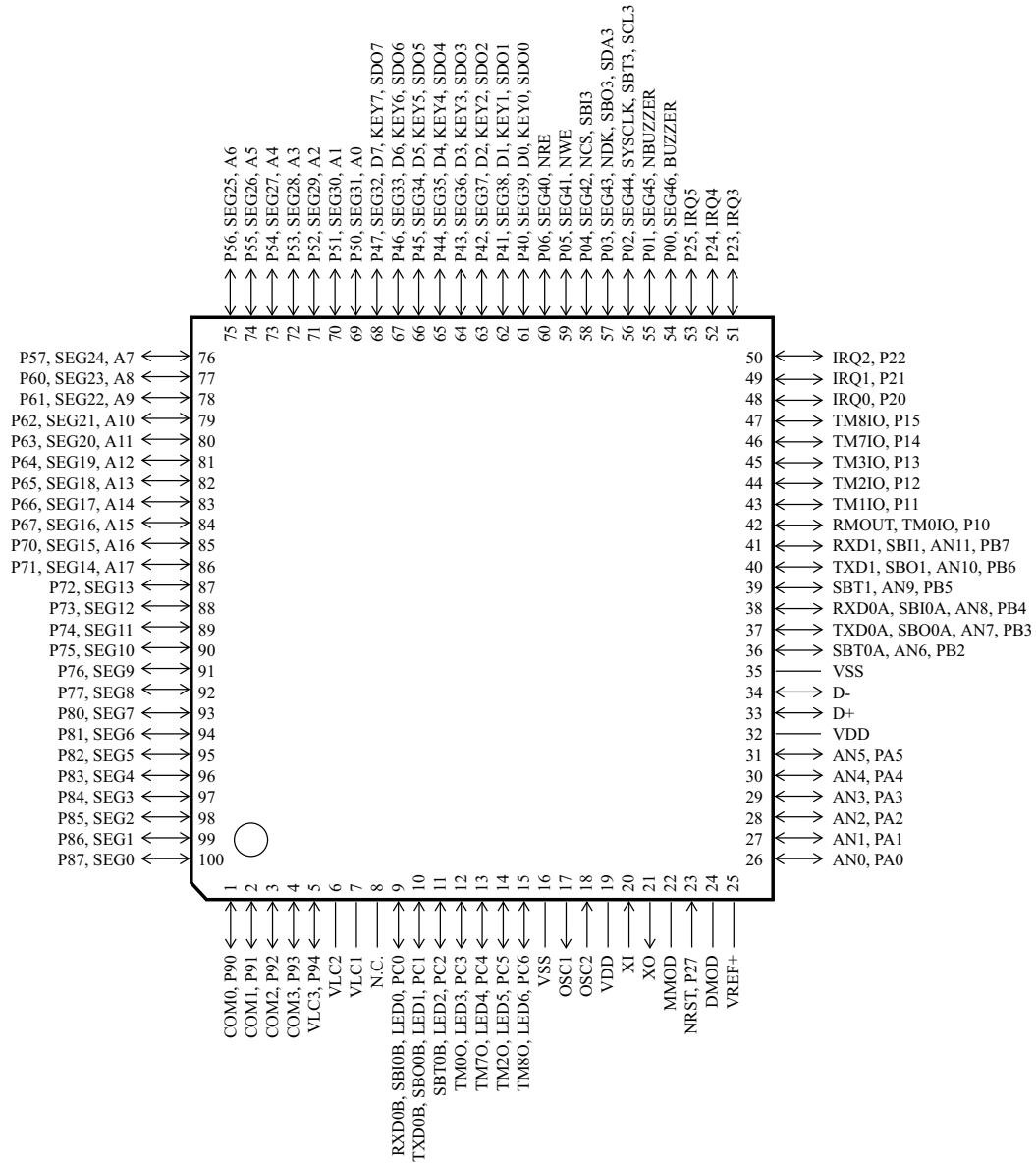
- LCD: 47 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty)
- LCD power supply separated from VDD (usable if $VDD = VLCD \leq 3.6\text{ V}$)
- LCD power shunt resistance contained

■ Special Ports

- USB ports (D+, D-). Buzzer output. Inverted buzzer output. Remote control carrier output. High-current drive port. Clock output

■ Pin Assignment

LQFP100-P-1414



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