MN101C70C

Туре	MN101C70C	MN101CF70D		
Internal ROM type	Mask ROM	FLASH		
ROM (byte)	48K	64K		
RAM (byte)	2K	4K		
Package (Lead-free)	LQFP080-P-1414A, TQFP080-P-1212D (Under planning)	LQFP080-P-1414A (Under development), TQFP080-P-1212D (Under planning)		
		0.25 μs (at 3.0 V to 3.6 V, 8 MHz) 0.50 μs (at 2.28 V to 3.6 V, 4 MHz) 62.5 μs (at 2.2 V to 3.6 V, 32 kHz)		

Interrupts

RESET, Watchdog, External 0 to 2, External 4 (key interrupt dedicated), Timer 0 to 3, Timer 6, Timer 7 (2 systems), Timer 8 (2 systems), Time base, Serial 0 (2 systems), Serial 2, A/D conversion finish, Automatic transfer finish

■ Timer Counter

Timer counter 0 : 8-bit \times 1

(square-wave/8-bit PWM output, event count, generation of remote control carrier, simple pulse width measurement, added pluse

(2-bit) system PWM output, real time output control)

(square-wave/PWM output to large current terminal P50 possible)

Interrupt source coincidence with compare register 0

Timer counter 1:8-bit \times 1

(square-wave output, event count, synchronous output event, serial transfer clock output)

Interrupt source coincidence with compare register 1

Timer counter 0, 1 can be cascade-connected.

Timer counter 2 : 8-bit \times 1

(square-wave output, added pluse (2-bit) system PWM output, PWM output, serial transfer clock output, real time output control, event count, synchronous output event, simple pulse width measurement)

(square-wave/PWM output to large current terminal P52 possible)

Interrupt source coincidence with compare register 2

Timer counter 3:8-bit \times 1

(square-wave output, event count, generation of remote control carrier, serial transfer clock)

Interrupt source coincidence with compare register 3

Timer counter 2, 3 can be cascade-connected.

Timer counter 6 : 8-bit freerun timer

Interrupt source coincidence with compare register 6

Timer counter 7: 16-bit × 1

(square-wave output, 16-bit PWM output (cycle / duty continuous variable), event count, synchronous output event, pulse width measurement, input capture, real time output control, high performance IGBT output (Cycle/Duty can be changed constantly))

(square-wave/PWM output to large current terminal P51 possible)

 $Clock\ source......1/1,\ 1/2,\ 1/4,\ 1/16\ of\ system\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\$

1/2, 1/4, 1/16 of external clock input frequency

Interrupt source coincidence with compare register 7 (2 lines), input capture register

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Timer counter 8: 16 bit × 1

(square-wave/16-bit PWM output [duty continuous variable], event count, pulse width measurement, input capture)(square-wave/PWM output to large current terminal P53 possible)

 $Clock\ source......1/1,\ 1/2,\ 1/4,\ 1/16\ of\ system\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2,\ 1/2,\ 1/4,\ 1/16\ of\ OSC\ oscillation\ clock\ frequency;\ 1/1,\ 1/2$

1/2, 1/4, 1/16 of external clock input frequency

Interrupt source coincidence with compare register 8 (2 lines), input capture register

Timer counters 7, 8 can be cascade-connected. (square-wave output, PWM is possible as a 32-bit timer.)

Time base timer (one-minute count setting)

Watchdog timer

Interrupt source 1/65536, 1/262144, 1/1048576 of system clock frequency

■ Serial interface

Serial 0 : synchronous type/UART (full-duplex) × 1

Serial 2 : synchronous type/single-master I²C × 1

■ DMA controller

Max. Transfer cycles: 255

Starting factor: external request, various types of interrupt, software Transfer mode: 1-byte transfer, word transfer, burst transfer

■ I/O Pins

I/O	66	Common use, Specified pull-up resistor available, Input/output selectable (bit unit)
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■ A/D converter

10-bit \times 16-ch. (with S/H)

■ Display control function

LCD

32 segments \times 4 commons (static, 1/2, 1/3, or 1/4 duty)

LCD power supply separated from VDD (usable if VDD \leq VLCD \leq 3.6 V)

LCD power step-up circuit contained (3/2, 2 and 3 times)

LCD power shunt resistance contained

LCD reference voltage is contained.

Special Ports

Buzzer output, remote control carrier signal output, high-current drive port

■ ROM Correction

Correcting address designation : up to 3 addresses possible

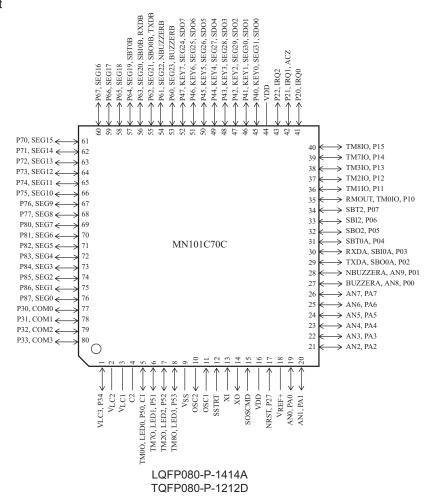
■ Electrical Charactreistics (Supply current)

Parameter	Symbol	Condition		Limit		
Parameter				typ	max	Unit
Operating supply current	IDD1	fosc = 4 MHz, VDD = 3 V		1	1.8	mA
	IDD2	fx = 32 kHz, $VDD = 3 V$		4	15	μΑ
Supply current at HALT	IDD3	$fx = 32 \text{ kHz}$, $VDD = 3 \text{ V}$, $Ta = 25^{\circ}\text{C}$		2	5	μΑ
	IDD4	$fx = 32 \text{ kHz}$, $VDD = 3 \text{ V}$, $Ta = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			10	μΑ
Supply current at STOP	IDD5	VDD = 3 V , Ta = 25°C			2	μΑ
Supply current at STOP	IDD6	VDD = 3 V, $Ta = -40$ °C to $+85$ °C			8	μΑ

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■ Development tools In-circuit Emulator PX-ICE101C/D+PX-PRB101C70-LQFP080-P-1414A-M PX-ICE101C/D+PX-PRB101C70-TQFP080-P-1212-M

■ Pin Assignment



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