



MICROCHIP

# 93C56A/B

## 2K 5.0V Automotive Temperature Microwire® Serial EEPROM

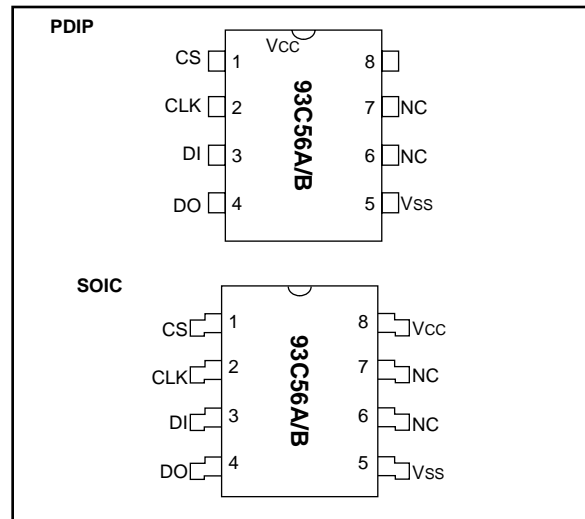
### FEATURES

- Single supply 5.0V operation
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1  $\mu$ A standby current (maximum)
- 256 x 8 bit organization (93C56A)
- 128 x 16 bit organization (93C56B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 100,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Available for the following temperature ranges:
  - Automotive (E): -40°C to +125°C

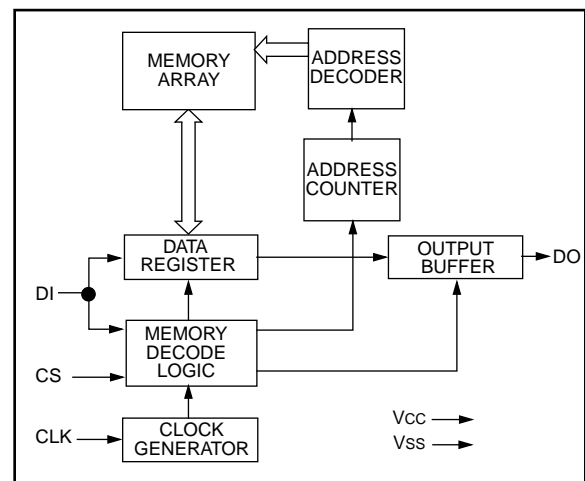
### DESCRIPTION

The Microchip Technology Inc. 93C56A/B is a 2K-bit, low-voltage serial Electrically Erasable PROM. The device memory is configured as 256 x 8 bits (93C56A) or 128 x 16 bits (93C56B). Advanced CMOS technology makes this device ideal for low-power, nonvolatile memory applications. The 93C56A/B is available in standard 8-pin DIP and surface mount SOIC packages. **This device is only recommended for 5V automotive temperature applications. For all commercial and industrial applications, the 93LC56A/B is recommended.**

### PACKAGE TYPE



### BLOCK DIAGRAM



Microwire is a registered trademark of National Semiconductor.

# 93C56A/B

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

V<sub>CC</sub> .....7.0V  
 All inputs and outputs w.r.t. V<sub>SS</sub> ..... -0.6V to V<sub>CC</sub> +1.0V  
 Storage temperature .....-65°C to +150°C  
 Ambient temp. with power applied.....-65°C to +125°C  
 Soldering temperature of leads (10 seconds) .....+300°C  
 ESD protection on all pins..... 4 kV

\***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V <sub>SS</sub>	Ground
NC	No Connect
V <sub>CC</sub>	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted		Automotive (E)V <sub>CC</sub> = +4.5V to +5.5V T <sub>amb</sub> = -40°C to +125°C				
Parameter	Symbol	Min.	Max.	Units	Conditions	
High level input voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> +1	V	(Note 2)	
Low level input voltage	V <sub>IL</sub>	-0.3	0.8	V		
Low level output voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 2.1 mA; V <sub>CC</sub> = 4.5V	
High level output voltage	V <sub>OH</sub>	2.4	—	V	I <sub>OH</sub> = -400 μA; V <sub>CC</sub> = 4.5V	
Input leakage current	I <sub>LI</sub>	-10	10	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	-10	10	μA	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Pin capacitance (all inputs/outputs)	C <sub>IN</sub> , C <sub>OUT</sub>	—	7	pF	V <sub>IN</sub> /V <sub>OUT</sub> = 0 V (Notes 1 & 2) T <sub>amb</sub> = +25°C, F <sub>CLK</sub> = 1 MHz	
Operating current	I <sub>CC</sub> write	—	1.5	mA		
	I <sub>CC</sub> read	—	1	mA		
Standby current	I <sub>CCS</sub>	—	1	μA	CS = V <sub>SS</sub>	
Clock frequency	F <sub>CLK</sub>	—	2	MHz		
Clock high time	T <sub>CKH</sub>	250	—	ns		
Clock low time	T <sub>CKL</sub>	250	—	ns		
Chip select setup time	T <sub>CSS</sub>	50	—	ns	Relative to CLK	
Chip select hold time	T <sub>CSH</sub>	0	—	ns	Relative to CLK	
Chip select low time	T <sub>CSL</sub>	250	—	ns		
Data input setup time	T <sub>DIS</sub>	100	—	ns	Relative to CLK	
Data input hold time	T <sub>DIH</sub>	100	—	ns	Relative to CLK	
Data output delay time	T <sub>PD</sub>	—	400	ns	C <sub>L</sub> = 100 pF	
Data output disable time	T <sub>CZ</sub>	—	100	ns	C <sub>L</sub> = 100 pF (Note 2)	
Status valid time	T <sub>SV</sub>	—	500	ns	C <sub>L</sub> = 100 pF	
Program cycle time	T <sub>WC</sub>	—	2	ms	ERASE/WRITE mode	
	T <sub>EC</sub>	—	6	ms	ERAL mode	
	T <sub>WL</sub>	—	15	ms	WRAL mode	
Endurance	—	100K	—	cycles	25°C, V <sub>CC</sub> = 5.0V, Block Mode (Note 3)	

**Note 1:** This parameter is tested at T<sub>amb</sub> = 25°C and F<sub>CLK</sub> = 1 MHz.

**2:** This parameter is periodically sampled and not 100% tested.

**3:** This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on Microchip's BBS or website.

## 2.0 PIN DESCRIPTION

### 2.1 Chip Select (CS)

A high level selects the device. A low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the CS input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T<sub>CSL</sub>) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

### 2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C56A/B. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T<sub>CKH</sub>) and clock low time (T<sub>CKL</sub>). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but the START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detecting a START condition, the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

**Note:** CS must go low between consecutive instructions.

### 2.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

### 2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T<sub>PD</sub> after the positive edge of CLK).

This pin also provides READY/ $\overline{\text{BUSY}}$  status information during ERASE and WRITE cycles. READY/BUSY status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (T<sub>CSL</sub>) and an ERASE or WRITE operation has been initiated. The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

**TABLE 2-1: INSTRUCTION SET FOR 93C56A**

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/ $\overline{\text{BSY}}$ )	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/ $\overline{\text{BSY}}$ )	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	X	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	X	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/ $\overline{\text{BSY}}$ )	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/ $\overline{\text{BSY}}$ )	20

**TABLE 2-2: INSTRUCTION SET FOR 93C56B**

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A6	A5	A4	A3	A2	A1	A0	—	(RDY/ $\overline{\text{BSY}}$ )	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/ $\overline{\text{BSY}}$ )	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	X	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	X	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/ $\overline{\text{BSY}}$ )	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/ $\overline{\text{BSY}}$ )	27

## 3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/ $\overline{\text{BUSY}}$  status during a programming operation. The READY/ $\overline{\text{BUSY}}$  status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

### 3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

## 3.2 Data IN (DI) and Data Out (DO)

It is possible to connect the Data In (DI) and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition, the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

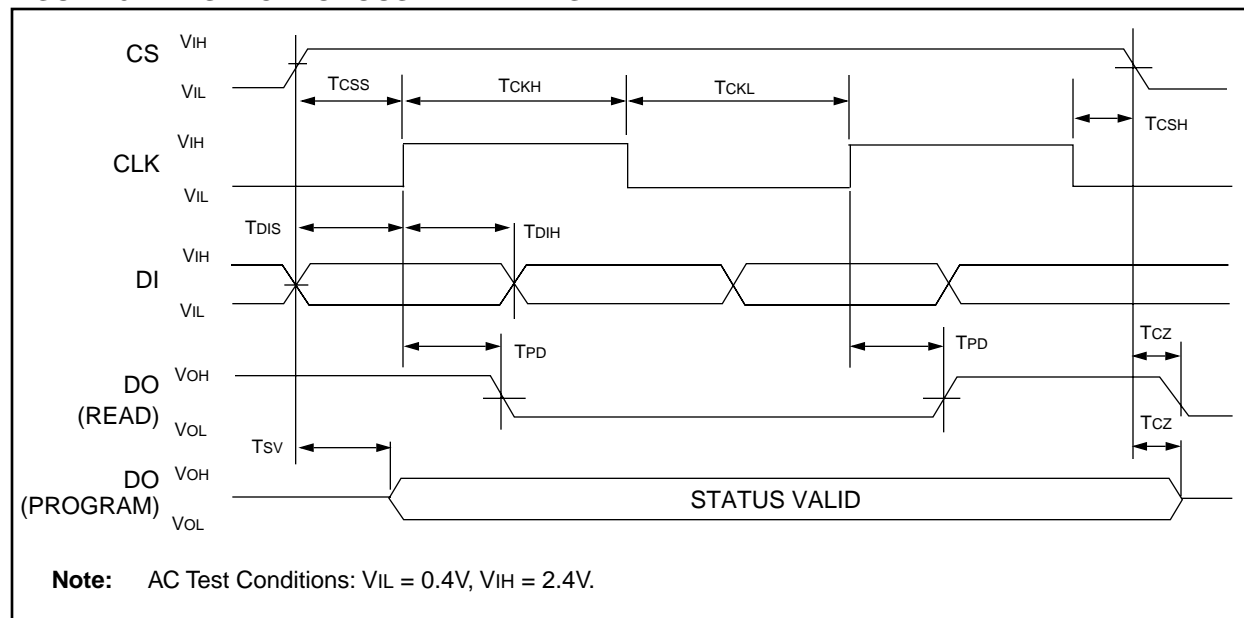
### 3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 3.8V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 3.8V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE WRTE Enable (EWEN) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

**FIGURE 3-1: SYNCHRONOUS DATA TIMING**



## 3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. This cycle begins on the rising clock edge of the last address bit.

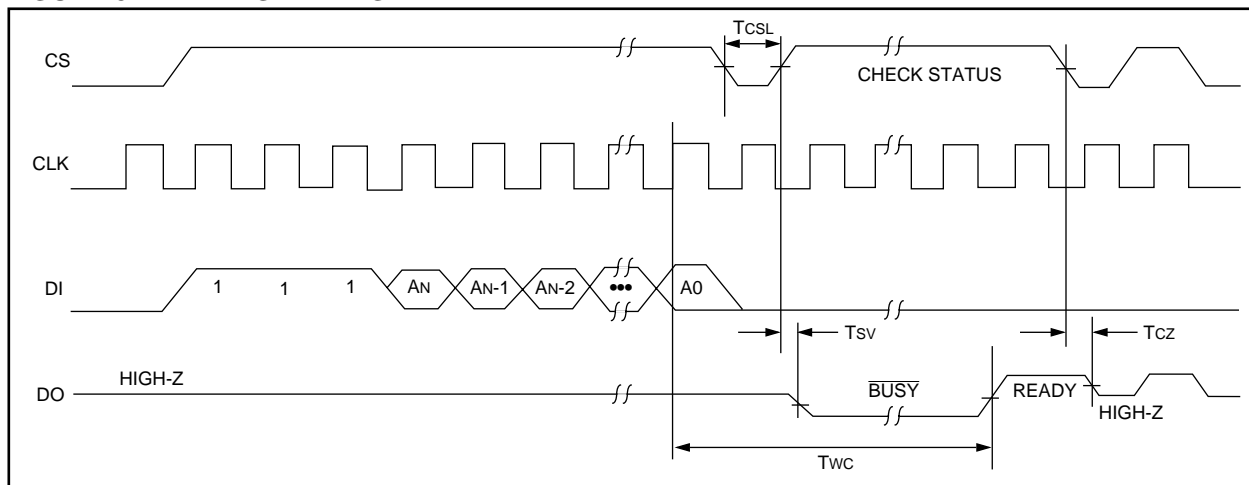
The DO pin indicates the READY/ $\overline{\text{BUSY}}$  status of the device if CS is brought high after a minimum of 250 ns low ( $T_{\text{CSL}}$ ). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

## 3.5 Erase All (ERAL)

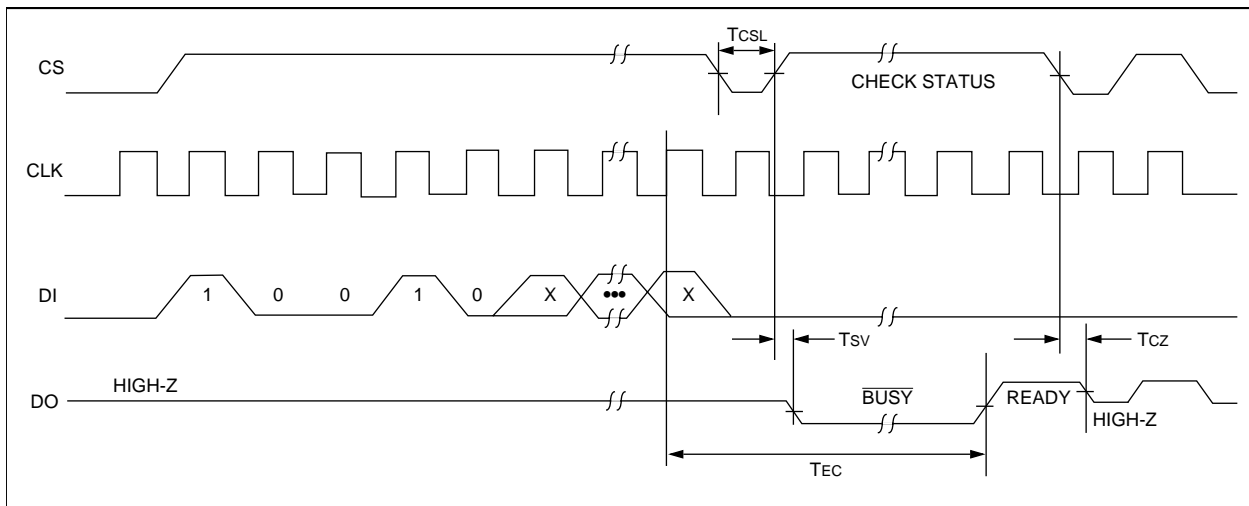
The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the rising clock edge of the last address bit. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/ $\overline{\text{BUSY}}$  status of the device, if CS is brought high after a minimum of 250 ns low ( $T_{\text{CSL}}$ ) and before the entire ERAL cycle is complete.

**FIGURE 3-2: ERASE TIMING**



**FIGURE 3-3: ERAL TIMING**



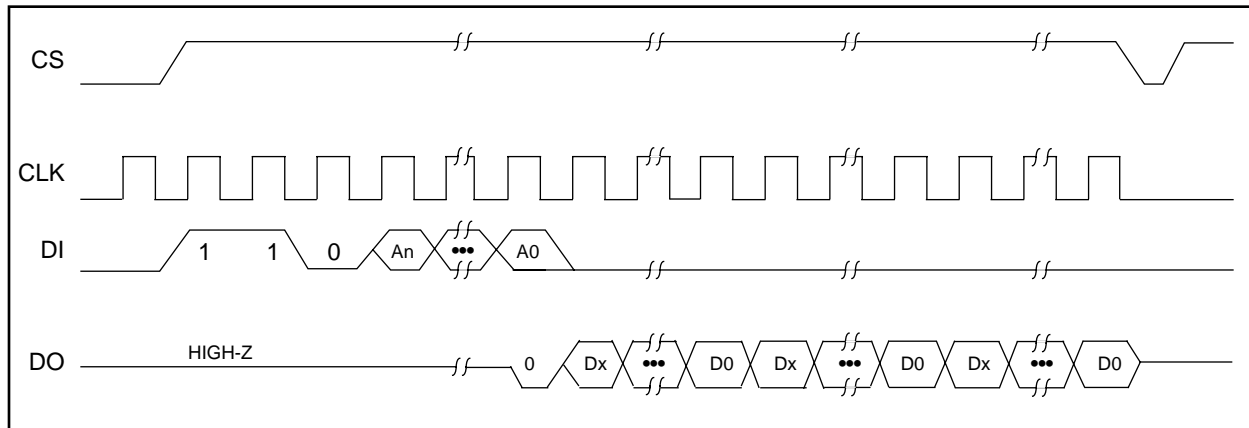
### 3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The device powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

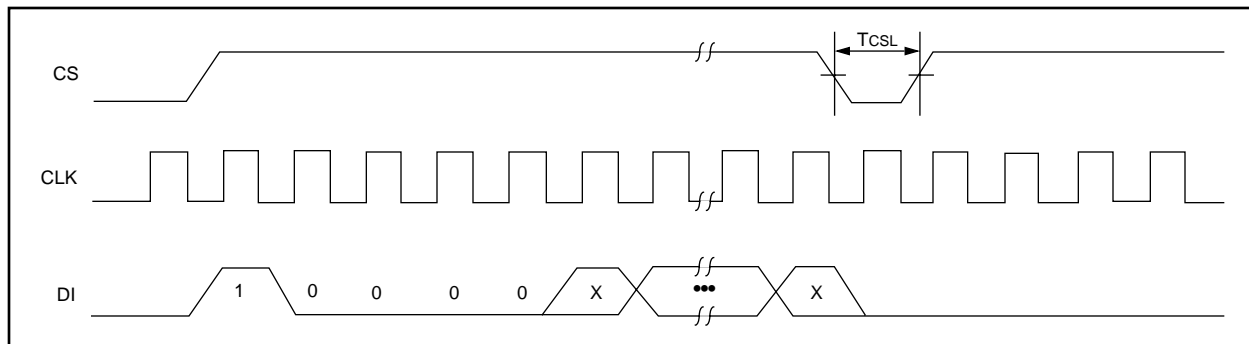
### 3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93C56A) or 16-bit (93C56B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

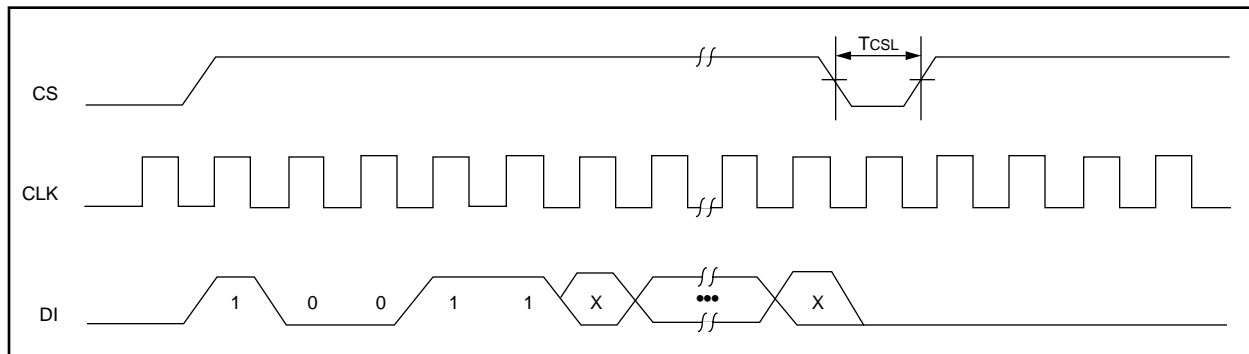
**FIGURE 3-4: READ TIMING**



**FIGURE 3-5: EWDS TIMING**



**FIGURE 3-6: EWEN TIMING**



## 3.8 WRITE

The WRITE instruction is followed by 8-bits (93C56A) 16-bits (93C56B) of data which are written into the specified address. After the last data bit is clocked into the DI pin, the self-timed auto-erase and programming cycle begins.

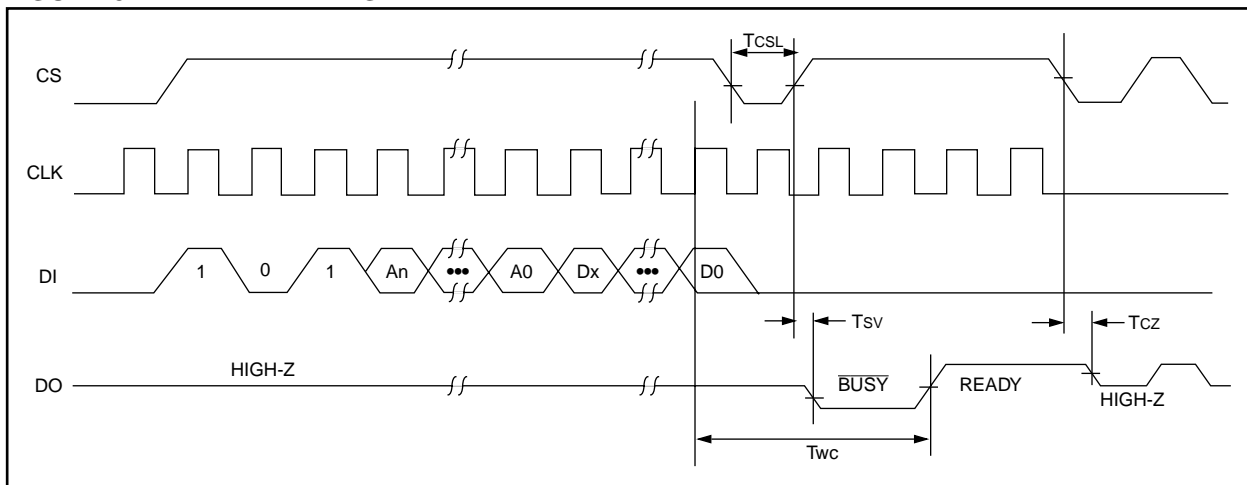
The DO pin indicates the  $\text{READY}/\overline{\text{BUSY}}$  status of the device, if CS is brought high after a minimum of 250 ns low ( $T_{\text{CSL}}$ ) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

## 3.9 Write All (WRAL)

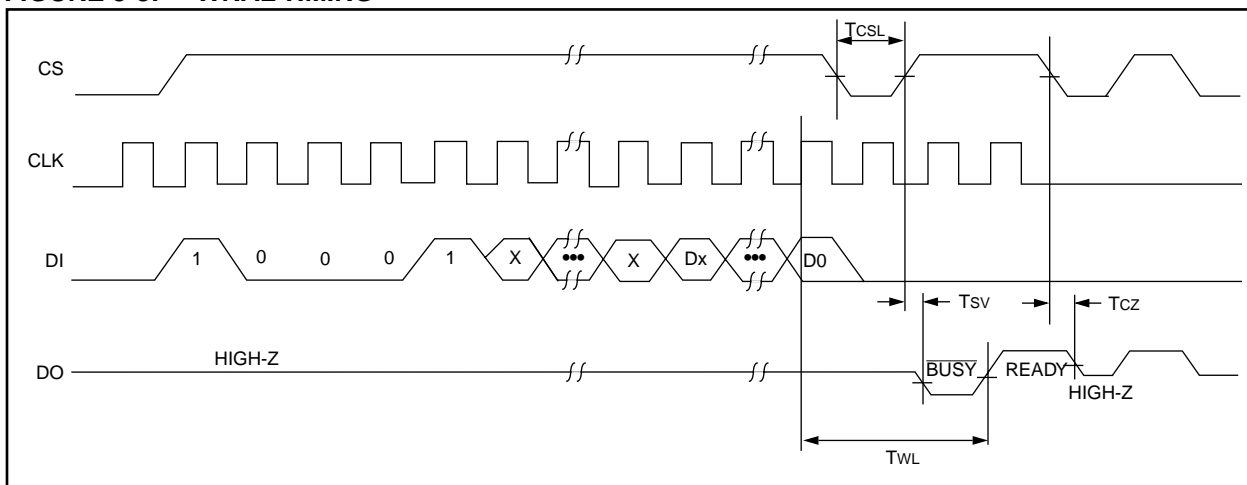
The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the rising clock edge of the last data bit. Cloning of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the  $\text{READY}/\overline{\text{BUSY}}$  status of the device if CS is brought high after a minimum of 250 ns low ( $T_{\text{CSL}}$ ).

**FIGURE 3-7: WRITE TIMING**



**FIGURE 3-8: WRAL TIMING**



# 93C56A/B

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NOTES:



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