24AA32A

32K 1.8V I²C™ Serial EEPROM

FEATURES

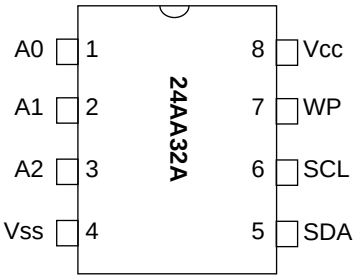
- Single supply with operation down to 1.8V
  - Maximum write current 3 mA at 6.0V
  - Standby current 1 µA max at 1.8V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Hardware write protect
- 1,000,000 Erase/Write cycles guaranteed
- 32 byte page or byte write modes available
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to eight devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C

DESCRIPTION

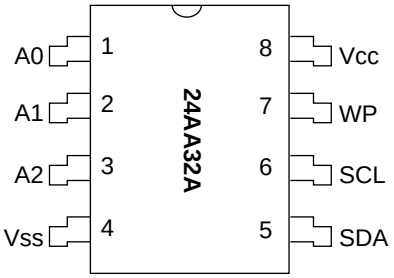
The Microchip Technology Inc. 24AA32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 6.0V). It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24AA32A also has a page-write capability of up to 32 bytes of data. The 24AA32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24AA32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low-voltage, nonvolatile code and data applications. The 24AA32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packages.

PACKAGE TYPE

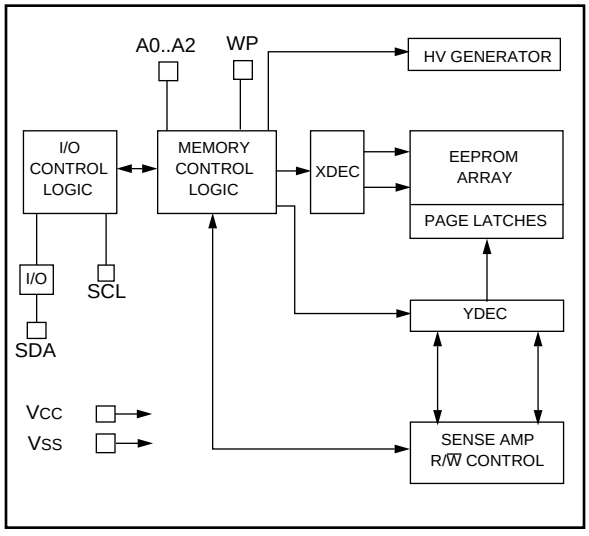
PDIP



SOIC



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65˚C to +150˚C
Ambient temp. with power applied ..... -65˚C to +125˚C
Soldering temperature of leads (10 seconds) ..... +300˚C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 6.0V Power Supply

TABLE 1-2: DC CHARACTERISTICS

Vcc = +1.8V to 6.0V
Commercial (C) Tamb = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
A0, A1, A2, SCL , SDA and WP pins:						
High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC		—	V	(Note)
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN,COUT	—		10	pF	VCC = 5.0V (Note) Tamb = 25˚C, F_c = 1 MHz
Operating current	ICC Write	—		3	mA	VCC = 6.0V
	ICC Read	—		0.5	mA	VCC = 6.0V, SCL = 400kHz
Standby current	ICCS	—	1	5	µA	SCL = SDA = VCC = 5.5V
	ICCS			1	µA	VCC = 1.8V (Note)

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

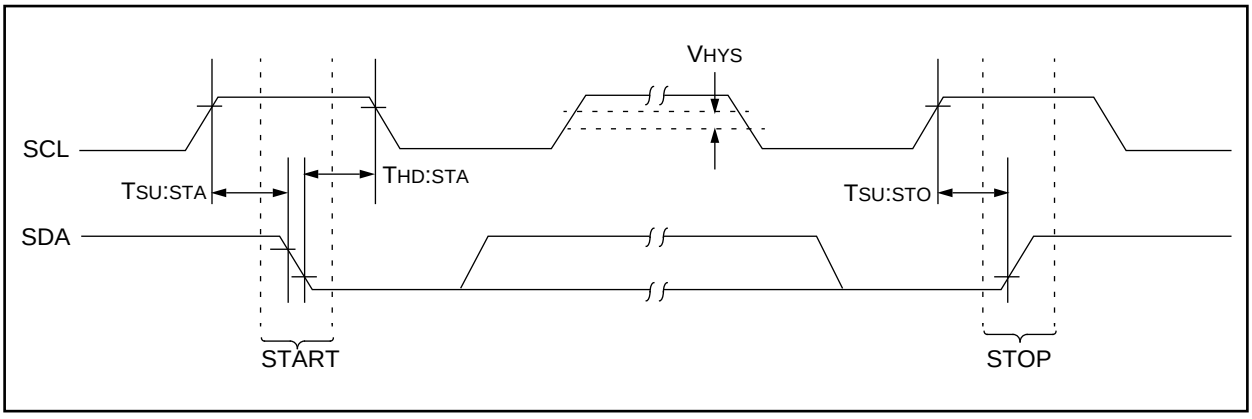


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 1.8-6.0V STD. MODE		Vcc = 4.5-6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms	Byte or Page Mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

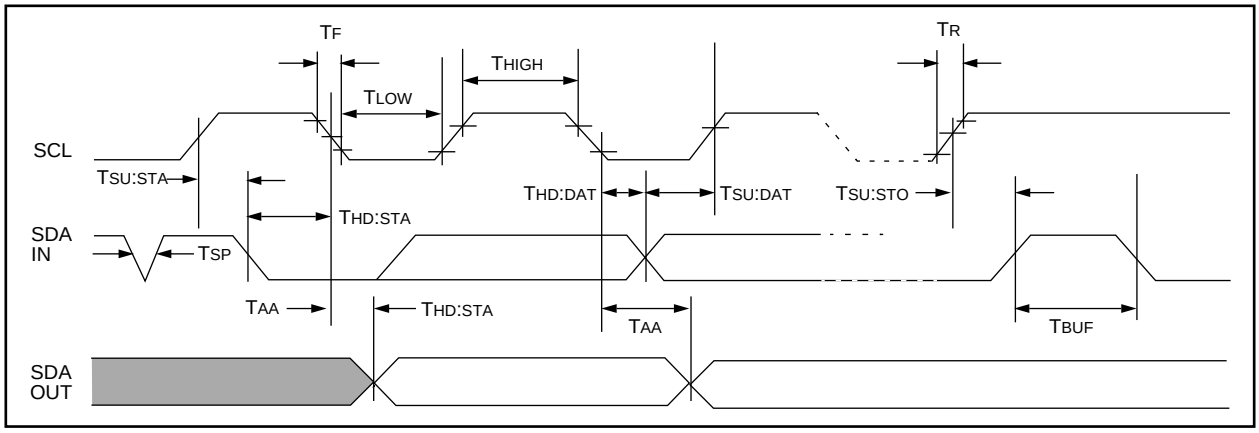
Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a trasmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA32A supports a Bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA32A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

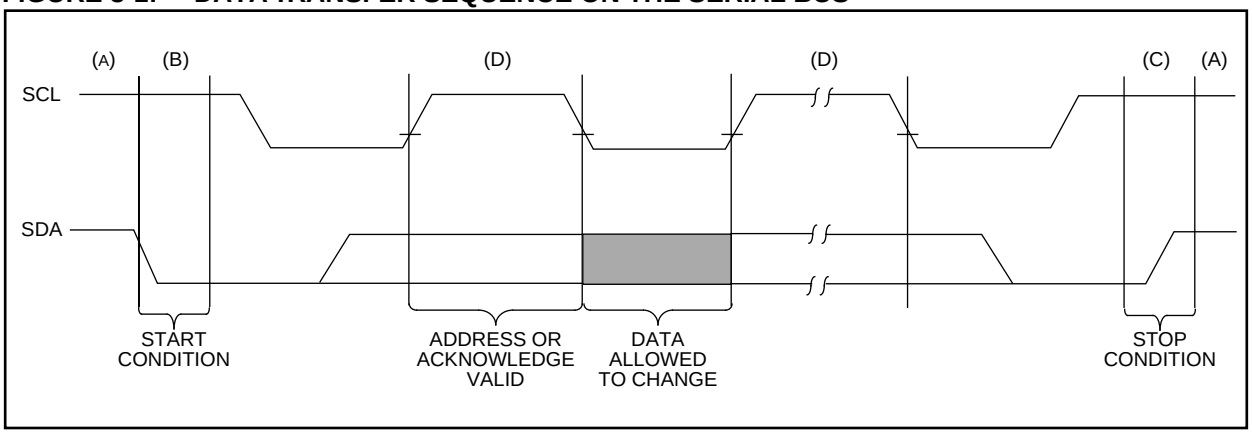
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24AA32A does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA32A) will leave the data line HIGH to enable the master to generate the STOP condition.

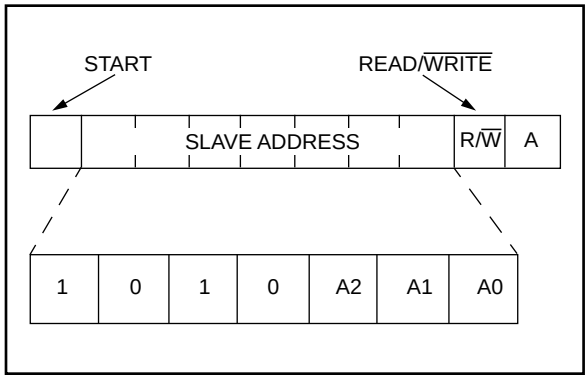
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code; for the 24AA32A this is set as 1010 binary for read and write (R/$\overline{W}$) operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

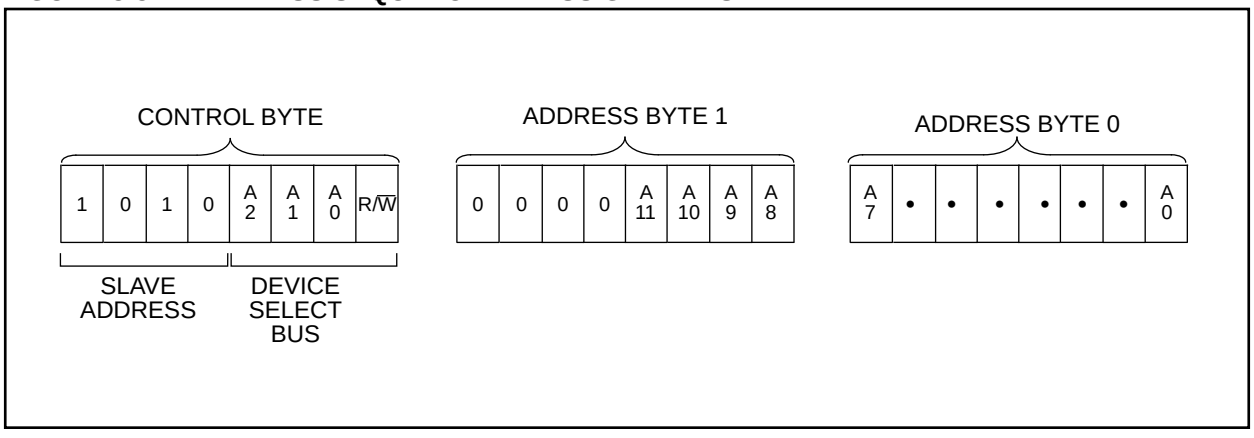
FIGURE 3-2: CONTROL BYTE ALLOCATION



Following the start condition, the 24AA32A monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA32A will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA32A. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA32A the master device will transmit the data word to be written into the addressed memory location.

The 24AA32A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA32A will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA32A in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 32 bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin. (Figure 4-2).

FIGURE 4-1: BYTE WRITE

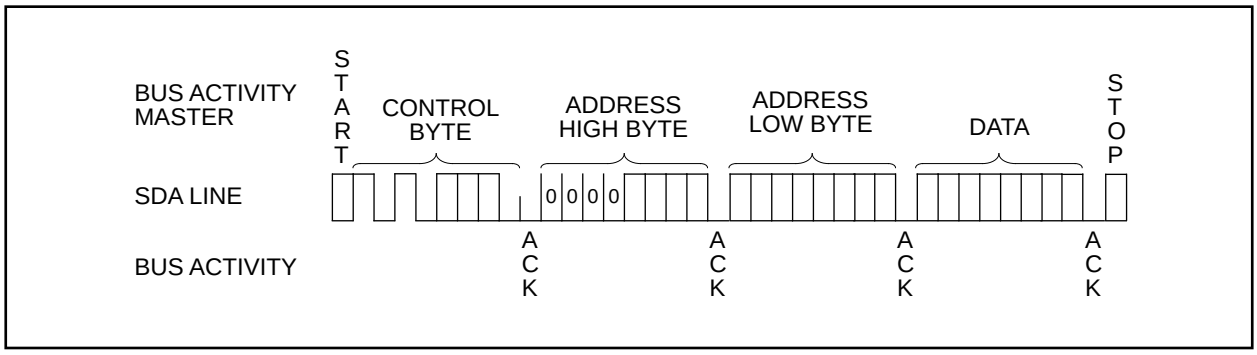
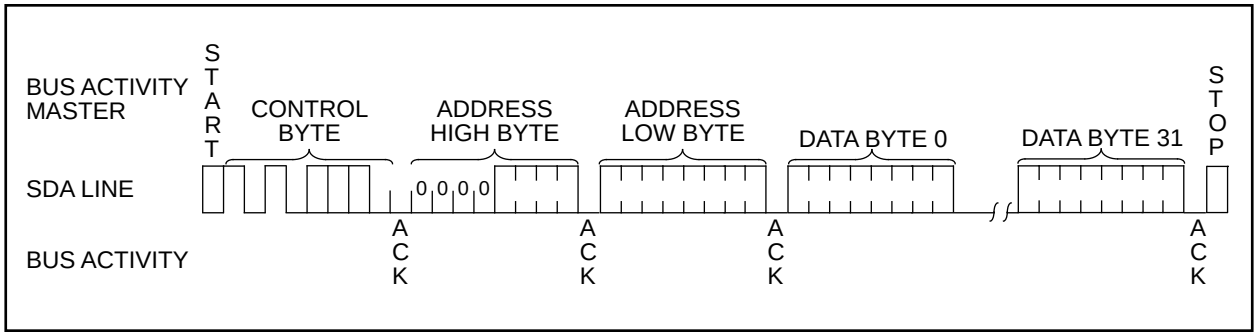


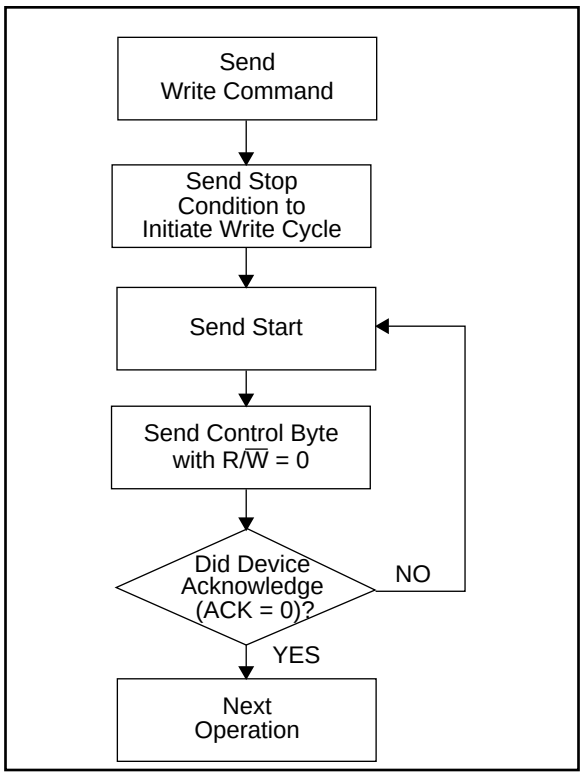
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. Acknowledge Polling (ACK) can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

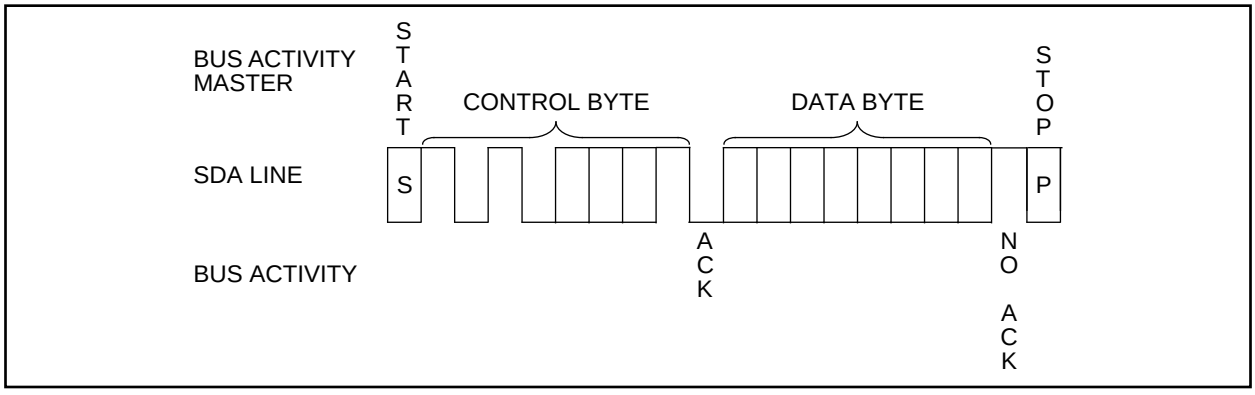
6.1 Current Address Read

The 24AA32A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA32A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA32A discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA32A as part of a write operation (R/$\overline{W}$ bit set to zero). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA32A will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA32A to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24AA32A's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA32A transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA32A to transmit the next sequentially addressed 8-bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA32A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFF to address 000 if the master acknowledges the byte received from the array address 0FFF.

FIGURE 6-2: RANDOM READ

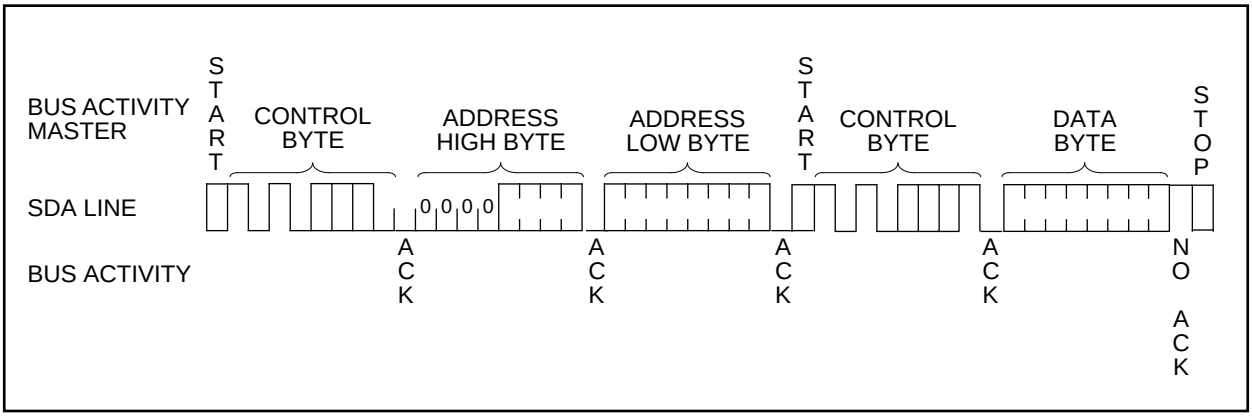
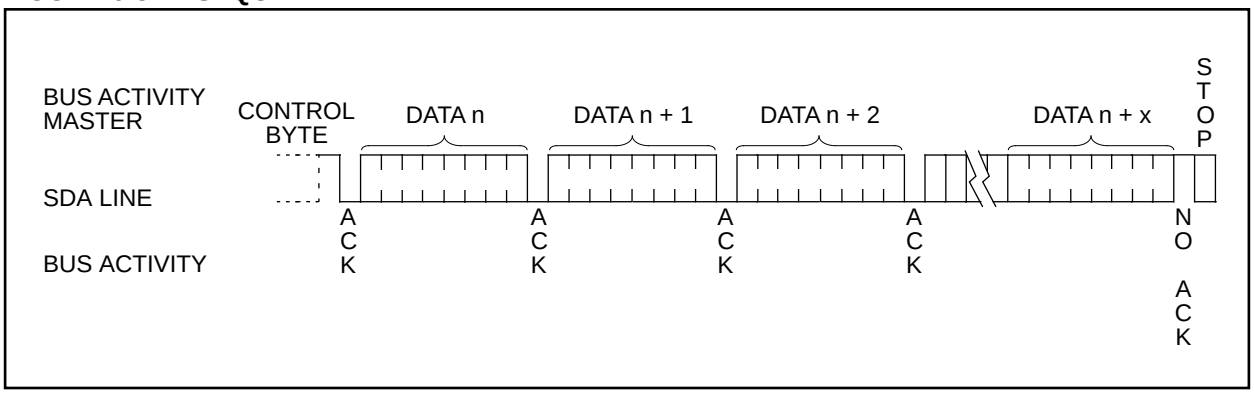


FIGURE 6-3: SEQUENTIAL READ



7.0 PIN DESCRIPTIONS

7.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

7.2 SDA Serial Address/Data Input/Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

7.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

7.4 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-FFF).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

8.0 NOISE PROTECTION

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

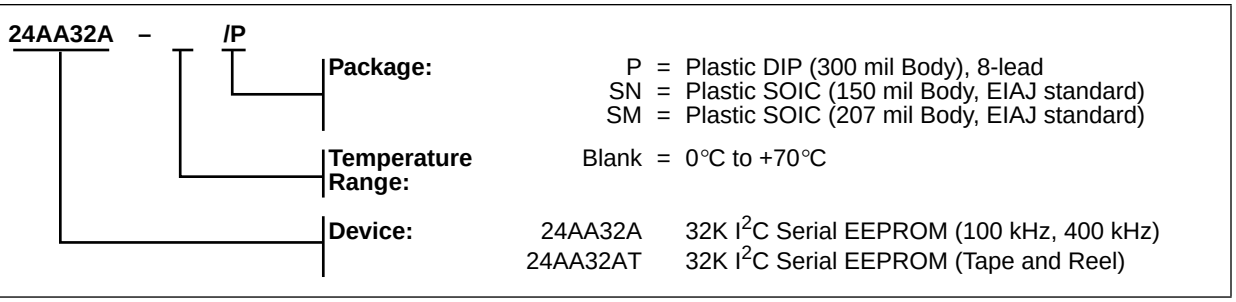
9.0 POWER MANAGEMENT

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e., not receiving an acknowledge or stop condition per the 2-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

NOTES:

24AA32A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



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