24AA00/24LC00/24C00

128 Bit I²C™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Device	Vcc Range	Temp Range
24AA00	1.8 - 6.0	C,I
24LC00	2.5 - 6.0	C,I
24C00	4.5 - 5.5	C,I,E

FEATURES

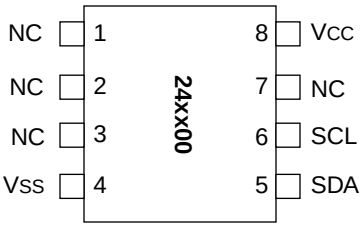
- Low power CMOS technology
  - 500 µA typical active current
  - 500 nA typical standby current
- Organized as 16 bytes x 8 bits
- 2-wire serial interface bus, I²C™ compatible
- 100kHz (1.8V) and 400kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- 4 ms maximum byte write cycle time
- 1,000,000 erase/write cycles guaranteed
- ESD protection > 4kV
- Data retention > 200 years
- 8L DIP, SOIC, TSSOP and 5L SOT-23 packages
- Temperature ranges available:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) -40°C to +125°C

DESCRIPTION

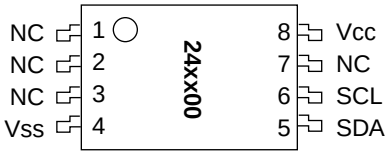
The Microchip Technology Inc. 24AA00/24LC00/24C00 (24xx00*) is a 128-bit Electrically Erasable PROM memory organized as 16 x 8 with a 2-wire serial interface. Low voltage design permits operation down to 1.8 volts for the 24xx00 version, and every version maintains a maximum standby current of only 1 µA and typical active current of only 500 µA. This device was designed where a small amount of EEPROM is needed for the storage of calibration values, ID numbers or manufacturing information, etc. The 24xx00 is available in 8ld PDIP, 8ld SOIC (150 mil), 8ld TSSOP and the 5ld SOT-23 packages.

PACKAGE TYPES

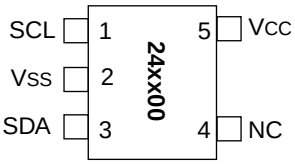
8-PIN PDIP/SOIC



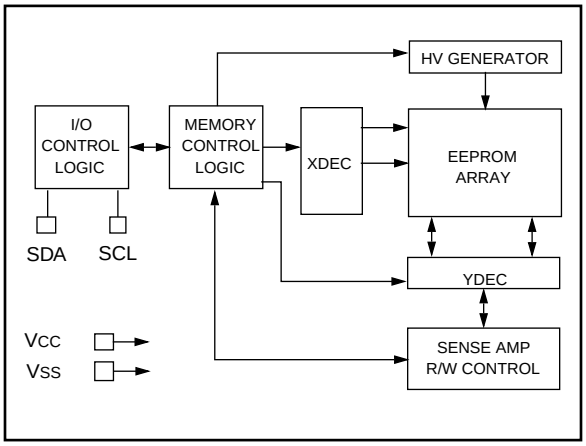
8-PIN TSSOP



5-PIN SOT-23



BLOCK DIAGRAM



*24xx00 is used in this document as a generic part number for the 24AA00/24LC00/24C00 devices.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss..... -0.6V to Vcc +1.0V
Storage temperature ..... -65˚C to +150˚C
Ambient temp. with power applied..... -65˚C to +125˚C
Soldering temperature of leads (10 seconds) ..... +300˚C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	+1.8V to 6.0V (24AA00) +2.5V to 6.0V (24LC00) +4.5V to 5.5V (24C00)
NC	No Internal Connection

TABLE 1-2 DC CHARACTERISTICS

All Parameters apply across the recommended operating ranges unless otherwise noted	Commercial (C): Tamb = 0˚C to +70˚C, Vcc = 1.8V to 6.0V Industrial (I): Tamb = -40˚C to +85˚C, Vcc = 1.8V to 6.0V Automotive (E) Tamb = -40˚C to +125˚C, Vcc = 4.5V to 5.5V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	.7 VCC		V	(Note)
Low level input voltage	VIL		.3 VCC	V	(Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, VCC = Vcc_{MIN}
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to 5.5V
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25˚C, f = 1 MHz
Operating current	ICC Write	—	2	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	1	µA	VCC = 5.5V, SDA = SCL = VCC

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING DATA

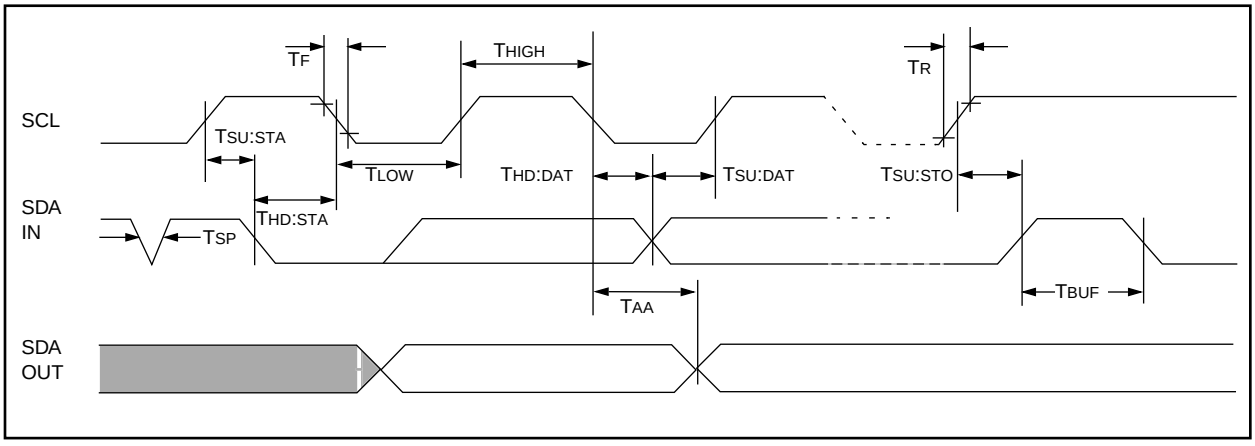


TABLE 1-3 AC CHARACTERISTICS

All Parameters apply across all recommended operating ranges unless otherwise noted	Commercial (C):	Tamb = 0°C to +70°C, Vcc = 1.8V to 6.0V			
	Industrial (I):	Tamb = -40°C to +85°C, Vcc = 1.8V to 6.0V			
	Automotive (E):	Tamb = -40°C to +125°C, Vcc = 4.5V to 5.5V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Output fall time from VIH minimum to VIL maximum	TOF	20+0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	4	ms	
Endurance		1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's BBS or website.

2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10kΩ for 100 kHz, 1kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 Noise Protection

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24xx00 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24xx00 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

0.1 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.3 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

4.4 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24xx00 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

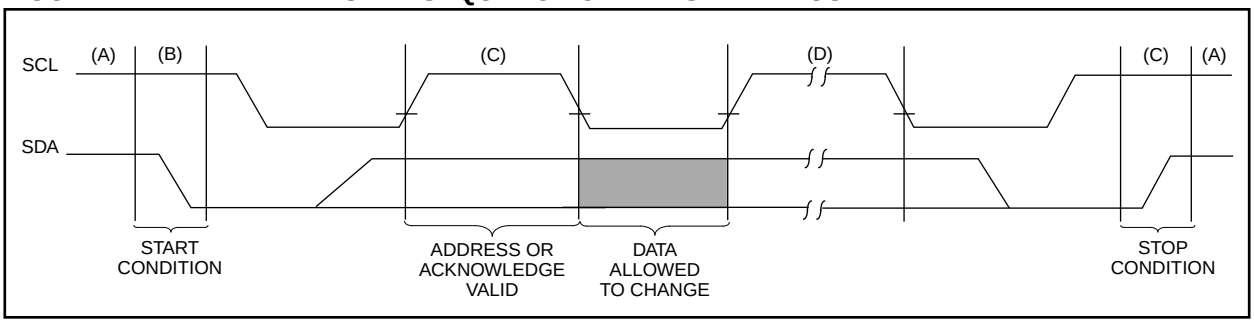
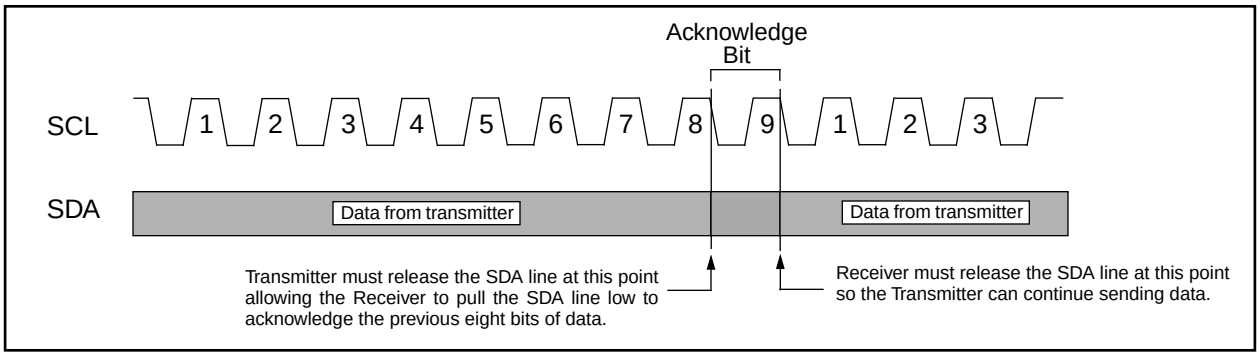


FIGURE 4-2: ACKNOWLEDGE TIMING

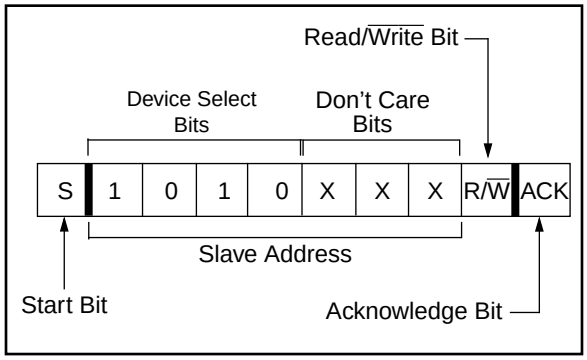


5.0 DEVICE ADDRESSING

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/$\overline{\text{Write}}$ bit that indicates what type of operation is to be performed. The slave address for the 24xx00 consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 5-1). The 24xx00 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 5-1: CONTROL BYTE FORMAT



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24xx00. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The 24xx00 will acknowledge the address byte and the master device will then transmit the data word to be written into the addressed memory location. The 24xx00 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24xx00 will not generate acknowledge signals (Figure 7-2). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The 24xx00 employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5V (24AA00 and 24LC00) or 3.8V (24C00) at nominal conditions.

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW

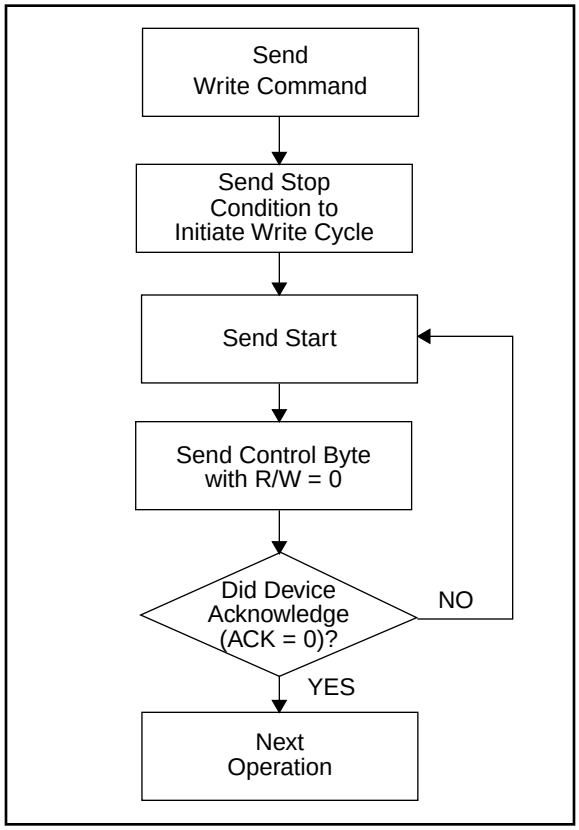
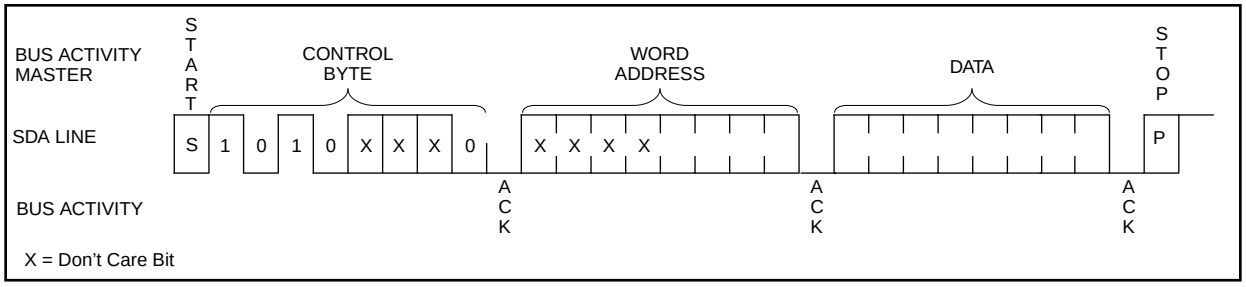


FIGURE 7-2: BYTE WRITE



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24xx00 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24xx00 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24xx00 contains an internal address pointer which is incremented by one at the completion of each read operation. This address pointer allows the entire memory contents to be serially read during one operation.

FIGURE 8-1: CURRENT ADDRESS READ

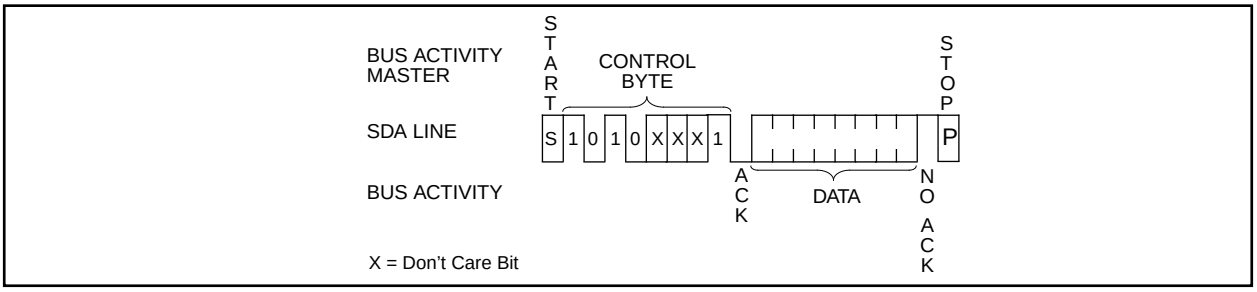


FIGURE 8-2: RANDOM READ

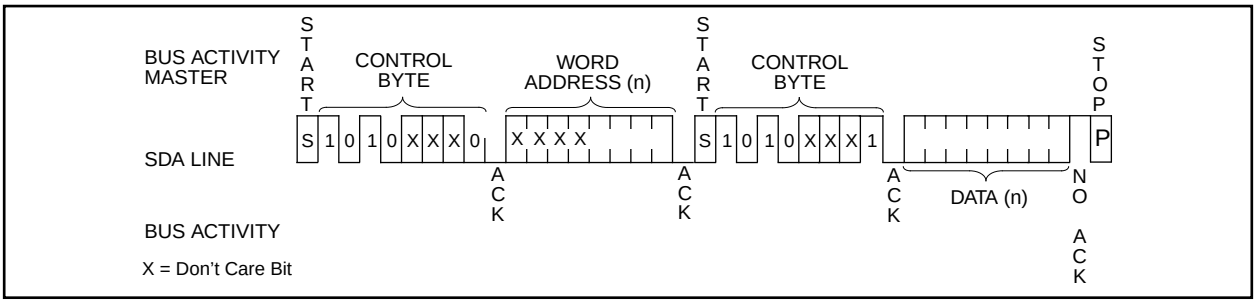
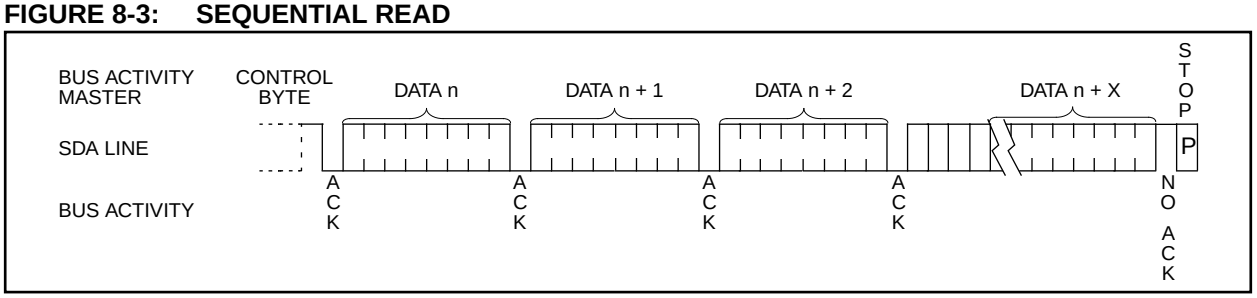


FIGURE 8-3: SEQUENTIAL READ



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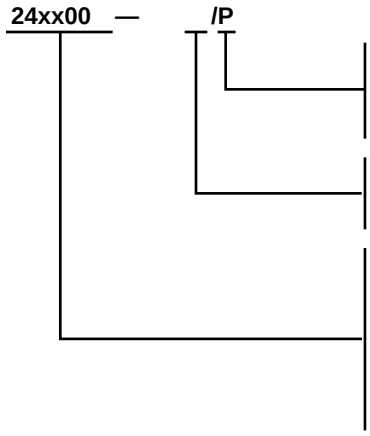
24XX00 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body)
	ST =	TSSOP, 8-lead
	OT =	SOT-23, 5 lead
Temperature Range:	Blank =	0˚C to +70˚C
	I =	–40˚C to +85˚C
	E =	–40˚C to +125˚C
Device:	24AA00	128 bit 1.8V I^2C Serial EEPROM
	24AA00T	128 bit 1.8V K I^2C Serial EEPROM (Tape and Reel)
	24LC00	128 bit 2.5V I^2C Serial EEPROM
	24LC00T	128 bit 2.5V K I^2C Serial EEPROM (Tape and Reel)
	24C00	128 bit 5.0V I^2C Serial EEPROM
	24C00T	128 bit 5.0V K I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see last page)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Development Tools

For the latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302. The latest version of Development Tools software can be downloaded from either our Bulletin Board or Worldwide Web Site. (Information on how to connect to our BBS or WWW site can be found in the On-Line Support section of this data sheet.)

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