

# DATA SHEET

## **CBT3857**

10-bit bus switch with 10 k $\Omega$  pull-down  
termination resistors

Product specification  
Supersedes data of 1998 Dec 10

1999 Sep 14

# 10-bit bus switch with 10 k $\Omega$ pull-down termination resistors

## CBT3857

### FEATURES

- Enable signal is SSTL\_2 compatible
- Optimized for use in Double Data Rate (DDR) SDRAM applications
- Flow-through architecture optimizes PCB layout
- Designed to be used with 200 Mbps
- Switch on resistance is designed to eliminate the need for series resistor to DDR SDRAM
- Internal 10 k $\Omega$  pull-down resistors on B port
- Internal 50 k $\Omega$  pull-up resistor on output enable input
- Full DDR solution provided when used with SSTL16857 and PCK857
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

### DESCRIPTION

This 10-bit bus switch is designed for 3 V to 3.6 V  $V_{CC}$  operation and SSTL\_2 output enable ( $\overline{OE}$ ) input levels.

When  $\overline{OE}$  is LOW, the 10-bit bus switch is on and port A is connected to port B. When  $\overline{OE}$  is HIGH, the switch is open, and a high-impedance state exists between the two ports.

The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3857 is characterized for operation from 0°C to +85°C.

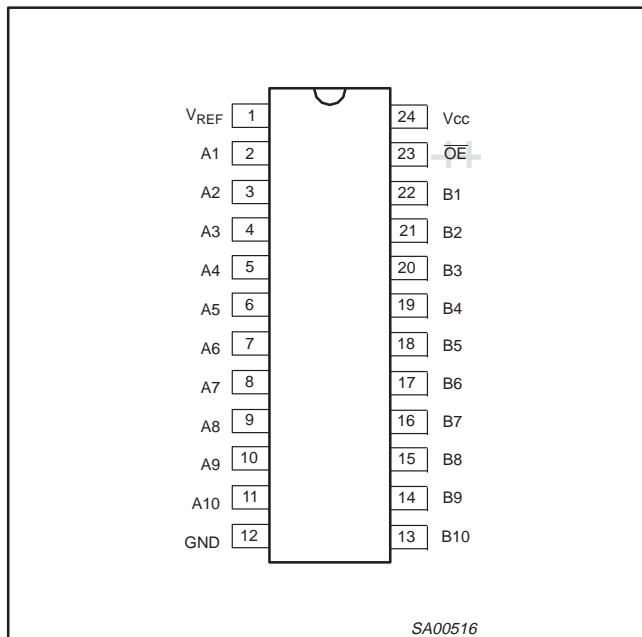
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0 \text{ V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Yn	$C_L = 30 \text{ pF}; V_{CC} = 3.3 \text{ V}$	720	ps
$C_{IN}$	Input capacitance	$V_I = 0 \text{ V or } V_{CC}$	2.8	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0 \text{ V or } V_{CC}$	6.4	pF
$I_{CCZ}$	Total supply current	$V_{CC} = 3.6 \text{ V}$	1	mA

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic TSSOP Type I	0°C to +85°C	CBT3857 PW	SOT355-1

### PIN CONFIGURATION



### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$V_{REF}$	Reference output voltage
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A1–A10	Inputs
12	GND	Ground (V)
22, 21, 20, 19, 18, 17, 16, 15, 14, 13	B1–B10	Outputs
23	$\overline{OE}$	Output enable
24	$V_{CC}$	Positive supply voltage

### FUNCTION TABLE

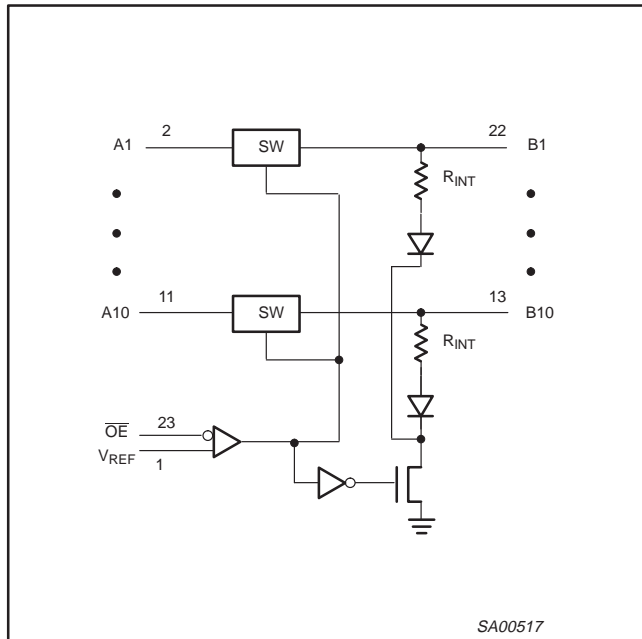
INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

H = High voltage level  
L = Low voltage level

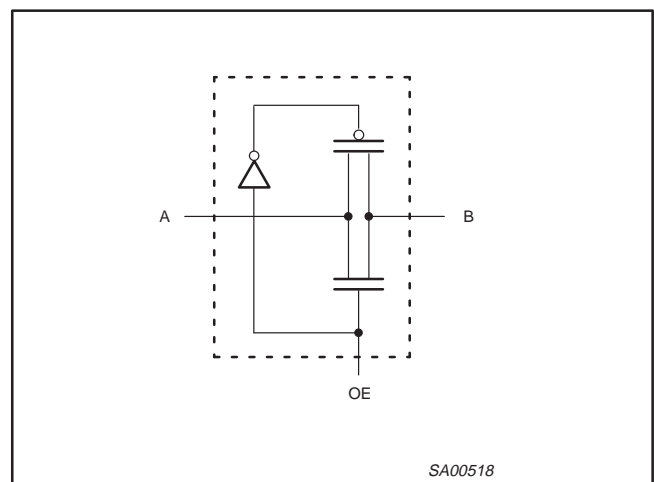
# 10-bit bus switch with 10 kΩ pull-down termination resistors

CBT3857

## LOGIC DIAGRAM (POSITIVE LOGIC)



## SIMPLIFIED SCHEMATIC, EACH FET SWITCH



## ABSOLUTE MAXIMUM RATINGS<sup>1, 3</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input clamp current	V <sub>I/O</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage range (OE only) <sup>2</sup>		V <sub>CC</sub> + 0.5	V
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C
V <sub>I</sub>	DC input voltage range (except OE) <sup>2</sup>		-0.5 to 4.6	V

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V <sub>CC</sub>	DC supply voltage	3	3.3	3.6	V
V <sub>REF</sub>	Reference voltage (0.38 x V <sub>CC</sub> )	1.15	1.25	1.35	V
V <sub>IH</sub>	AC high-level input voltage	V <sub>REF</sub> + 350 mV			V
V <sub>IL</sub>	AC low-level Input voltage			V <sub>REF</sub> - 350 mV	V
V <sub>IH</sub>	DC high-level input voltage	V <sub>REF</sub> + 180 mV			V
V <sub>IL</sub>	DC low-level Input voltage			V <sub>REF</sub> - 180 mV	V
T <sub>amb</sub>	Operating free-air temperature range	0		+85	°C

### NOTE:

- All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

# 10-bit bus switch with 10 kΩ pull-down termination resistors

CBT3857

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			T <sub>amb</sub> = 0°C to +85°C				
			Min	Typ <sup>1</sup>	Max		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 3 V; I <sub>I</sub> = -18 mA			-1.2	V	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	OE		±0.73	±500	μA
			A Port		±0.1	±1	μA
			B Port		±20	±500	μA
			V <sub>REF</sub>		±0.1	±1	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		0.7	1.5	mA	
C <sub>I</sub>	Control pins	V <sub>I</sub> = 3 V or 0		2.8		pF	
C <sub>IO(OFF)</sub>	Power-off leakage current	V <sub>O</sub> = 3 V or 0; OE = V <sub>CC</sub>		6.4		pF	
r <sub>on</sub> <sup>2</sup>	On-resistance	V <sub>CC</sub> = 3 V to 3.6 V; V <sub>A</sub> = 0.8 V; V <sub>B</sub> = 1.15 V	20	24	30	Ω	
		V <sub>CC</sub> = 3 V to 3.6 V; V <sub>A</sub> = 1.7 V; V <sub>B</sub> = 1.35 V	20	24	30		
		V <sub>CC</sub> = 3 V to 3.6 V; V <sub>I</sub> = 1.25 V; I <sub>I</sub> = ±10 mA	20	24	30		
r <sub>off</sub> <sup>2</sup>	Off-resistance	V <sub>CC</sub> = 3 V to 3.6 V; V <sub>I</sub> = 1.65 V	1			MΩ	

**NOTES:**

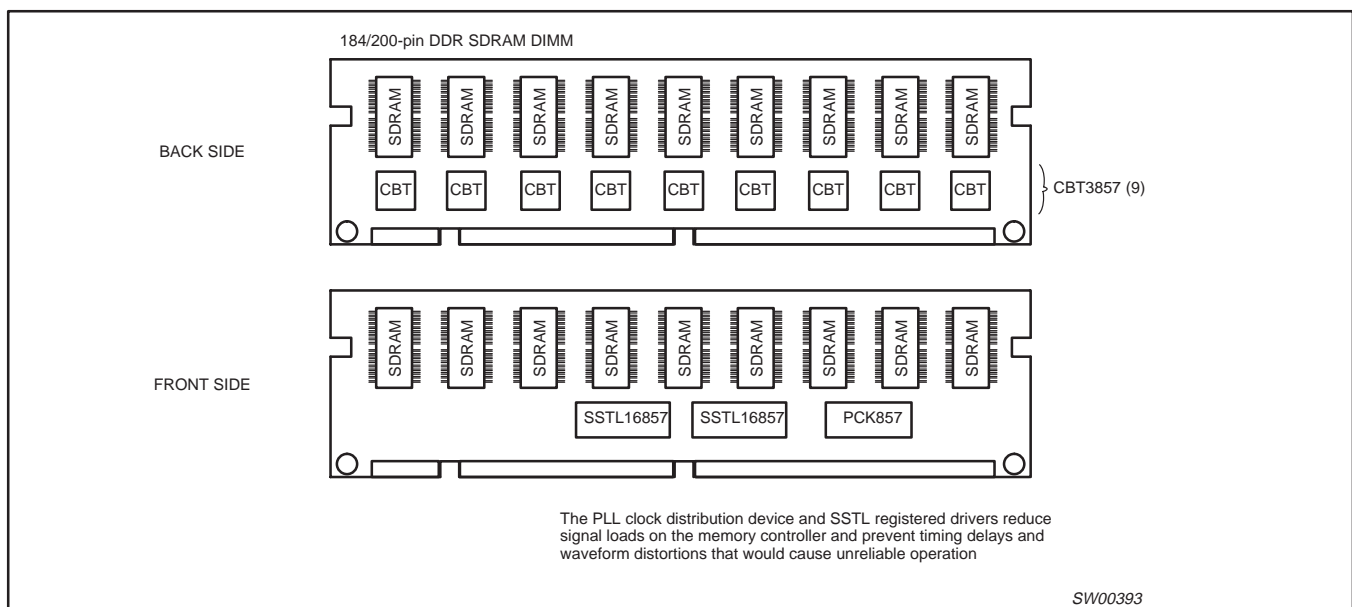
- All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>amb</sub> = 25°C
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## AC CHARACTERISTICS

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = +3.3 V ±0.3 V		UNIT
				Min	Max	
t <sub>pd</sub>	Propagation delay <sup>1</sup>	A or B	B or A		750	ps
t <sub>en</sub>	enable	OE	A or B	1	3	ns
t <sub>dis</sub>	disable	OE	A or B	1	3	ns

**NOTE:**

- The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 24 Ω × 30 pF.

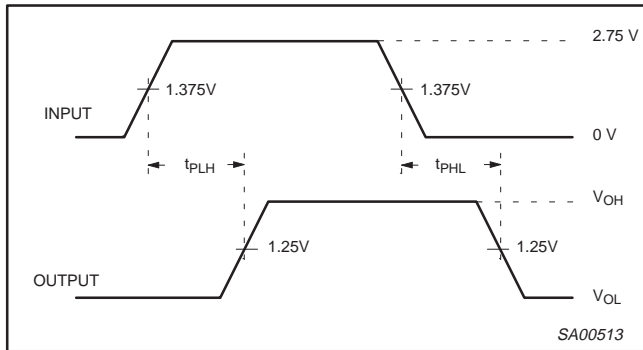


# 10-bit bus switch with 10 kΩ pull-down termination resistors

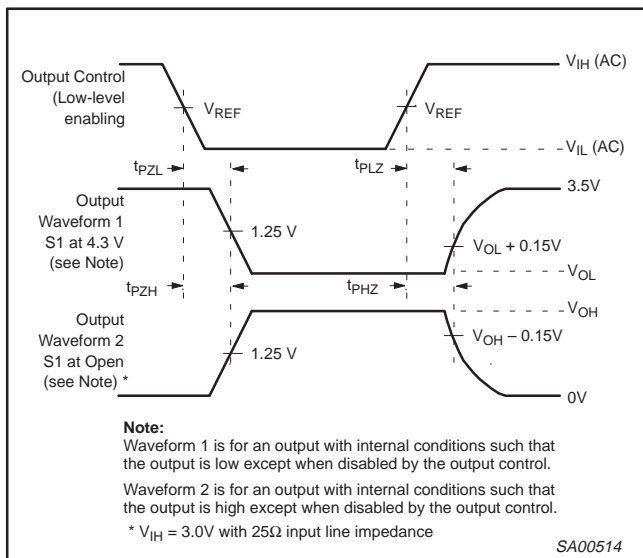
CBT3857

## AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 3.0\text{ V}$

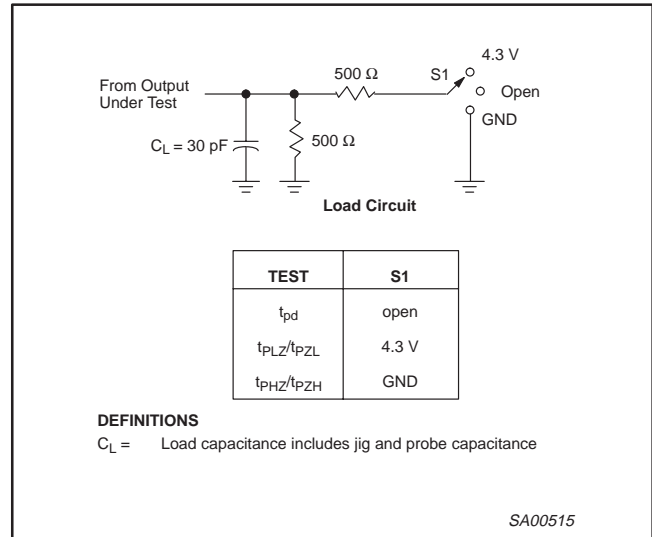


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

## TEST CIRCUIT AND WAVEFORMS



**DEFINITIONS**

$C_L =$  Load capacitance includes jig and probe capacitance

**NOTES:**

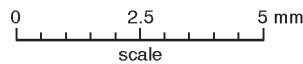
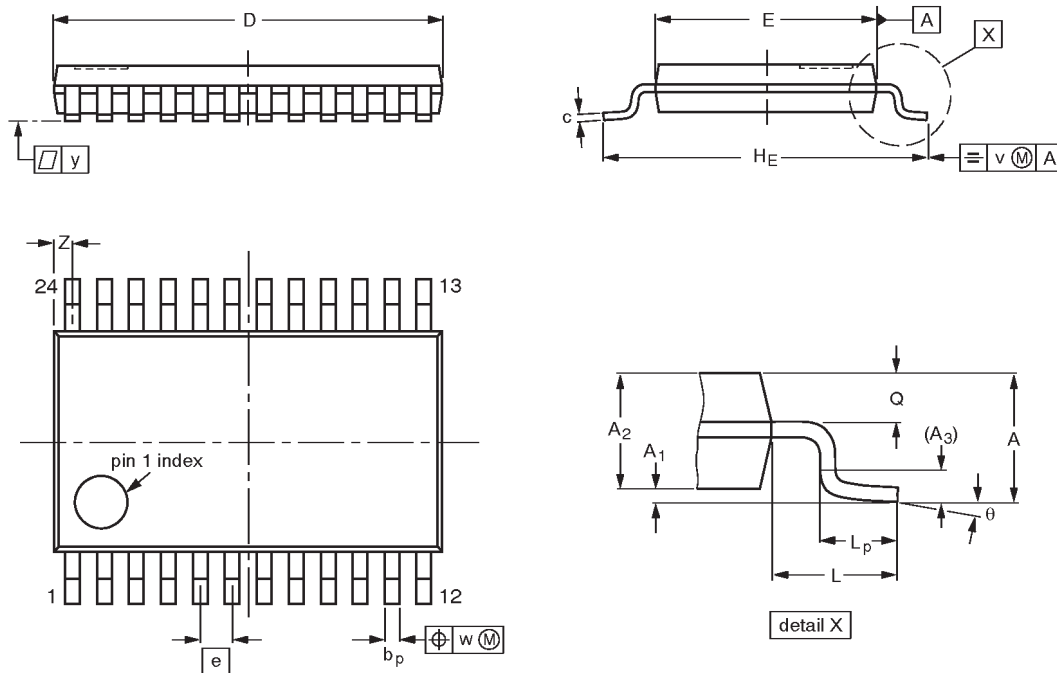
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
2. The outputs are measured one at a time with one transition per measurement.

# 10-bit bus switch with 10 kΩ pull-down termination resistors

## CBT3857

**TSSOP24:** plastic thin shrink small outline package; 24 leads; body width 4.4 mm

**SOT355-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				-93-06-16 95-02-04

---

10-bit bus switch with 10 k $\Omega$  pull-down  
termination resistors

---

CBT3857

**NOTES**

# 10-bit bus switch with 10 k $\Omega$ pull-down termination resistors

CBT3857

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1999  
All rights reserved. Printed in U.S.A.

Date of release: 09-99

Document order number:

9397-750 -06413

*Let's make things better.*

Philips  
Semiconductors



**PHILIPS**