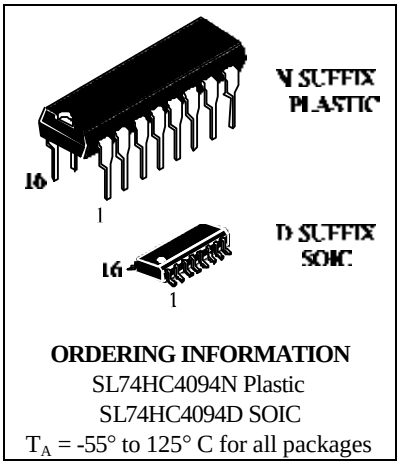
8-Bit Serial-Input Shift Register With Latched 3-State Outputs

High-Performance Silicon-Gate CMOS



ORDERING INFORMATION
SL74HC4094N Plastic
SL74HC4094D SOIC
T_A = -55° to 125° C for all packages

The SL74HC4094 is identical in pinout to the LS/ALS4094. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

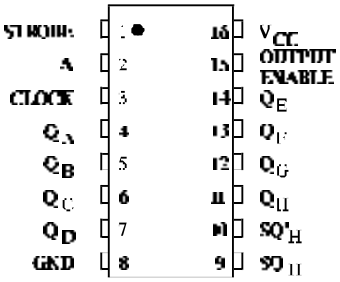
This device consists of an 8-bit shift register and 8-bit D-type latch with three-state parallel outputs. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage SQ_H can be used to cascade several devices.

Data on the SQ_H output is transferred to a second output (SQ_H') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the Strobe input signal. When the Strobe input is held high, data propagates through the latch to a 3-state output buffer.

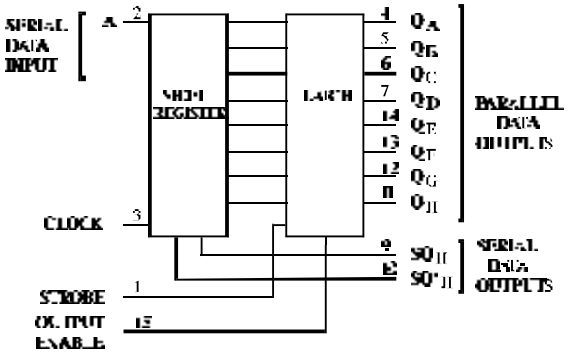
This buffer is enabled when Output Enable input is taken high.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- High Noise Immunity Characteristic of CMOS Devices

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs				Parallel Outputs		Serial Outputs	
Clock	Output Enable	Strobe	A	Q_A	Q_N	SQ_H	SQ_H'
⌐	L	X	X	Z	Z	Q6	NC
¬	L	X	X	Z	Z	NC	SQ_H
⌐	H	L	X	NC	NC	Q6	NC
⌐	H	H	L	L	Q_{N-1}	Q6	NC
⌐	H	H	H	H	Q_{N-1}	Q6	NC
¬	H	X	X	NC	NC	NC	SQ_H

NC = No Change
Z = high impedance
X = don' t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}= V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V_{IN}= V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25 °C to -55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	6 30 35	5 25 28	4 20 23	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to SQ_H (Figures 1 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q_A-Q_H (Figures 2 and 5)	2.0 4.5 6.0	195 40 33	245 50 42	295 60 50	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay ,Output Enable to Q_A-Q_H (Figures 3 and 6)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay ,Output Enable to Q_A-Q_H (Figures 3 and 6)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q_A-Q_H	-	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 300	pF

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25 °C to -55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t_{su}	Minimum Setup Time, Serial Data Input A to Clock (Figure 4)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, Clock to Data Input A (Figure 4)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t_w	Minimum Pulse Width, Strobe (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

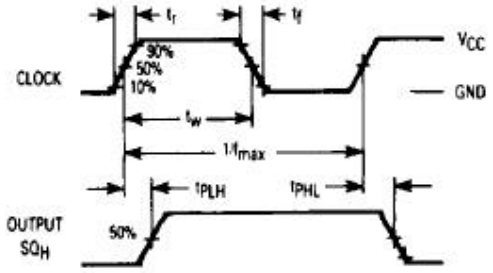


Figure 1. Switching Waveforms

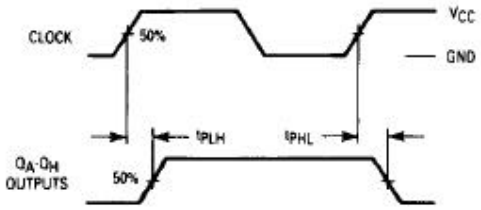


Figure 2. Switching Waveforms

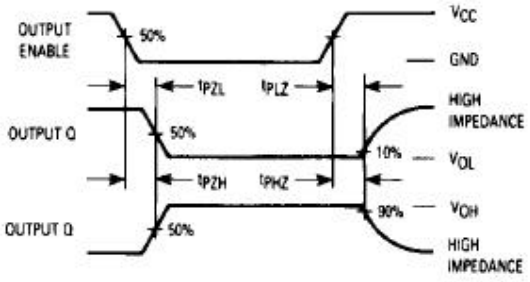


Figure 3. Switching Waveforms

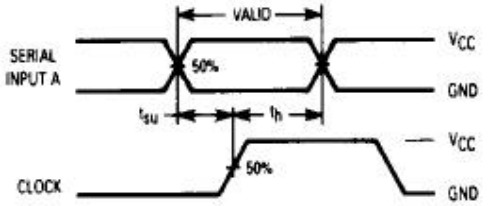
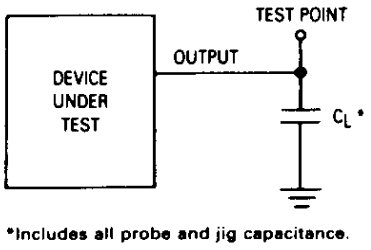
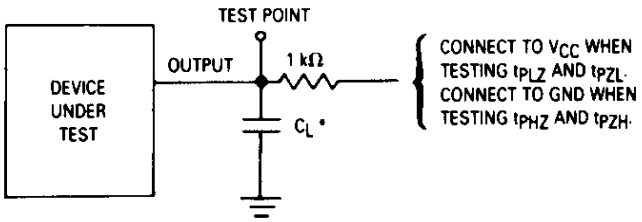


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.

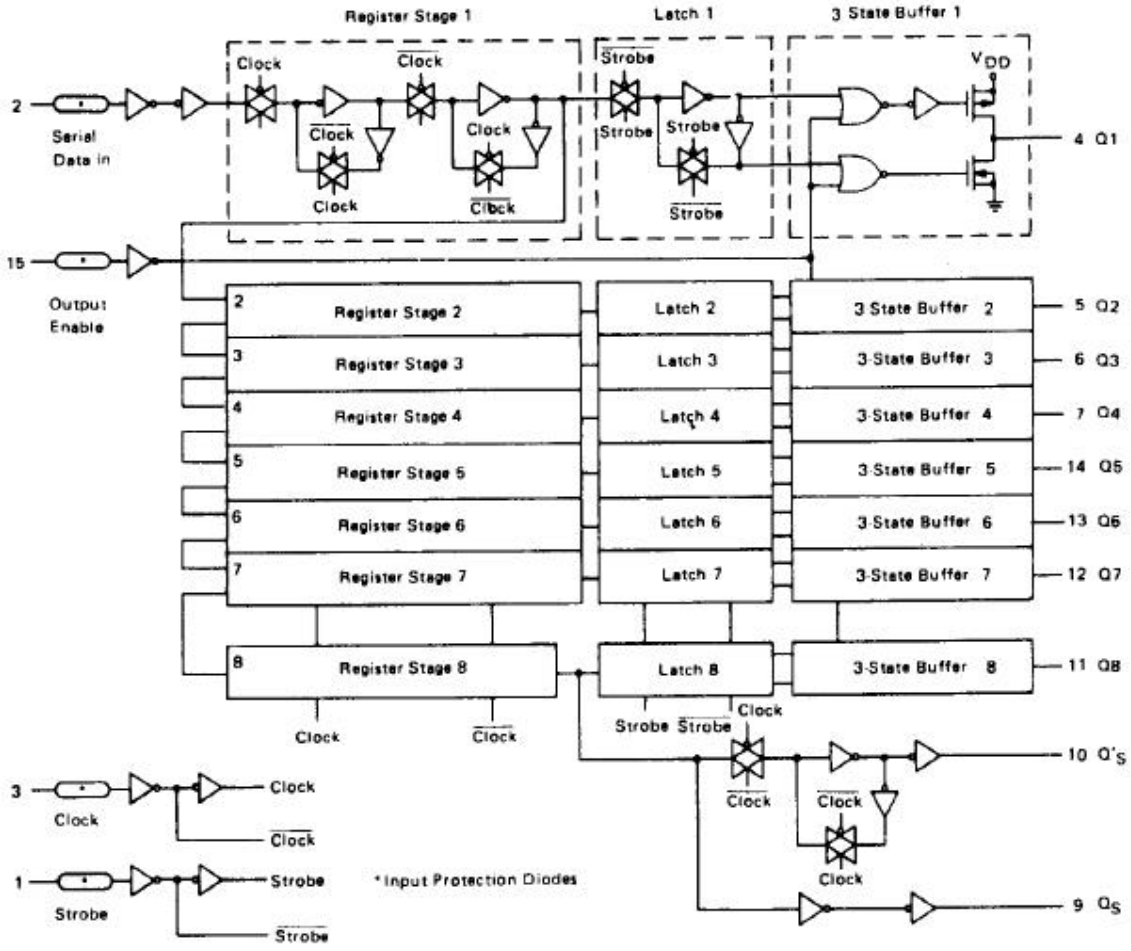
Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM