National Semiconductor

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LP2966
Dual 150mA Ultra Low-Dropout Regulator

General Description

The LP2966 dual ultra low-dropout (LDO) regulator operates from a +2.70V to +7.0V input supply. Each output delivers 150mA over full temperature range. The IC operates with extremely low drop-out voltage and quiescent current, which makes it very suitable for battery powered and portable applications. Each LDO in the LP2966 has independent shutdown capability. The LP2966 provides low noise performance with low ground pin current in an extremely small MSOP-8 package (refer to package dimensions and connection diagram for more information on MSOP-8 package). A wide range of preset voltage options are available for each output. In addition to the voltage combinations listed in the ordering information table, many more are available upon request with minimum orders. In all, 256 voltage combinations are possible.

Key Specifications

Dropout Voltage: Varies linearly with load current. Typically 0.9 mV at 1mA load current and 135mV at 150mA load current.

Ground Pin Current: Typically 300µA at 1mA load current and 340µA at 100mA load current (with one shutdown pin pulled low).

Shutdown Mode: Less than 1µA quiescent current when both shutdown pins are pulled low.

Error Flag: Open drain output, goes low when the corresponding output drops 10% below nominal.

Precision Output Voltage: Multiple output voltage options available ranging from 1.8V to 5.0V with a guaranteed accuracy of ±1% at room temperature.

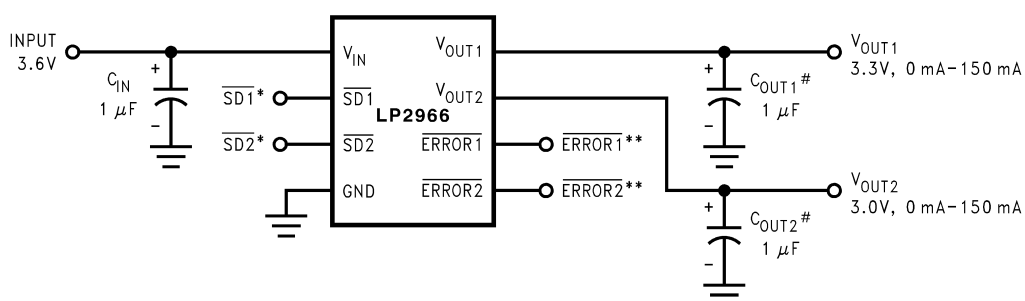
Features

- Ultra low drop-out voltage
- Low ground pin current
- <1µA quiescent current in shutdown mode
- Independent shutdown of each LDO regulator
- Output voltage accuracy ±1%
- Guaranteed 150mA output current at each output
- Low output noise
- Error Flags indicate status of each output
- Available in MSOP-8 surface mount packages
- Low output capacitor requirements (1µF)
- Operates with Low ESR ceramic capacitors in most applications
- Over temperature/over current protection
- -40˚C to +125˚C junction temperature range

Applications

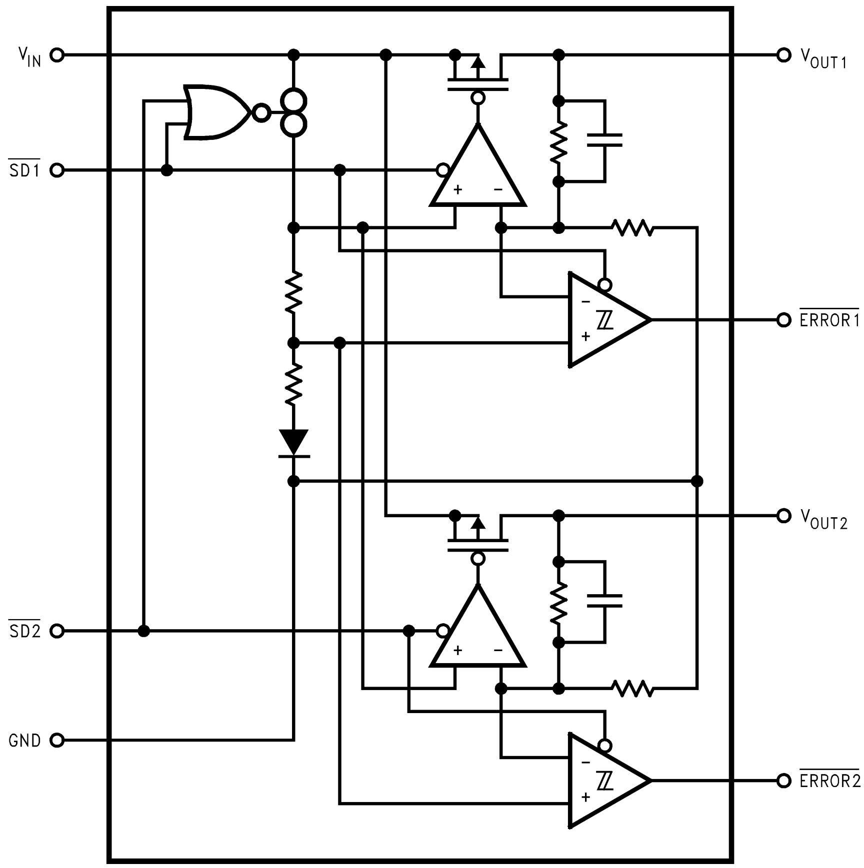
- Cellular and Wireless Applications
- Palmtop/Laptop Computer
- GPS systems
- Flat panel displays
- Post regulators
- USB applications
- Hand held equipment and multimeters
- Wireless data terminals
- Other battery powered applications

Typical Application Circuit



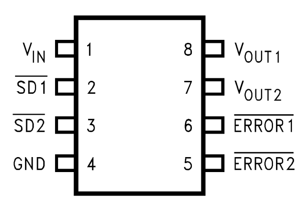
*SD1 and SD2 must be actively terminated through a pull up resistor. Tie to V_{IN} if not used.
**ERROR1 and ERROR2 are open drain outputs. These pins must be connected to ground if not used.
Minimum output capacitance is 1µF to insure stability over full load current range. More capacitance improves superior dynamic performance and provides additional stability margin.

Block Diagram



DS100850-31

Connection Diagram



DS100850-32

Top View
Mini SO-8 Package
8-Lead Small Outline Integrated Circuit (SOIC)
Package Code: MSOP-8

Pin Description

Pin	Name	Function
1	VIN	Input Supply pin
2	$\overline{SD1}$	Active low shutdown pin for output 1
3	$\overline{SD2}$	Active low shutdown pin for output 2
4	GND	Ground
5	$\overline{ERROR2}$	Error flag for output 2 - Normally high impedance, should be connected to ground if not used.
6	$\overline{ERROR1}$	Error flag for output 1 - Normally high impedance, should be connected to ground if not used.
7	VOUT2	Output 2
8	VOUT1	Output 1

Ordering Information

The following voltage options and their combinations are possible.

5.0V, 4.0V, 3.8V, 3.6V, 3.3V, 3.2V, 3.1V, 3.0V, 2.9V, 2.8V, 2.7V, 2.6V, 2.5V, 2.4V, 2.0V and 1.8V

TABLE 1.

Output Voltage 1	Output Voltage 2	Order Number	Package Marking	Supplied As:
5.0	5.0	LP2966IMM-5050	LAFB	1000 units on tape and reel
5.0	5.0	LP2966IMMX-5050	LAFB	3500 units on tape and reel
3.6	3.6	LP2966IMM-3636	LAEB	1000 units on tape and reel
3.6	3.6	LP2966IMMX-3636	LAEB	3500 units on tape and reel
3.3	3.6	LP2966IMM-3336	LAHB	1000 units on tape and reel
3.3	3.6	LP2966IMMX-3336	LAHB	3500 units on tape and reel
3.3	3.3	LP2966IMM-3333	LADB	1000 units on tape and reel
3.3	3.3	LP2966IMMX-3333	LADB	3500 units on tape and reel
3.3	2.5	LP2966IMM-3325	LARB	1000 units on tape and reel
3.3	2.5	LP2966IMMX-3325	LARB	3500 units on tape and reel
3.0	3.0	LP2966IMM-3030	LACB	1000 units on tape and reel
3.0	3.0	LP2966IMMX-3030	LACB	3500 units on tape and reel
2.8	3.0	LP2966IMM-2830	LASB	1000 units on tape and reel
2.8	3.0	LP2966IMMX-2830	LASB	3500 units on tape and reel
2.8	2.8	LP2966IMM-2828	LABB	1000 units on tape and reel
2.8	2.8	LP2966IMMX-2828	LABB	3500 units on tape and reel
2.5	2.5	LP2966IMM-2525	LAAB	1000 units on tape and reel
2.5	2.5	LP2966IMMX-2525	LAAB	3500 units on tape and reel
1.8	3.3	LP2966IMM-1833	LCFB	1000 units on tape and reel
1.8	3.3	LP2966IMMX-1833	LCFB	3500 units on Tape and reel
1.8	1.8	LP2966IMM-1818	LA9B	1000 units on tape and reel
1.8	1.8	LP2966IMMX-1818	LA9B	3500 units on tape and reel

The voltage options and combinations shown in *Table 1* **are available. For other custom voltage options or combinations of voltage options, please contact your nearest National Semiconductor Sales Office.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65 to +150˚C
Lead Temp. (Soldering, 5 sec.)	260˚C
Power Dissipation (Note 2)	Internally Limited
ESD Rating (Note 3)	2kV
Input Supply Voltage (Survival)	−0.3V to 7.5V
Shutdown Input Voltage (Survival)	−0.3V to (Vin + 0.3V)
Maximum Voltage for $\overline{ERROR}$ Pins	10V
I_{OUT} (Survival)	Short Circuit Protected
Output Voltage (Survival)(Note 6), (Note 7)	−0.3V to (Vin + 0.3V)

Operating Ratings (Note 1)

Input Supply Voltage	2.7V to 7.0V
Shutdown Input Voltage	−0.3V to (Vin + 0.3V)
Operating Junction Temperature Range	−40˚C to +125˚C
Maximum Voltage for $\overline{ERROR}$ pins	10V

Electrical Characteristics

Limits in standard typeface are for T_j = 25˚C, and limits in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified, $V_{IN} = V_{O(NOM)}$ + 1V, (Note 16), C_{OUT} = 1µF, I_{OUT} = 1mA, C_{IN} = 1µF, $V_{SD1} = V_{SD2} = V_{IN}$.

Symbol	Parameter	Conditions	Typ (Note 4)	LP2966IMM (Note 5)		Unit
				Min	Max	
V_o (Note 13)	Output Voltage Tolerance	V_{OUT} + 1V < V_{IN} < 7.0V	0.0	−1 **-3**	1 **3**	$\%V_{NOM}$
		1mA < I_L < 100mA	0.0	−1.5 **-3.5**	1.5 **3.5**	$\%V_{NOM}$
$\Delta V_O/\Delta V_{IN}$ (Note 8) (Note 13)	Output Voltage Line Regulation		0.1			mV/V
$\Delta V_O/\Delta I_{OUT}$	Output Voltage Load Regulation (Note 9)	1mA < I_L< 100mA (Note 9)	0.1			mV/mA
$\Delta V_{O2}/\Delta I_{OUT1}$	Output Voltage Cross Regulation (Note 10)	1mA < I_{L1}< 100mA (Note 10)	0.0004			mV/mA
V_{IN} -V_{OUT}	Dropout Voltage (Note 12)	I_L = 1mA	0.9		2.0 **3.0**	mV
		I_L = 100mA	90		130 **180**	
		I_L = 150mA	135		195 **270**	
$I_{GND(1,0)}$(Note 18)	Ground Pin Current (One LDO On)	I_L = 1mA $V_{SD2} \leq 0.1V$, $V_{SD1}= V_{IN}$	**300**			µA
		I_L = 100mA $V_{SD2} \leq 0.1V$, $V_{SD1}= V_{IN}$	**340**			
$I_{GND(1,1)}$	Ground Pin Current (Both LDOs On)	I_L = 1mA	340		450 **500**	µA
		I_L = 100mA	420		540 **600**	
$I_{GND(0,0)}$	Ground Pin Current in Shutdown Mode	$V_{SD1}= V_{SD2} \leq 0.1V$	0.006		0.3 **10**	µA
$I_{O(PK)}$	Peak Output Current	(Note 2) $V_{OUT} \geq V_{OUT(NOM)}$- 5%	500	350 **150**		mA
Short Circuit Foldback Protection						
I_{FB}	Short Circuit Foldback Knee	(Note 2), (Note 14)	600			mA

Electrical Characteristics (Continued)

Limits in standard typeface are for T_j = 25˚C, and limits in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified, $V_{IN} = V_{O(NOM)}$ + 1V, (Note 16), C_{OUT} = 1µF, I_{OUT} = 1mA, C_{IN} = 1µF, $V_{SD1} = V_{SD2} = V_{IN}$.

Symbol	Parameter	Conditions	Typ (Note 4)	LP2966IMM (Note 5)		Unit
				Min	Max	
Over Temperature Protection						
Tsh(t)	Shutdown Threshold		165			˚C
Tsh(h)	Thermal Shutdown Hysteresis		25			˚C
Shutdown Input						
V_{SDT}	Shutdown Threshold (Note 15)	Output = Low	0		**0.1**	V
		Output = High	V_{IN}	**V_{IN} - 0.1**		
T_{dOFF}	Turn-off Delay (Note 17)	I_L = 100 mA	20			µsec
T_{dON}	Turn-on Delay (Note 17)	I_L = 100 mA	25			µsec
I_{SD}	SD Input Current	$V_{SD} = V_{IN}$	1			nA
		V_{SD} = 0 V	1			
Error Flag Comparators						
V_T	Threshold (output goes high to low)	(Note 11)	10	**5**	**16**	%
V_{TH}	Threshold Hysteresis	(Note 11)	5	**2**	**8**	%
$V_{ERR(Sat)}$	Error Flag Saturation	I_{Fsink} = 100µA	0.015		**0.1**	V
$I_{EF(leak)}$	Error Flag Pin Leakage Current		1			nA
$I_{(EFsink)}$	Error Flag Pin Sink Current		1			mA
AC Parameters						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1V, f = 120Hz, V_{OUT} = 3.3V	60			dB
		$V_{IN} = V_{OUT}$ + 0.3V, f = 120Hz, V_{OUT} = 3.3V	40			
ρn(1/f)	Output Noise Density	f =120Hz	1			µV/√Hz
e_n	Output Noise Voltage (rms)	BW = 10Hz − 100kHz, C_{OUT} = 10µF	150			µV(rms)
		BW = 300Hz − 300kHz, C_{OUT} = 10µF	100			

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: At elevated temperatures, devices must be derated based on package thermal resistance. The device in the surface-mount package must be derated at θ_{jA} = 235˚C/W, junction-to-ambient. Please refer to the applications section on maximum current capability for further information. The device has internal thermal protection.

Note 3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 4: : Typical numbers are at 25˚C and represent the most likely parametric norm.

Note 5: : Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Averaging Outgoing Quality Level (AOQL).

Note 6: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2966 output must be diode-clamped to ground.

Note 7: The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} and V_{OUT} will turn on this diode.

Note 8: Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in input line voltage.

Note 9: Output voltage load regulation is defined as the change in output voltage from the nominal value when the load current changes from 1mA to 100mA.

Note 10: Output voltage cross regulation is defined as the percentage change in the output voltage from the nominal value at one output when the load current changes from 1mA to full load in the other output. This is an important parameter in multiple output regulators. The specification for $\Delta V_{O1}/\Delta I_{OUT2}$ is equal to the specification for $\Delta V_{O2}/\Delta I_{OUT1}$.

Note 11: Error Flag threshold and hysteresis are specified as the percentage below the regulated output voltage.

Note 12: Dropout voltage is defined as the input to output differential at which the output voltage drops 100mV below the nominal value. Drop-out voltage specification applies only to output voltages greater than 2.7V. For output voltages below 2.7V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.7V.

Note 13: Output voltage tolerance specification also includes the line regulation and load regulation.

Electrical Characteristics (Continued)

Note 14: LP2966 has fold back current limited short circuit protection. The knee is the current at which the output voltage drops 10% below the nominal value.

Note 15: V_{SDT} is the shutdown pin voltage threshold below which the output is disabled.

Note 16: The condition $V_{IN} = V_{O(NOM)} + 1V$ applies when Vout1 = Vout2. If Vout1 ≠ Vout2, then this condition would apply to the output which is greater in value. As an example, if Vout1 = 3.3V and Vout2 = 5V, then the condition $V_{IN} = V_{O(NOM)} + 1V$ would apply to Vout2 only.

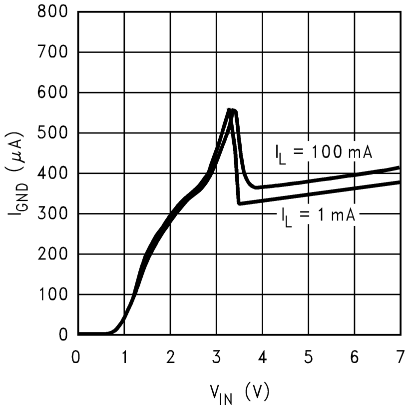
Note 17: Turn-on delay is the time interval between the low to high transition on the shutdown pin to the output voltage settling to within 5% of the nominal value. Turn-off delay is the time interval between the high to low transition on the shutdown pin to the output voltage dropping below 50% of the nominal value. The external load impedance influences the output voltage decay in shutdown mode.

Note 18: The limits for the ground pin current specification, $I_{GND(0,1)}$ will be same as the limits for the specification, $I_{GND(1,0)}$.

Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $V_{SD1} = V_{SD2} = V_{IN}$, and $T_A = 25^{\circ}C$.

Ground Pin Current vs Supply Voltage (one LDO on)



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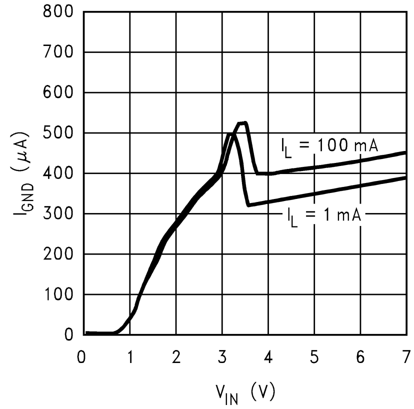
Ground Pin Current vs Supply Voltage (both LDOs on)



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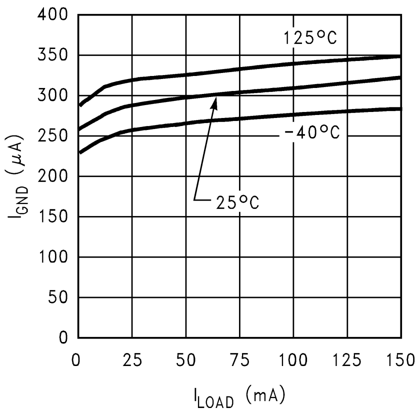
Ground Pin Current vs Load Current over temperature (one LDO on)



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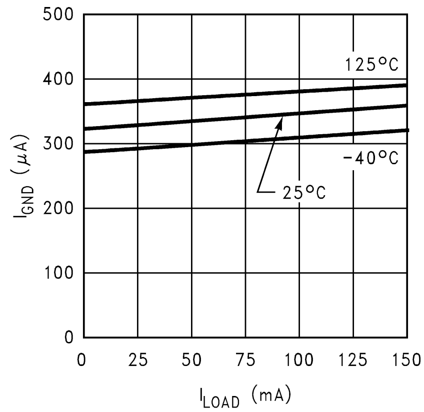
Ground Pin Current vs Load Current over temperature (both LDOs on)



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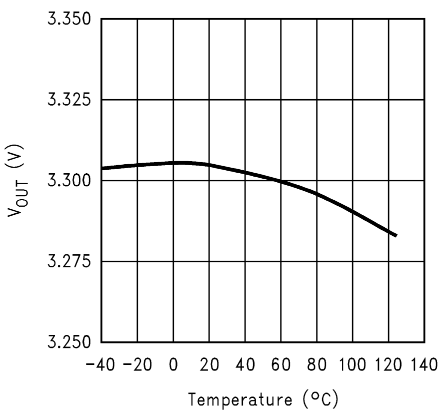
Output Voltage vs Temperature



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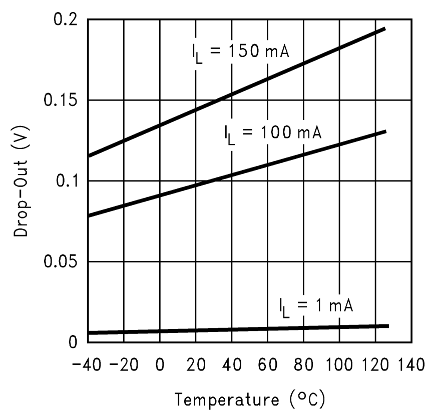
Drop-out Voltage vs Temperature

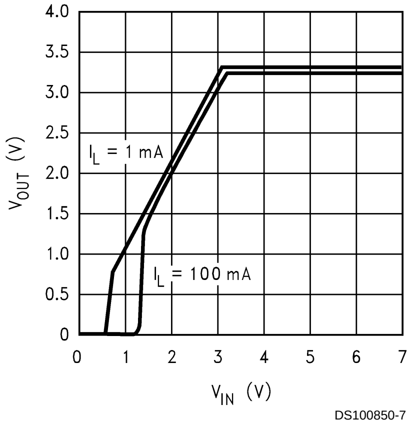


DS100850-6

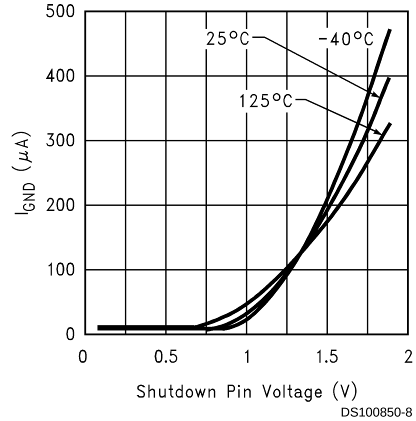
Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $V_{SD1} = V_{SD2} = V_{IN}$, and $T_A = 25^\circ C$. (Continued)

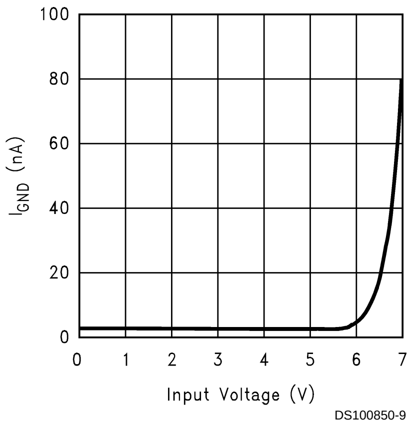
Input Voltage vs Output Voltage



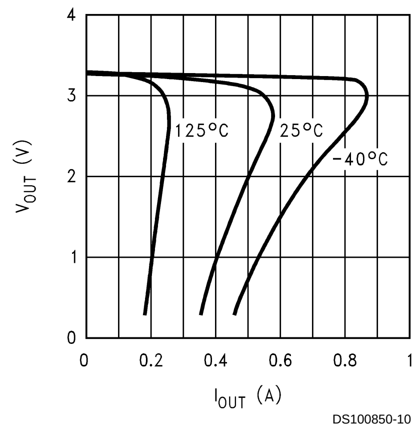
Ground Pin Current vs Shutdown Pin Voltage



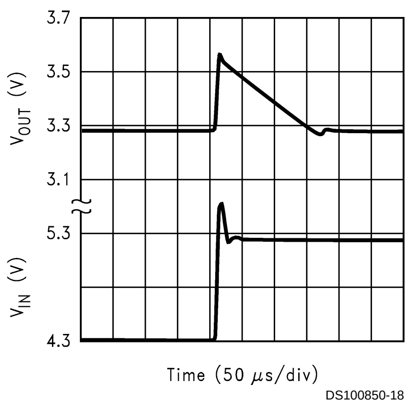
Ground Pin Current vs Input Voltage (Both LDOs off)



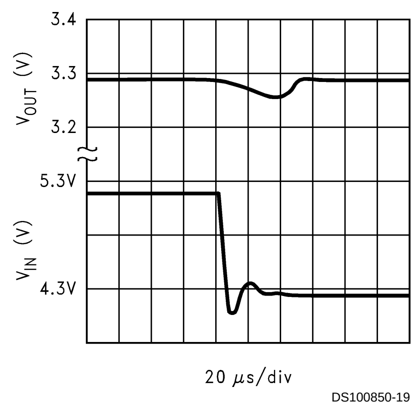
Short-Circuit Foldback Protection



Line Transient Response
($C_{OUT} = 2.2\mu F$, $I_{OUT} = 1mA$)



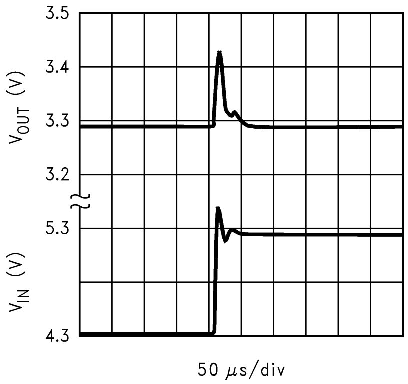
Line Transient Response
($C_{OUT} = 2.2\mu F$, $I_{OUT} = 1mA$)



Typical Performance Characteristics

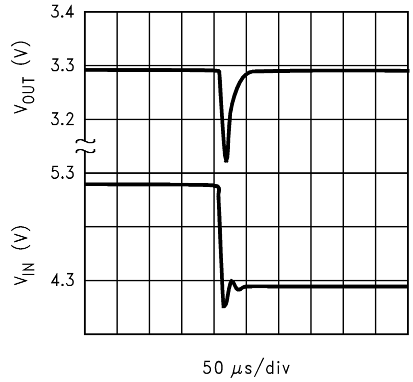
Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $V_{SD1} = V_{SD2} = V_{IN}$, and $T_A = 25^{\circ}C$. (Continued)

Line Transient Response (C_{OUT} = 2.2µF, I_{OUT} = 100mA)



DS100850-20

Line Transient Response (C_{OUT} = 2.2µF, I_{OUT} = 100mA)



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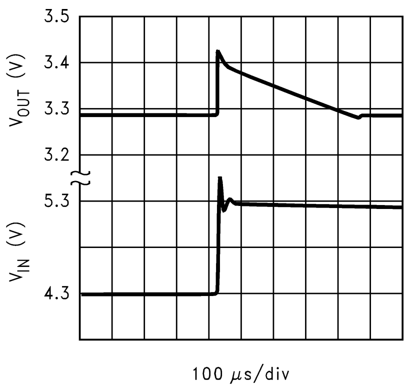
Line Transient Response (C_{OUT} = 10µF, I_{OUT} = 1mA)



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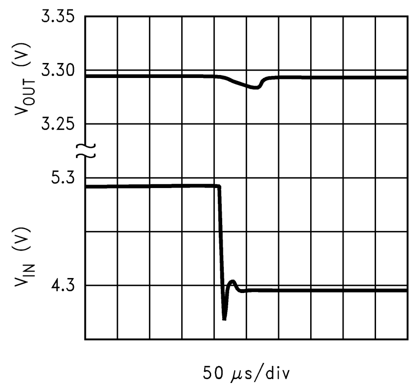
Line Transient Response (C_{OUT} = 10µF, I_{OUT} = 1mA)



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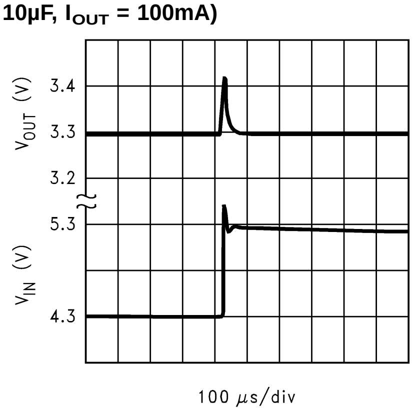
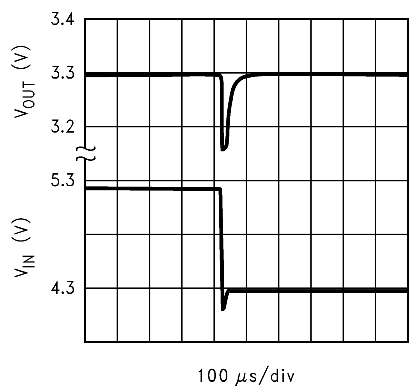
Line Transient Response (C_{OUT} = 10µF, I_{OUT} = 100mA)



DS100850-25

Line Transient Response (C_{OUT} = 10µF, I_{OUT} = 100mA)



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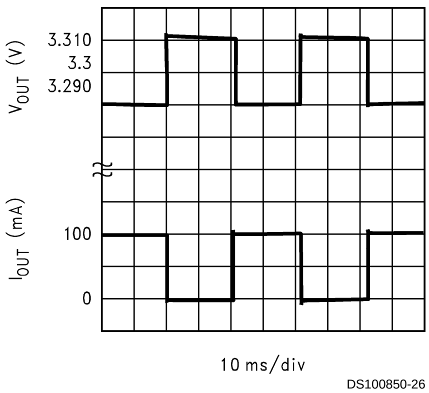
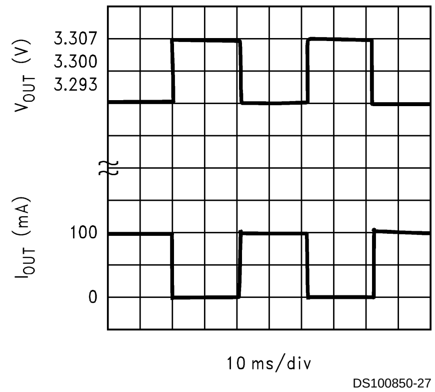
Typical Performance Characteristics

Unless otherwise specified, V_{IN} =$V_{O(NOM)}$ + 1V, V_{OUT}= 3.3V, C_{OUT} =1µF, I_{OUT} = 1mA, C_{IN} =1µF, V_{SD1} = V_{SD2} = V_{IN}, and T_A = 25˚C. (Continued)

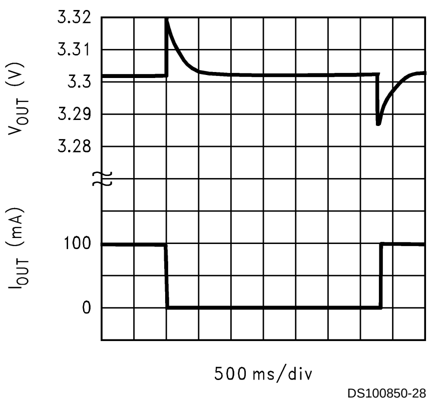
Load Transient Response (C_{OUT} = 2.2µF)



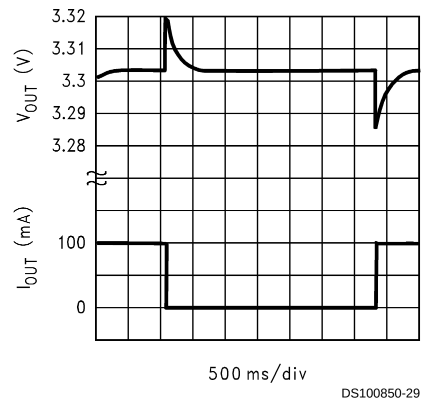
Load Transient Response (C_{OUT} = 10µF)



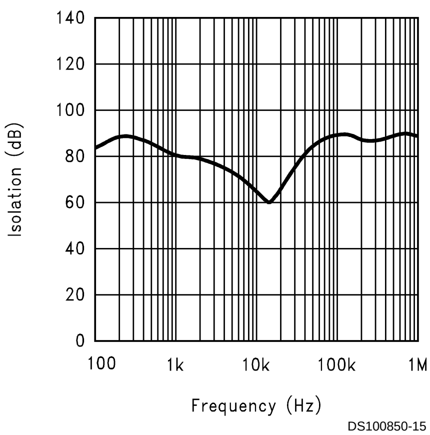
Load Transient Response (C_{OUT} = 10µF)



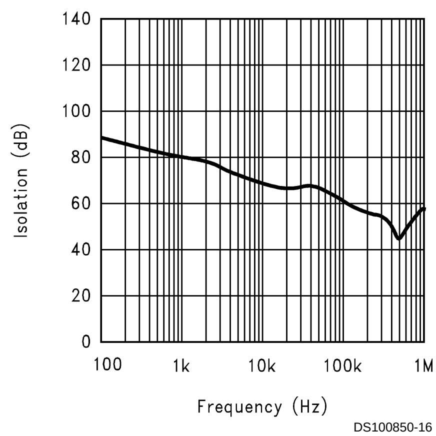
Load Transient Response (C_{OUT} = 2.2µF)



Cross-Channel Isolation vs Frequency (I_{OUT1} =1mA, I_{OUT2} = 1mA)



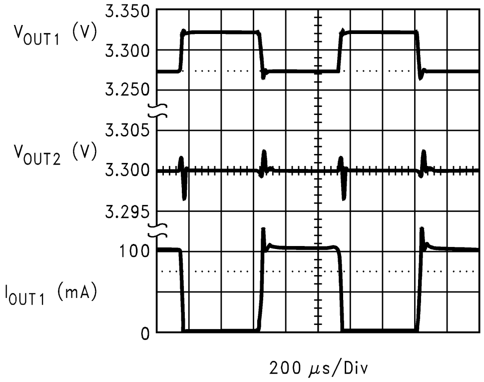
Cross-Channel Isolation vs Frequency (I_{OUT1} = I_{OUT2} = 100mA)



Typical Performance Characteristics

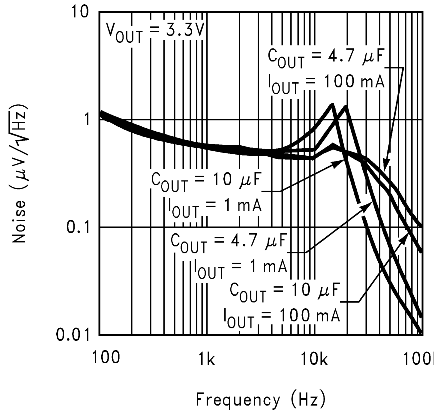
Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $V_{SD1} = V_{SD2} = V_{IN}$, and $T_A = 25°C$. (Continued)

Output Voltage Cross-Coupling



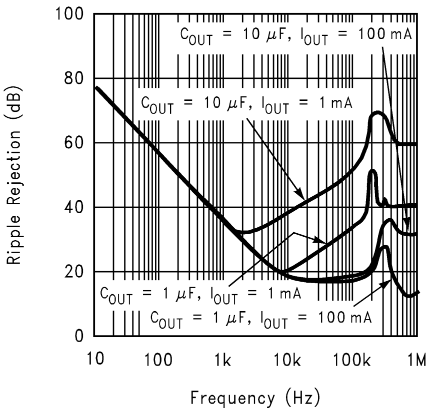
DS100850-13

Output Noise Density



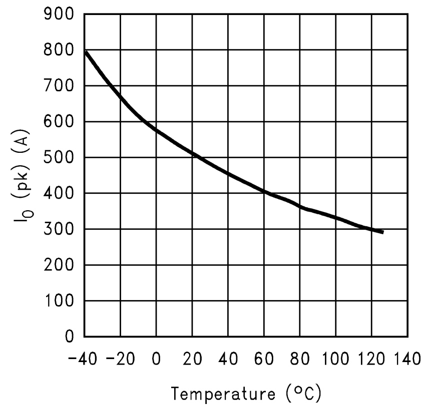
DS100850-14

Power Supply Ripple Rejection



DS100850-17

Peak Output Current vs Temperature



DS100850-41

Applications Information

Input Capacitor Selection

LP2966 requires a minimum input capacitance of 1µF between the input and ground pins to prevent any impedance interactions with the supply. This capacitor should be located very close to the input pin. This capacitor can be of any type such as ceramic, tantalum, or aluminium. Any good quality capacitor which has good tolerance over temperature and frequency is recommended.

Output Capacitor Selection

The LP2966 requires a minimum of 1µF capacitance on each output for proper operation. To insure stability, this capacitor should maintain its ESR (equivalent series resistance) in the stable region of the ESR curves (*Figure 1* and *Figure 2* over the full operating temperature range of the application. The output capacitor should have a good tolerance over temperature, voltage, and frequency. The output capacitor can be increased without limit. Larger capacitance provides better stability and noise performance. The output capacitor should be connected very close to the Vout pin of the IC.

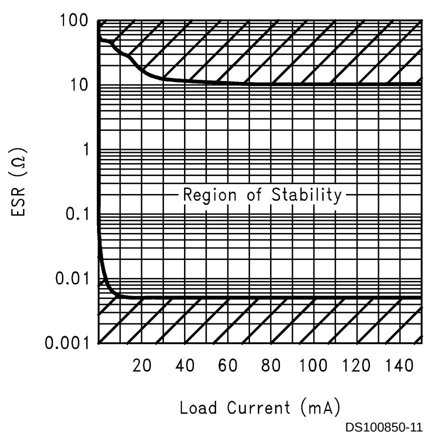


FIGURE 1. ESR Curve for V_{OUT} = 5V and C_{OUT} = 2.2µF

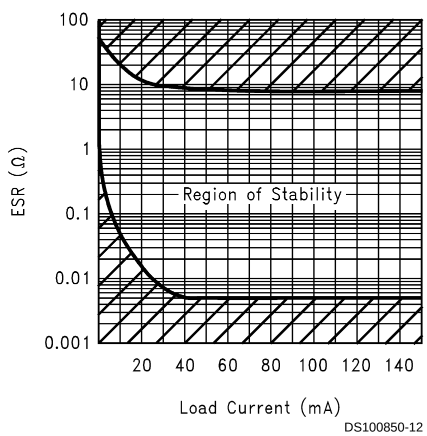


FIGURE 2. ESR Curve for V_{OUT} = 3.3V and C_{OUT} = 2.2µF

LP2966 works best with Tantalum capacitors. However, the ESR and the capcitance value of these capacitors vary a lot with temperature, voltage, and frequency. So while using Tantalum capacitors, it should be ensured that the ESR is within the limits for stability over the full operating tempararture range.

For output voltages greater than 2.5V, good quality ceramic capacitors (such as the X7R series from Taiyoyuden) can also be used with LP2966 in applications not requiring light load operation (< 5mA for the 5V output option). Once again, it should be ensured that the capacitance value and the ESR are within the limits for stability over the full operating temperature range.

The ESRD Series Polymer Aluminium Electrolytic capacitors from Cornell Dubilier are very stable over temperature and frequency. The excellent capacitance and ESR tolerance of these capacitors over voltage, temperature and frequency make these capacitors very suitable for use with LDO regulators.

Output Noise

Noise is specified in two ways-

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output Noise or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/√Hz or nV/√Hz and total output noise is measured in µV(rms).

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which storngly depend on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will increase the die size and decreases the chance of fitting the die into a small package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current) of the IC. Using an optimized trade-off of ground pin current and die size, LP2966 achieves low noise performance with low quiescent current in an MSOP-8 package.

Short-Circuit Foldback protection

In the presence of a short or excessive load current condition, the LP2966 uses an internal short circuit foldback mechanism that regulates the maximum deliverable output current. A strong negative temperature coefficient is designed into the circuit to enable extremely higher peak output current capability (in excess of 400mA per output at room temperature, see typical curves). Thus, a system designer using the LP2966 can achieve higher peak output current capability in applications where the LP2966 internal junction temperature is kept below 125˚C. Refer to the applications section on calculating the maximum output current capability of the LP2966 for your application.

Error Flag Operation

The LP2966 produces a logic low signal at the Error Flag pin ($\overline{ERROR}$) when the corresponding output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in Hysteresis. The timing diagram in *Figure 3* shows the relationship between the $\overline{ERROR}$ and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

Applications Information (Continued)

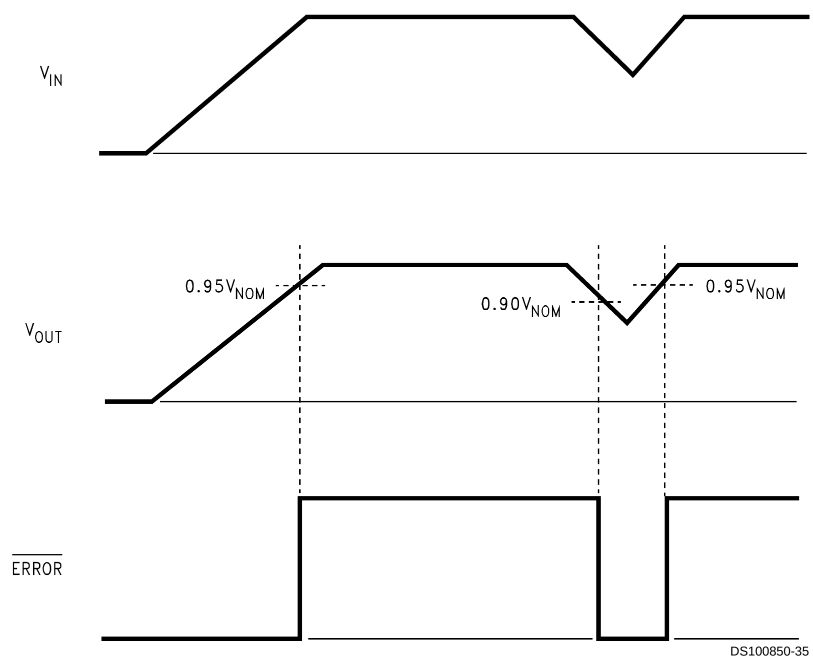


FIGURE 3. Error Flag Operation

The internal error flag comparators have open drain output stages. Hence, the $\overline{ERROR}$ pins should be pulled high through a pull up resistor. Although the $\overline{ERROR}$ pin can sink current of 1mA, this current adds to the battery drain. Hence, the value of the pull up resistor should be in the range of 100kΩ to 1MΩ. **The $\overline{ERROR}$ pins must be connected to ground if this function is not used.** It should also be noted that when the shutdown pins are pulled low, the $\overline{ERROR}$ pins are forced to be invalid for reasons of saving power in shutdown mode.

Shutdown Operation

The two LDO regulators in the LP2966 have independent shutdown. A CMOS Logic level signal at the shutdown($\overline{SD}$) pin will turn-off the corresponding regulator. Pins $\overline{SD1}$ and $\overline{SD2}$ must be actively terminated through a 100kΩ pull-up resistor for a proper operation. If these pins are driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. These pins must be tied to Vin if not used.

Drop-Out Voltage

The drop-out voltage of a regulator is defined as the minimum input-to-output differential required to stay within 100mV of the output voltage measured with a 1V differential. The LP2966 uses an internal MOSFET with an Rds(on) of 1Ω. For CMOS LDOs, the drop-out voltage is the product of the load current and the Rds(on) of the internal MOSFET.

Reverse Current Path

The internal MOSFET in the LP2966 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 150mA.

Maximum Output Current Capability

Each output in the LP2966 can deliver a current of more than 150mA over the full operating temperature range. However, the maximum output current capability should be derated by the junction temperature. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The LP2966 is available in MSOP-8 package. This package has a junction to ambient temperature coefficient (θ_{ja}) of 235 ˚C/W with minimum amount of copper area. The total power dissipation of the device is approximately given by:

$$P_D = (V_{in} - V_{OUT1})I_{OUT1} + (V_{in} - V_{OUT2})I_{OUT2}$$

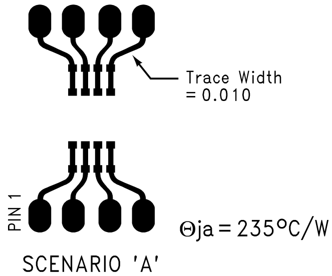
The maximum power dissipation, P_{Dmax}, that the device can tolerate can be calculated by using the formula

$$P_{Dmax} = (T_{jmax} - T_A)/\theta_{ja}$$

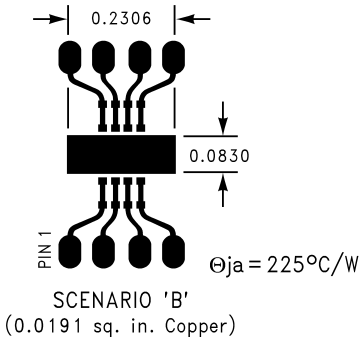
where T_{jmax} is the maximum specified junction temperature (125˚C), and T_A is the ambient temperature.

The following figures show the variation of thermal coefficient with different layout scenarios.

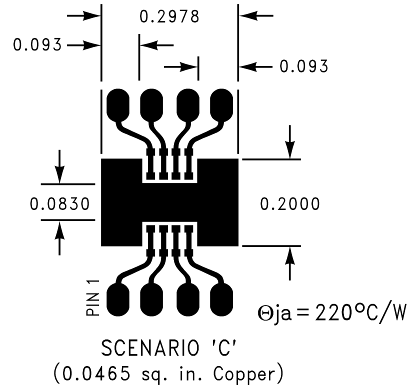
Applications Information (Continued)



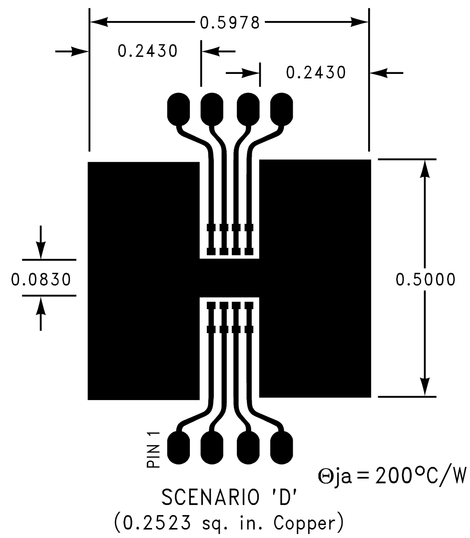
DS100850-36



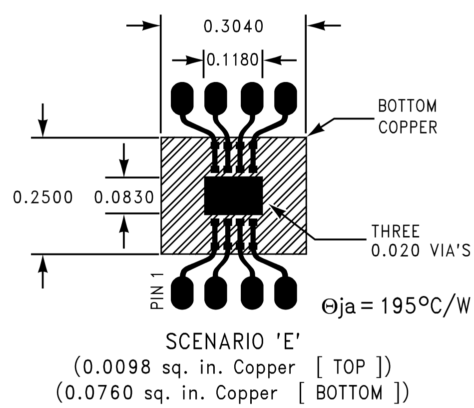
DS100850-37



DS100850-38



DS100850-39



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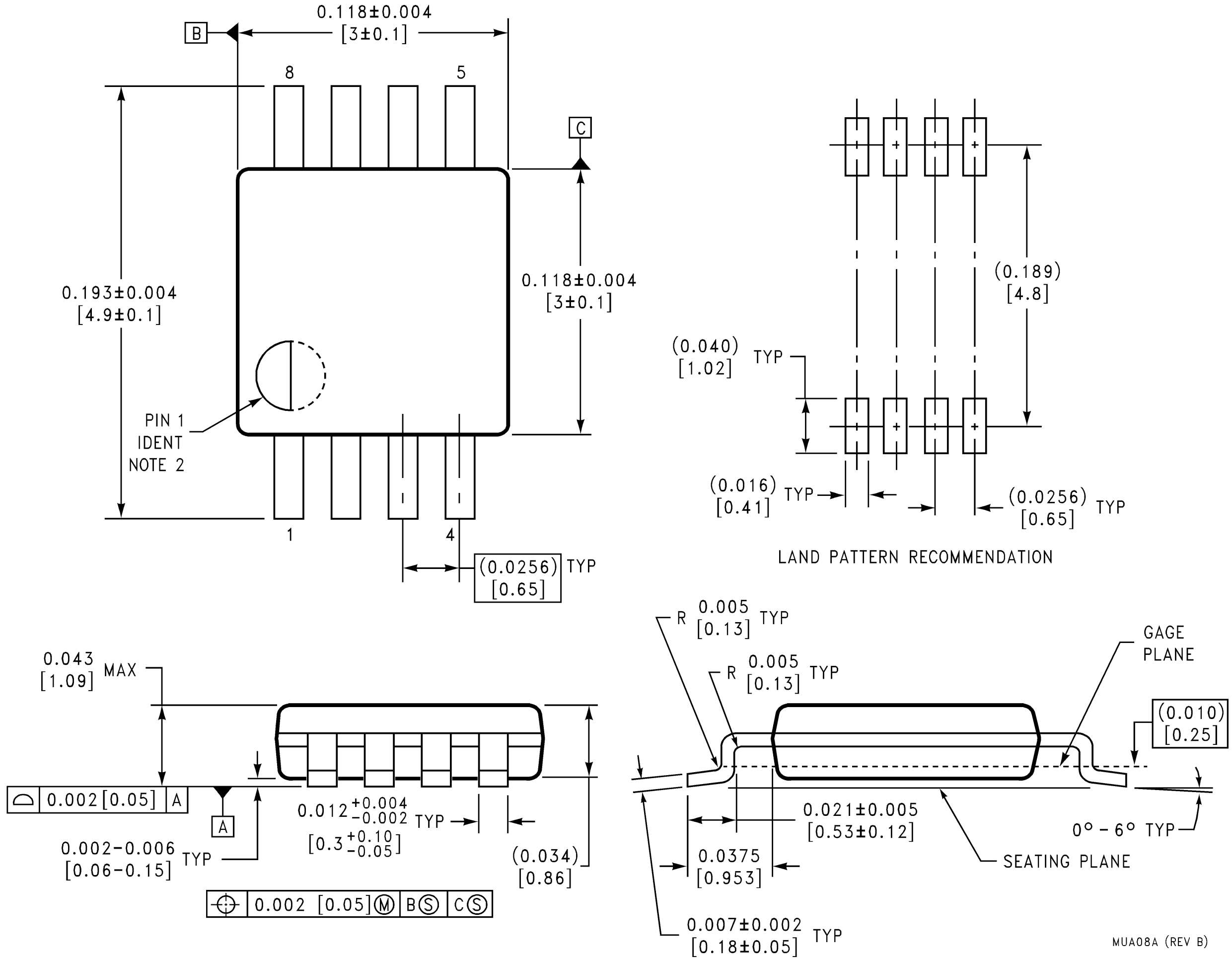
Physical Dimensions inches (millimeters) unless otherwise noted



Mini SO-8 Package Type MM
For Ordering, Refer to Ordering Information Table
NS Package Number MUA08A

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