

74LCX126

Low Voltage Quad Buffer with 5V Tolerant Inputs and Outputs

General Description

The LCX126 contains four independent non-inverting buffers with 3-STATE outputs. Each output is disabled when the associated output-enable (OE) input is LOW. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX126 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 100V

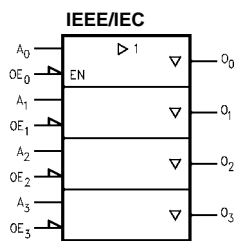
Note 1: To ensure the high-impedance state during power up or down, OE should be tied to GND through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

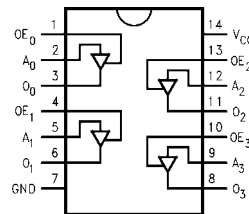
Order Number	Package Number	Package Description
74LCX126M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX126SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX126MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n	Inputs
OE_n	Output Enable Inputs
O_n	Outputs

Truth Table

Inputs		Output
OE_n	A_n	O_n
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

Absolute Maximum Ratings (Note 2)						
Symbol	Parameter	Value	Conditions	Units		
V _{CC}	Supply Voltage	-0.5 to +7.0		V		
V _I	DC Input Voltage	-0.5 to +7.0		V		
V _O	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V		
		-0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 3)	V		
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA		
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA		
		+50	V _O > V _{CC}	mA		
I _O	DC Output Source/Sink Current	±50		mA		
I _{CC}	DC Supply Current per Supply Pin	±100		mA		
I _{GND}	DC Ground Current per Ground Pin	±100		mA		
T _{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 4)						
Symbol	Parameter	Min	Max	Units		
V _{CC}	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
V _I	Input Voltage	0	5.5	V		
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}	V	
		3-STATE	0	5.5		
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V		±24	mA	
		V _{CC} = 2.7V – 3.0V		±12		
		V _{CC} = 2.3V – 2.7V		±8		
T _A	Free-Air Operating Temperature	-40	85	°C		
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V		
<p>Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 3: I_O Absolute Maximum Rating must be observed.</p> <p>Note 4: Unused inputs or I/Os must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 – 3.6	V _{CC} - 0.2		V
		I _{OH} = -8 mA	2.3	1.8		
		I _{OH} = -12 mA	2.7	2.2		
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 – 3.6		0.2	V
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 – 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units		
				Min	Max			
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		10	μA		
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 5)	2.3 – 3.6		±10			
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6V	2.3 – 3.6		500	μA		
Note 5: Outputs disabled or 3-STATE only.								
AC Electrical Characteristics								
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	5.5	1.5	6.0	1.5	6.6	ns
t _{PLH}		1.5	5.5	1.5	6.0	1.5	6.6	
t _{PZL}	Output Enable Time	1.5	6.0	1.5	7.0	1.5	7.8	ns
t _{PZH}		1.5	6.0	1.5	7.0	1.5	7.8	
t _{PLZ}	Output Disable Time	1.5	5.5	1.5	6.5	1.5	6.6	ns
t _{PHZ}		1.5	5.5	1.5	6.5	1.5	6.6	
t _{OSSL}	Output to Output Skew (Note 6)		1.0					ns
t _{OSLH}			1.0					
Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t _{OSSL}) or LOW-to-HIGH (t _{OSLH}).								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units			
				Typical				
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V			
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6				
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V			
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF				
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF				
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	25	pF				

AC Loading and Waveforms Generic for LCX Family

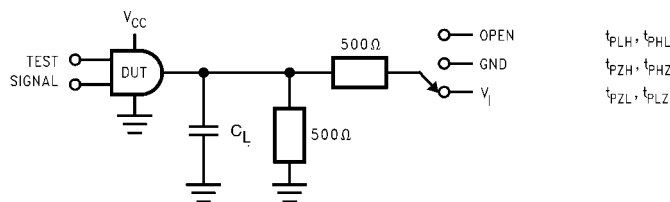
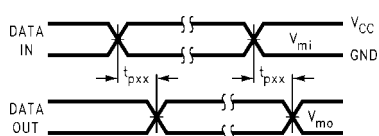
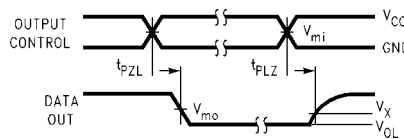


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

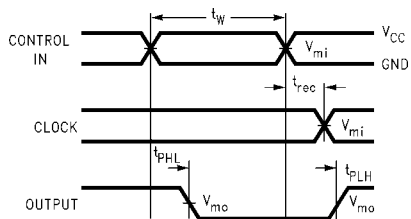
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



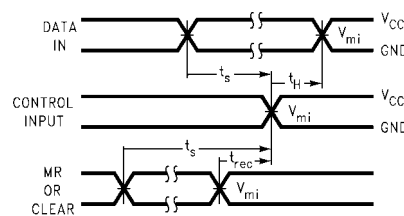
Waveform for Inverting and Non-Inverting Functions



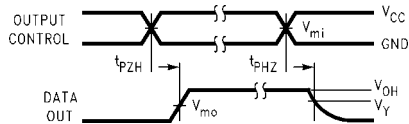
3-STATE Output Low Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output High Enable and Disable Times for Logic

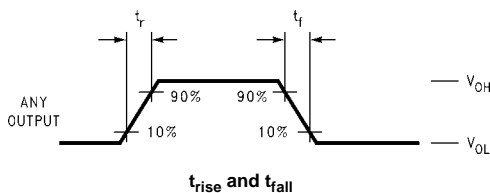


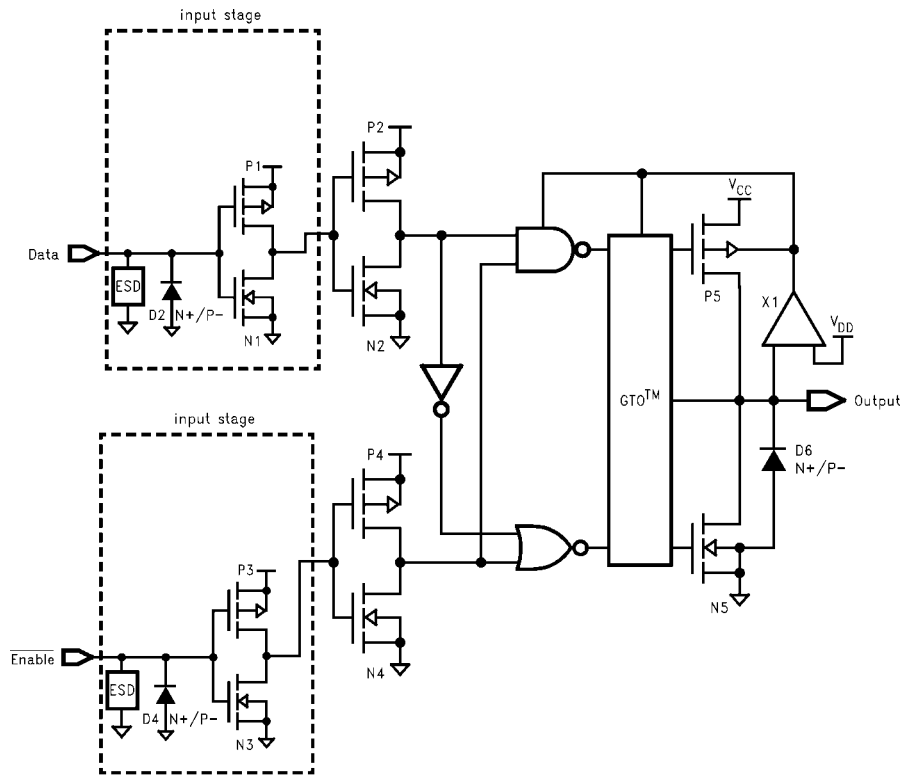
FIGURE 2. Waveforms

(Input Pulse Characteristics; $f = 1\text{MHz}$, $t_r = t_f = 3\text{ns}$)

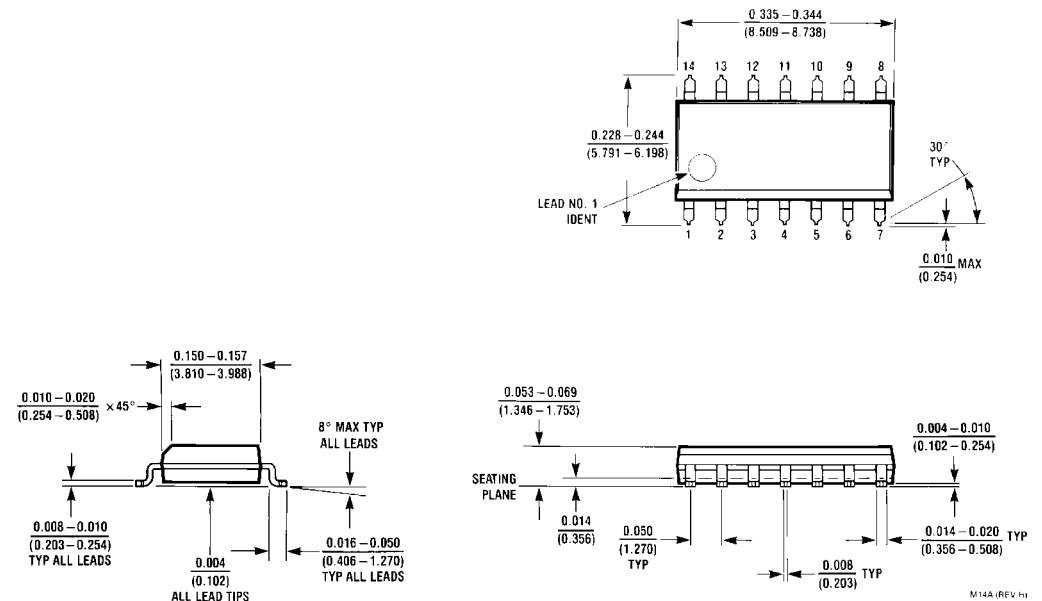
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

74LCX126

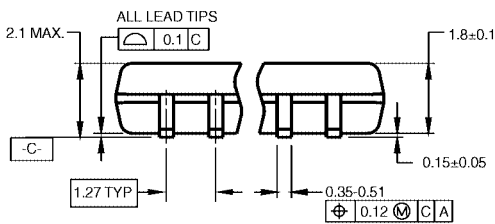
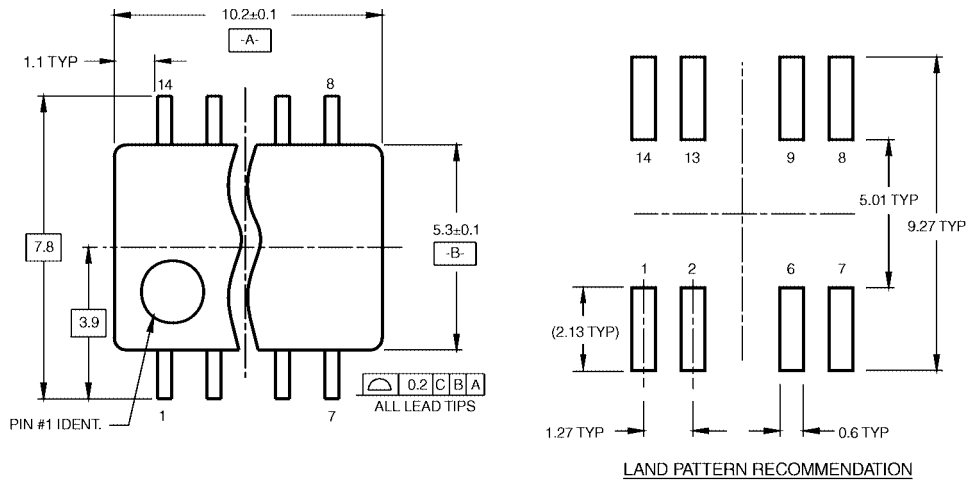


Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

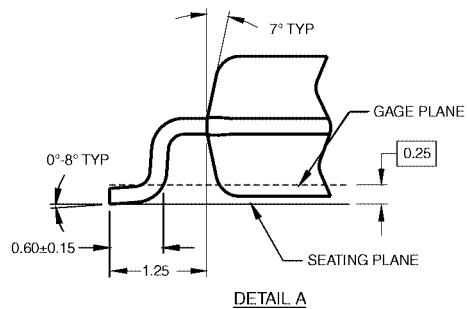
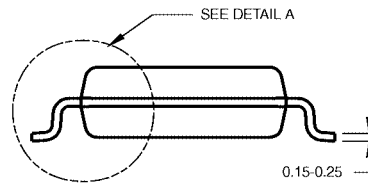


DIMENSIONS ARE IN MILLIMETERS

NOTES:

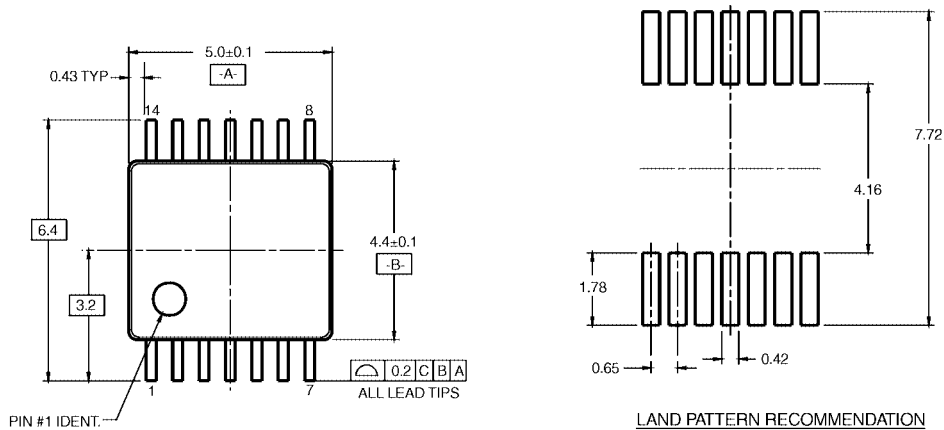
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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

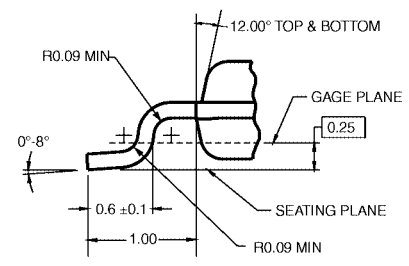
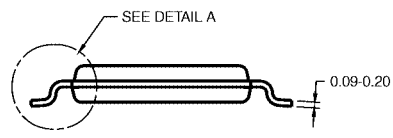
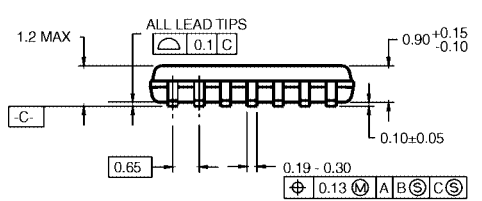


**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DETAIL A

- NOTES:
 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

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