Genlocking Sync Generator with Digital Audio Clock for NTSC, PAL & VGA

GENERAL DESCRIPTION

The ML6430/ML6431 are multi-standard single-chip BiCMOS video Genlock ICs for NTSC, PAL and VGA. They are designed to provide a stable clock from an analog video signal, and to provide timing pulses for clamping, decoding, blanking and processing video signals. The ML6430/ML6431 handle VCR glitches and variations created by head switching, tape dropouts, missing sync pulses, freeze frames, high speed playback and camcorder gyro errors. The ML6430/ML6431 are designed for high noise immunity, insensitivity to varying signal amplitudes, overmodulated color carriers, and sync glitches. Advanced analog and digital clock synthesis techniques provide multi-standard and non-standard operation from a single crystal or external asynchronous clock source. Pin selectable preset modes allow operation for most video standards in simple stand-alone mode without the necessity of using the serial bus. For more demanding applications, a two wire serial control bus is available for full control of all of the ML6430/ML6431 features.

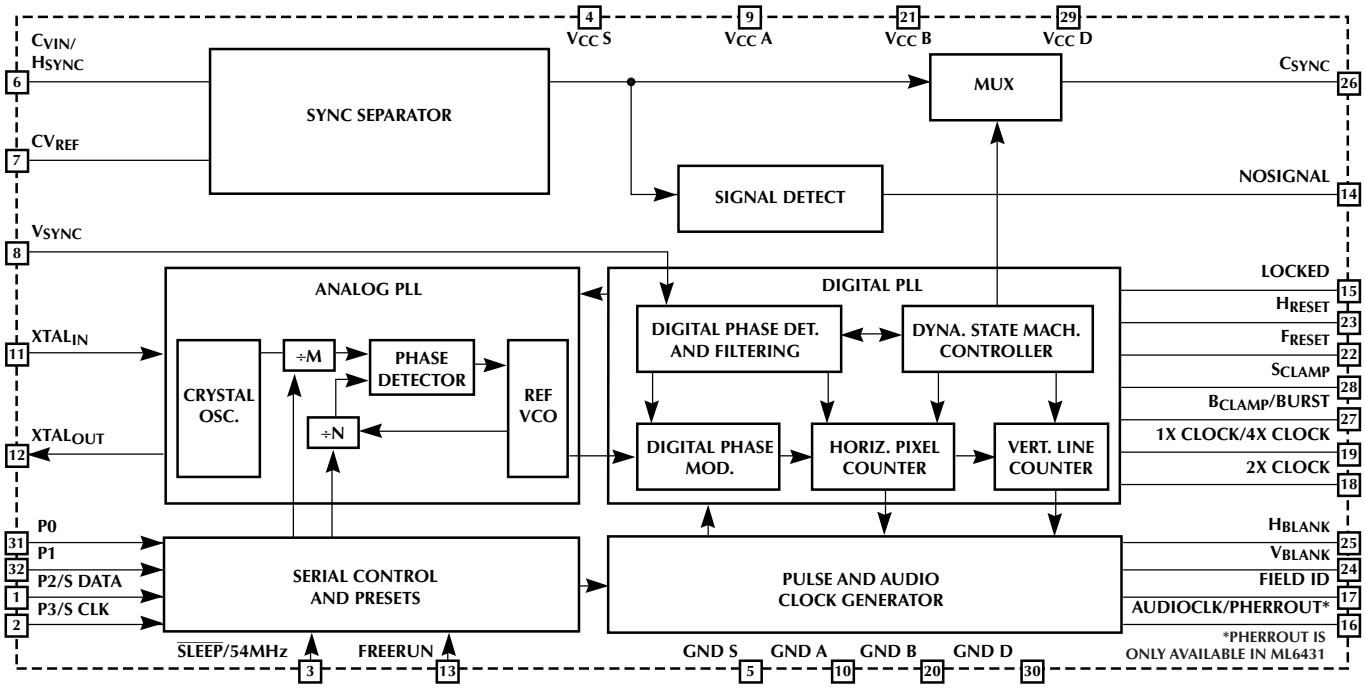
The ML6430/ML6431 are ideal for clock generation in MPEG encoders, high performance display timing, and video editing.

FEATURES

- Line locked scalable horizontal pixel clock for an arbitrary number of pixels per line
- Standard frequencies of 12.27, 13.5, 14.75MHz, or 4Fsc
- 4×/2× or 2×/1× clock outputs (54 and 27MHz, or 27 and 13.5MHz) and VGA clocks
- Audio clocks: 32, 44.1, or 48kHz, locked to video
- On-chip sync separator, VCO and pulse generator
- Low clock jitter: Short Term: <200ps rms locked
- Line to line: <600ps rms (2.2ns peak-to-peak) locked
- Fast recovery from VCR head switch, stable for fast shuttle speeds and pause
- Single crystal or external frequency source
- PAL, NTSC or VGA operation
- 2 wire serial control bus, or selectable presets for stand alone operation
- RS170A compatible

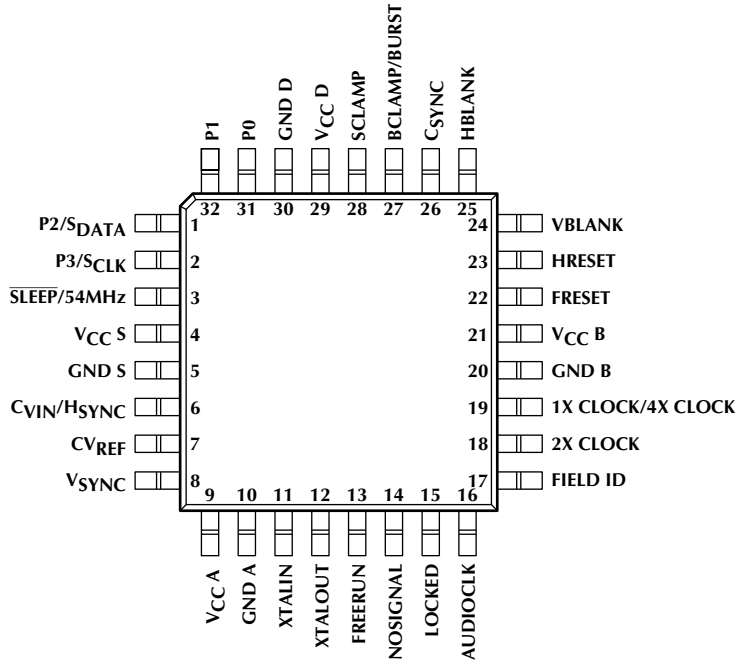
*** This Part Is End Of Life As Of August 1, 2000**

BLOCK DIAGRAM



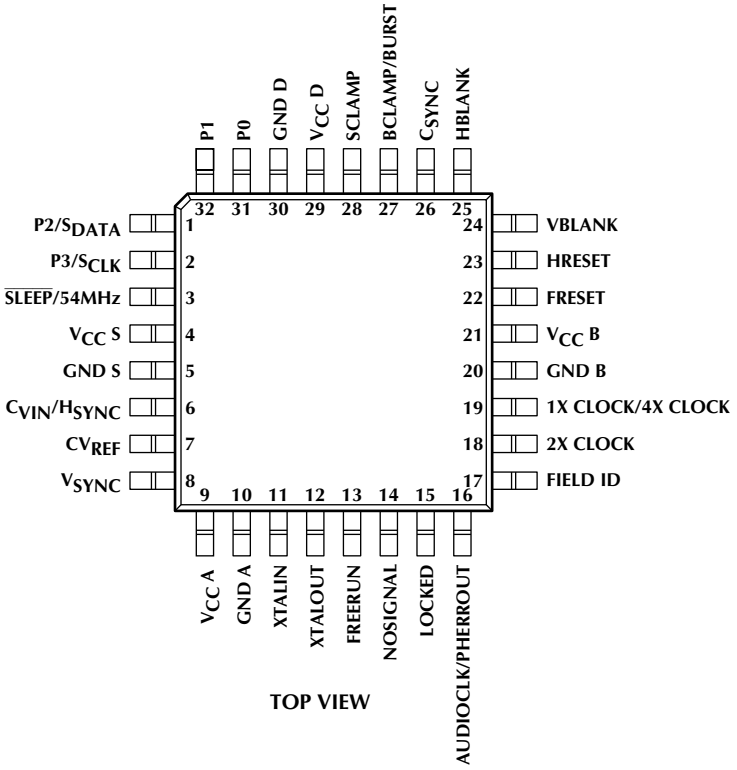
PIN CONFIGURATION

ML6430
32-Pin TQFP (H32-7)



TOP VIEW

ML6431
32-Pin TQFP (H32-7)



TOP VIEW

PIN DESCRIPTION (NOTE: ML6430 and ML6431 pin functions are identical *except* for pin 16. See below)

PIN	NAME	FUNCTION
1	P2/S_{DATA}	This is a dual function pin. If presets are enabled, refer to Table 7. If presets are disabled, serial bus data input.
2	P3/S_{CLK}	This is a dual function pin. If presets are enabled, refer to Table 7. If presets are disabled, serial bus clock input.
3	$\overline{SLEEP}$/54MHz	Hardware sleep mode: when low, disables entire chip for ultra-low power dissipation. Sleep mode can also be enabled/disabled via serial bus (Register 8). 54MHz is a clock input. This can be any 4X clock up to 70MHz used for pulse generation.
4	V_{CC} S	Analog supply for sync separator.
5	GND S	Analog ground for sync separator.
6	CV_{IN}/H_{SYNC}	Composite video input; video input in typical composite video applications, or Y input for YUV applications, or G input for RGB applications with sync on green. For typical VGA or other high performance display applications, this input may be supplied with a TTL level H_{SYNC} signal and the vertical sync input supplied with a TTL level V_{SYNC} signal.
7	CV_{REF}	Reference voltage for internal sync slicer. The external capacitor is driven by a charge pump to follow the sync tip.
8	V_{SYNC}	Vertical input for non-composite sources. This input may be supplied with a TTL level V_{SYNC} signal. For composite inputs this pin is tied high or low.
9	V_{CC} A	Analog supply pin for analog PLL.
10	GND A	Analog ground for analog PLL.
11	$XTAL_{IN}$	Crystal may be parallel tuned 3.58 MHz or 4.43MHz, or may be driven by an external oscillator at these frequencies, or at 4x these frequencies.
12	$XTAL_{OUT}$	Crystal drive pin. No connect if using external oscillator or clock.
13	FREERUN	Forces the PLL to run at a selected standard without syncing to a video signal. Accuracy is ±20ppm in FREERUN with ideal crystal, otherwise locked to video source
14	NOSIGNAL	Indicates video signal activity has not been detected at the composite input. If NOSIGNAL = low, this condition does not imply that lock has been established. The NOSIGNAL pin can be tied to FREERUN to create a local loop in which the genlock will not try to lock until a signal is detected at the input.
15	LOCKED	Indicates when digital PLL is locked to incoming video signal.
16	(ML6430) AUDIOCLK	Digital audio clock output. Programmable for 32kHz, 44.1kHz or 48kHz output.
16	(ML6431) AUDIOCLK/PHERROUT	This is a dual mode pin. Pin is selected via serial bus (Register 7). AUDIOCLK is an audio clock signal (see Table 9). PHERROUT indicates whether incoming HSYNC is ahead or behind output HSYNC.
17	FIELD ID	Field Flag: Odd = 1, Even = 0
18	2X CLOCK	2X oversampled PIXEL CLOCK & Output of Digital PLL. Nominal frequency of 27MHz
19	1X CLOCK/4X CLOCK	1X pixel clock. Nominal frequency of 13.5MHz or 54MHz ±20ppm in FREERUN with ideal crystal, otherwise locked to video source. PAL 4X CLOCK not available (no 4x4.4336MHz clock).
20	GND B	Digital ground for output driver buffers.
21	V_{CC} B	Digital supply for output driver buffers.
22	F_{RESET}	Frame reset; active low for one half line at the high to low transition of field ID. In NTSC mode, FRESET goes low on the high-to-low transition on the Field ID pin and at the beginning of line 1 (see Figure 2). In PAL mode, FRESET goes low on the high-to-low transition on the Field ID pin and at the end of line 310 (see Figure 3).

PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION
23	H_{RESET}	Horizontal reset; active low for one half pixel.
24	V_{BLANK}	Vertical blanking, active low
25	H_{BLANK}	Horizontal blanking, active low
26	C_{SYNC}	Composite sync output. May be either the raw output of sync slicer, or regenerated signal from internal pulse generators. If raw slicer output is selected, then signals disappear when input signal disappears. If regenerated output is selected, then signal is always present regardless of input conditions. Preset modes produce regenerated sync.
27	B_{CLAMP}/BURST	This is a dual mode pin. User may select either a back porch clamp pulse or a burst gate pulse via the serial control bus. Preset is B_{CLAMP} pulse.
28	S_{CLAMP}	Sync clamp pulse occurs just after leading edge of sync. Duration is typically less than 50% of sync pulse to avoid problems with equalizers in the vertical interval, active high.
29	V_{CC} D	Digital supply pin for digital PLL.
30	GND D	Digital ground pin for digital PLL.
31	P0	This is a three-state pin: low means serial bus is enabled, high or unconnected (high Z) means presets are active. Refer to Table 7.
32	P1	This is a three state pin. Refer to Table 7. If presets are disabled pin is ignored.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC Supply Voltage (V_{CC} A & V_{CC} D) ..... –0.3V to 7V
Analog & Digital Inputs/Outputs ... –0.3V to V_{CC} A + 0.3V
Input current per pin ..... ±25mA
Storage Temperature ..... – 65°C to 150°C
Junction Temperature ..... 125°C

OPERATING CONDITIONS

Supply Range ..... 4.5V to 5.5V
Temperature Range ..... 0°C to 70°C
Thermal Resistance ..... 80°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 4.5 to 5.5V and T_A = 0° to 70°C, C_{IN} = 0.1µF, C_{REF} = 0.1µF (Note 1).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
Supply Current (Analog and Digital)			80	120	mA
Analog Supply Current	V_{CC} A = V_{CC} D = 4.5		35		mA
Digital Supply Current	Max programmed clock rates		45		mA
DIGITAL INPUTS					
Low Level Input Voltage		0		0.8	V
High Level Input Voltage		V_{CC} – 0.8		V_{CC}	V
Low Level Input Current	V_{IN} = 0V + 0.1V			1.0	µA
High Level Input Current	V_{IN} = V_{CC} D – 0.1V			1.0	µA
Input Capacitance			2		pF
TTL INPUTS (H_{SYNC}, V_{SYNC})					
V_{IL} Input Low Voltage				0.8	V
V_{IH} Input High Voltage		2.0			V
THREE STATE DIGITAL INPUTS					
Low Level Input Voltage		0		0.8	V
High Level Input Voltage		V_{CC} – 0.8			V
Low Level Input Current	V_{IN} = 0V		50	150	µA
High Level Input Current	V_{IN} = V_{CC} D		50	150	µA
Input Capacitance			2		pF
Mid Level Input Voltage with 5V Supply		2		3	V
DIGITAL OUTPUTS					
Low Level Output Voltage		0		0.5	V
High Level Output Voltage		V_{CC} – 0.5			V
C_{LOAD} : Output Capacitance			50		pF
Output Disable Leakage				10	µA

GENLOCK PERFORMANCE SPECIFICATIONS

Unless otherwise noted, V_{IN} = 1 V_{PP} NTSC test signal for composite inputs, or 100% color bars for component (Note 1). See Figure 1 for parameter measurement definition

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC SEPARATION					
Min Sync Amplitude		135			mV
Max Video Amplitude				3	V
Clamp timing error	NTC7 AC bounce signal (Note 2)			10	ns
Clamp Recovery TIme	NTC7 DC bounce signal (Note 3)			16	µs
CLOCK RECOVERY					
Short Term Output Jitter Rejection	Input jitter = 50ns RMS		–15		dB
RMS Residual Output Clock Jitter	Input jitter <1ns RMS		600		ps
Peak to Peak (6σ), Line to Line Jitter	Input Jitter < 1ns		2.0	2.2	ns
Head Switch Recovery Time to 1ns Error	5µs step H change on or before line 1		4		lines
Step Frequency Recovery Time to 1ns Error	1% step H frequency change on or before line 1		12	15	ms
Missing Sync Sensitivity	(Note 4)		1.0		ns
Sync Glitch Sensitivity	(Note 5)		1.0		ns
4X Clock Duty Cycle	C_{LOAD} = 50pF, f_{CLK4X} < 60MHz	40		60	%
2X Clock Duty Cycle	C_{LOAD} = 50pF, f_{CLK2X} < 30MHz	48		52	%
1X Clock Duty Cycle	C_{LOAD} = 50pF, f_{CLK1X} < 15MHz	48		52	%
Clock Skew — 1X to 2X	C_{LOAD} = 50pF, f_{CLK1X} < 15MHz			6	ns
Pulse Output Rise Time	C_{LOAD} = 50pF	2		10	ns
Pulse Output Fall Time	C_{LOAD} = 50pF	2		10	ns
Pulse Output Setup Time	C_{LOAD} = 50pF	20			ns
Pulse Output Hold Time	C_{LOAD} = 50pF	20			ns

SERIAL BUS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Low Level Input Voltage		0		0.8	V
High Level Input Voltage		V_{CC} – 0.8		V_{CC}	V
Low Level Input Current	V_{IN} = 0V			1.0	µA
High Level Input Current	V_{IN} = V_{CC} D			1.0	µA
Input Impedance f_{CLK} = 100kHz			1		MΩ
Input Capacitance (C_{IN})			2		pF
SYSTEM TIMING					
S_{CLK} Frequency (f_{CLOCK})				100	kHz
Input Hysteresis (V_{HYS})		0.2			V
Spike Suppression (t_{SPIKE})	Max length for zero response		50		ns
Power Setup Time to Valid Data Inputs	VCC Settled to Within 1%	10			ms

SERIAL BUS LOGIC (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM TIMING (Continued)					
Wait Time From STOP to START On S_{DATA} (t_{WAIT})			1.3		µs
Hold Time for START On S_{DATA} ($t_{HD/START}$)			0.6		µs
Setup Time for START On S_{DATA} ($t_{SU/START}$)			0.6		µs
Min LOW Time On S_{CLK} (t_{LOW})		1.3			µs
Min HIGH Time On S_{CLK} (t_{HI})		0.6			µs
Hold Time On S_{DATA} ($t_{HD/DATA}$)			5.0		µs
Setup Time On ($t_{SU/DATA}$)	Fast mode (Note 2)	100			ns
	Slow mode (Note 2)	250			ns
Rise Time for S_{CLK} & S_{DATA} (t_{LH})			30	300	ns
Fall Time for S_{CLK} & S_{DATA} (t_{HL})			30	300	ns
Setup Time for STOP On S_{DATA} ($t_{SU/STOP}$)			0.6		µs

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Parameter is Luma dependent.

Note 3: Reclock time after bounce.

Note 4: Net phase error for single isolated missing H pulse.

Note 5: Net phase error for glitch at sync level <50ns.

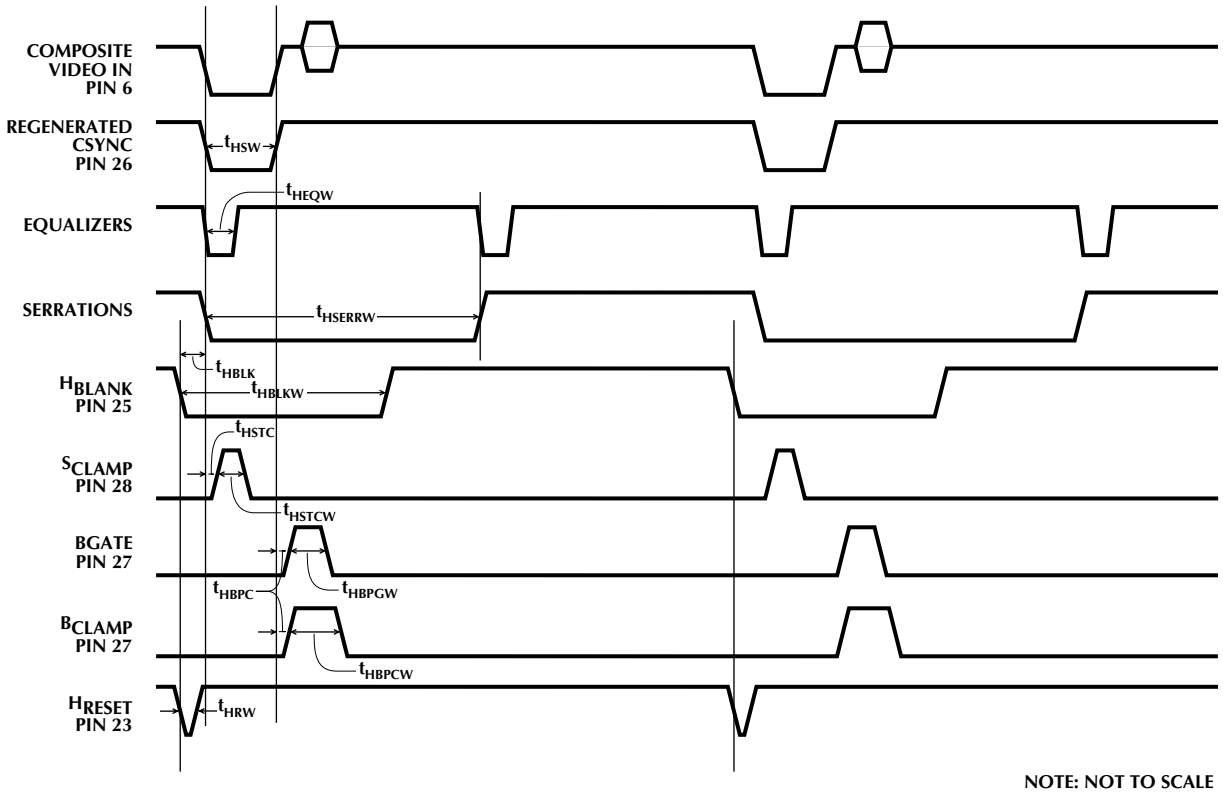


Figure 1. Line Rate Waveforms

DEVICE DIFFERENCES

Tables 1 and 2 summarize the differences between the ML6430 and ML6431. The pinouts of the ML6430 and the ML6431 are the same with the exception that the ML6431 has a few enhancements, (Center Frequency and Free Run Mode, see Table 1) and added functionality (see Table 2).

DEVICE	FUNCTIONAL DESCRIPTION									
	Video Formats, Timing, and Pulse Generation		Clock Rates			Input Crystal		Free Run Mode	VGA Clock	VCR Lock
	NTSC	PAL	CCIR601	Square Pixel	4xFSC	3.58 MHz	4.43 MHz			
ML6430	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes. Limited transition between free run modes 1 and 2. (Figure 4)	Yes. Limited to 640x480 pixel clock.	Yes
ML6431	Yes	Yes*	Yes	Yes*	Yes	Yes	Yes	Yes. Faster transition between freerun modes 1and 2. (Figure 4a)	Yes. Works up to 75MHz. (Table 6)	Yes.

* Readjusted the center frequency for PAL square pixel with NTSC crystal to achieve greater than +/-5% range. See Table 4

Table 1. Summary of Functional Differences between the ML6430 and ML6431.

DEVICE	MODE	REGISTER DIFFERENCES		PIN OUT DIFFERENCES	
		Register 7, Bit 2	Register 7, Bit 3	Pin 3	Pin 16
ML6430	Sleep Mode	0	0	$\overline{\text{SLEEP}}$	AUDIOCLK
	Pulse Generator Mode*	1	0	54MHz**	AUDIOCLK
	Time Base Correction Mode	*This function not available in the ML6430*			
ML6431	Sleep Mode	0	0	$\overline{\text{SLEEP}}$	AUDIOCLK
	Pulse Generator Mode*	1	0	54MHz**	AUDIOCLK
	PHERROUT Mode*	X	1	Must be set HIGH	PHERROUT

*For these modes the SLEEP mode can only be enable/disabled via serial bus (Register 8).

**The 54MHz clock input (pin 3) can be any 4 x Clock up to 70MHz

Table 2. Summary of Register Differences between the ML6430 and ML6431.

FUNCTIONAL DESCRIPTION

DUAL PLLS

The Genlock has the following properties:

- A stable, asynchronous crystal controlled oscillator provides the basic timing signals.
- A precision analog circuit uses the above timing signals to generate an arbitrarily phased output whose phase can be altered at pixel rate.
- A digital PLL loop monitors the error signal from a digital phase detector, and generates a pixel by pixel phase adjustment of the output.
- An intelligent state machine further enhances performance by monitoring errors and error history and adjusting the gains of the loop accordingly.
- A circuit automatically detects a VCR signal and increases loop gain for proper tracking and minimum jitter.

The digital PLL has five operating modes. In normal operation with a stable input the controller will settle to state 1. If errors are large and consistent, controller will move to state 5. If error conditions are corrected, controller will sequentially decrease the state as the errors are reduced toward 0. If small but consistent errors persist while controller is in state 1, then controller may move to states 2 or 3 to help settle out errors more quickly. None of these changes will cause a reset of pixel count, or a discontinuity of output clocks. Operating modes are described in greater detail below.

1. Normal: Gain is low, instantaneous phase gain is 1/32, giving a net short term jitter gain (output/input jitter) of about -30db. Full peak to peak jitter (including lower frequency jitter) from a white source is about -15db.
2. Slow: Gain is increased by 4x, and settling time reduced by about the same. This mode is used as a transition mode during normal lock sequence, or as a modest speed up mode if errors are high.
3. Medium: Gain is increased by 8x, and settling time reduced by about the same. This mode is used as a transition mode during normal lock sequence, or as a speed up mode if errors are consistently high.
4. Fast: Gain is increased by 16x. Adds frequency adjustments to mode 5 for fast settling during hot switches or pathological gyro errors in hand held camcorders.
5. Phase: Only Gain is 16x for phase changes, 0 for frequency changes. Primarily used to quickly settle head switch phase errors without affecting loop frequency.

LOW POWER SLEEP MODES

Sleep mode may be initiated either from the serial control bus, or from an external pin. In both cases the entire chip except the serial bus is shut down. For applications where PHERROUT is used, the sleep mode can only be enabled/disabled via serial control.

PHERROUT SIGNAL

The PHERROUT pin indicates, on a line by line basis, whether the H SYNC pulse of the analog input signal is leading or trailing the genlock's output H SYNC pulse. This information is used by the genlock to decide whether to speed up or slow down the internal clock to achieve locking of the H SYNC pulses. If PHERROUT = 0, then the analog sync is ahead; therefore, the internal clock will speed up in an effort to lock the H SYNC pulses. By contrast, if PHERROUT = 1, then the analog sync is behind; therefore, the internal clock will slow down in an effort to lock the H SYNC pulses. Ultimately, when the genlock is locked to the incoming analog signal, PHERROUT will alternate approximately every line between 0 and 1.

PHERROUT (PIN 16)	DESCRIPTION
0	Speed up output timing
1	Slow down output timing

Table 3. PHERROUT Signal Description

SYNC SEPARATION

Sync separation is accomplished using peak tracking analog amplifiers with a precision sync slicer. The closed tracking loop is equipped with timers to discriminate true sync pulses from noise glitches or chroma overshoots. The use of analog sync separation techniques removes a serious source of jitter present in most digital PLLs.

CRYSTAL SELECTION

The precision crystal source for the ML6430/ML6431 can be supplied in one of four ways. An industry standard 3.58MHz parallel tuned NTSC color subcarrier crystal or a 4.43MHz parallel tuned PAL color subcarrier crystal may be used. Alternately, a 14.318MHz NTSC or 17.7MHz PAL, 4xFs, or a 3.58MHz or 4.43MHz oscillator source may be used. Regardless of the crystal used, the ML6430/ML6431 can lock to PAL, NTSC, Beta or MII or YUV in either 625 or 525 standards. Table 4 provides the clock rate accuracy for both the NTSC and PAL clock rates for each crystal selected. Note that the range may vary between the ML6430 and the ML6431.

FUNCTIONAL DESCRIPTION (Continued)

CENTER FREQUENCY AND ± RANGE FOR EACH FREQUENCY STANDARD OF THE ML6430

VIDEO STANDARD	CLOCK RATE	CLOCK RATE ACCURACY
3.58MHz Crystal		
NTSC Square Pixel	4xClk= 49.09MHz	+8.35%/ –5.19%
NTSC 601	4xClk= 54.00MHz	+6.07%/ –7.18%
NTSC 4fsc	4xClk= 57.27MHz	+7.15%/ –6.23%
PAL Square Pixel	4xClk= 59.00MHz	+4.01%/ –9.10%
PAL 601	4xClk= 54.00MHz	+6.07%/–7.18%
PAL 4fsc	4xClk= 35.47MHz	+9.58%/ –4.14%
4.43MHz Crystal		
NTSC Square Pixel	4xClk= 49.09MHz	+8.28%/ –5.23%
NTSC 601	4xClk= 54.00MHz	+7.81%/ –5.64%
NTSC 4fsc	4xClk= 57.27MHz	+6.00%/ –7.18%
PAL Square Pixel	4xClk= 59.00MHz	+7.27%/ –6.13%
PAL 601	4xClk= 54.00MHz	+7.81%/–5.64%
PAL 4fsc	4xClk= 35.47MHz	+7.05%/ –6.31%

CENTER FREQUENCY AND ± RANGE FOR EACH FREQUENCY STANDARD OF THE ML6431

VIDEO STANDARD	CLOCK RATE	CLOCK RATE ACCURACY
3.58MHz Crystal		
NTSC Square Pixel	4xClk= 49.09MHz	+8.35%/ –5.19%
NTSC 601	4xClk= 54.00MHz	+6.07%/ –7.18%
NTSC 4fsc	4xClk= 57.27MHz	+7.15%/ –6.23%
PAL Square Pixel	4xClk= 59.00MHz	+7.47%/ –5.93%
PAL 601	4xClk= 54.00MHz	+6.07%/–7.18%
PAL 4fsc	4xClk= 35.47MHz	+7.64%/ –5.77%
4.43MHz Crystal		
NTSC Square Pixel	4xClk= 49.09MHz	+8.28%/ –5.23%
NTSC 601	4xClk= 54.00MHz	+7.81%/ –5.64%
NTSC 4fsc	4xClk= 57.27MHz	+6.00%/ –7.18%
PAL Square Pixel	4xClk= 59.00MHz	+7.27%/ –6.13%
PAL 601	4xClk= 54.00MHz	+7.81%/–5.64%
PAL 4fsc	4xClk= 35.47MHz	+7.05%/ –6.31%

Table 4. NTSC/ PAL Clock Rate Range vs. Crystal Input

DISABLING AUTOMATIC VCR SIGNAL DETECTION

DEVICE	DISABLE VCR SIGNAL DETECTION?
ML6430	No. Detection function is always on.
ML6431	Yes. Detection function can be disabled or enabled via serial bus only. This feature is enabled by default.

Table 5.

In the ML6430, the VCR detection circuit is always enabled. This circuit detects the presence of a VCR input signal at C_{VIN} / H_{SYNC} (pin 6) and automatically adjusts the gain settings for the digital PLL to optimize locking performance. This circuit scans for head switching greater than the thresholds selected by the user threshold bits (via serial bus) and then increases the phase gain of the digital PLL to compensate.

In the ML6431, the VCR detection circuit operates the same as the ML6430 with the additional ability to disable or enable the VCR detection circuit to optimize for low jitter performance. This feature is enabled by default. This feature can be disabled in the ML6431 only by setting the appropriate values in Register 7, Bit 0 via the serial bus interface (see Table 11). When the VCR detect circuit is disabled, the ML6431 is optimized for low jitter performance.

PULSE GENERATOR MODE

54MHz Input or Any 4X Clock

The 54MHz pin (pin 3) is an input that clocks the horizontal and vertical counters. In this mode, the ML6430 or ML6431 is used as a pulse generator. The input signal at can be any 4X clock; for example, 54MHz (4 x CCIR clock rate of 13.5MHz), 49.09MHz (4 x Square Pixel clock rate of 12.27MHz), or 57.27 MHz (4 x Fsc clock rate of 14.31MHz for NTSC color subcarrier). This input is limited to 70MHz.

As a pulse generator, the sync, clamp, blanking, and clock signals are derived from the clock input at the 54MHz pin. This mode is activated by setting the appropriate values in Register 7 via the serial bus. See Tables 10 or 11.

USING F_{RESET} FOR NTSC vs. PAL MODES

In NTSC mode, F_{RESET} (pin 22) goes low on the high-to-low transition of the FIELD ID pin (pin 17) and the beginning of line 1 (see Figure 2).

In the PAL mode, F_{RESET} (pin 22)goes low on the low-to-high transition of the FIELD ID pin and the end of line 310 (see Figure 3).

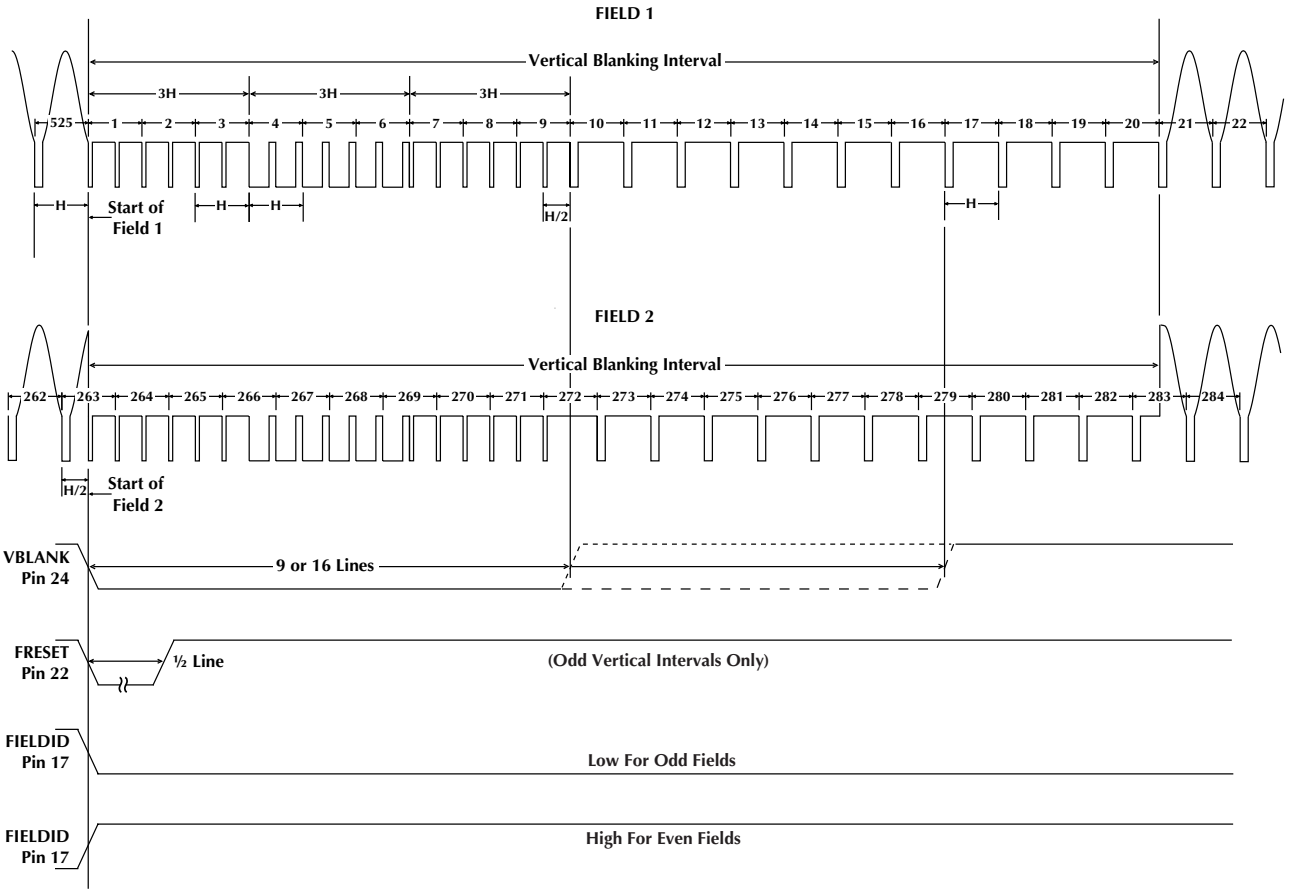


Figure 2. NTSC Field Rate Waveforms

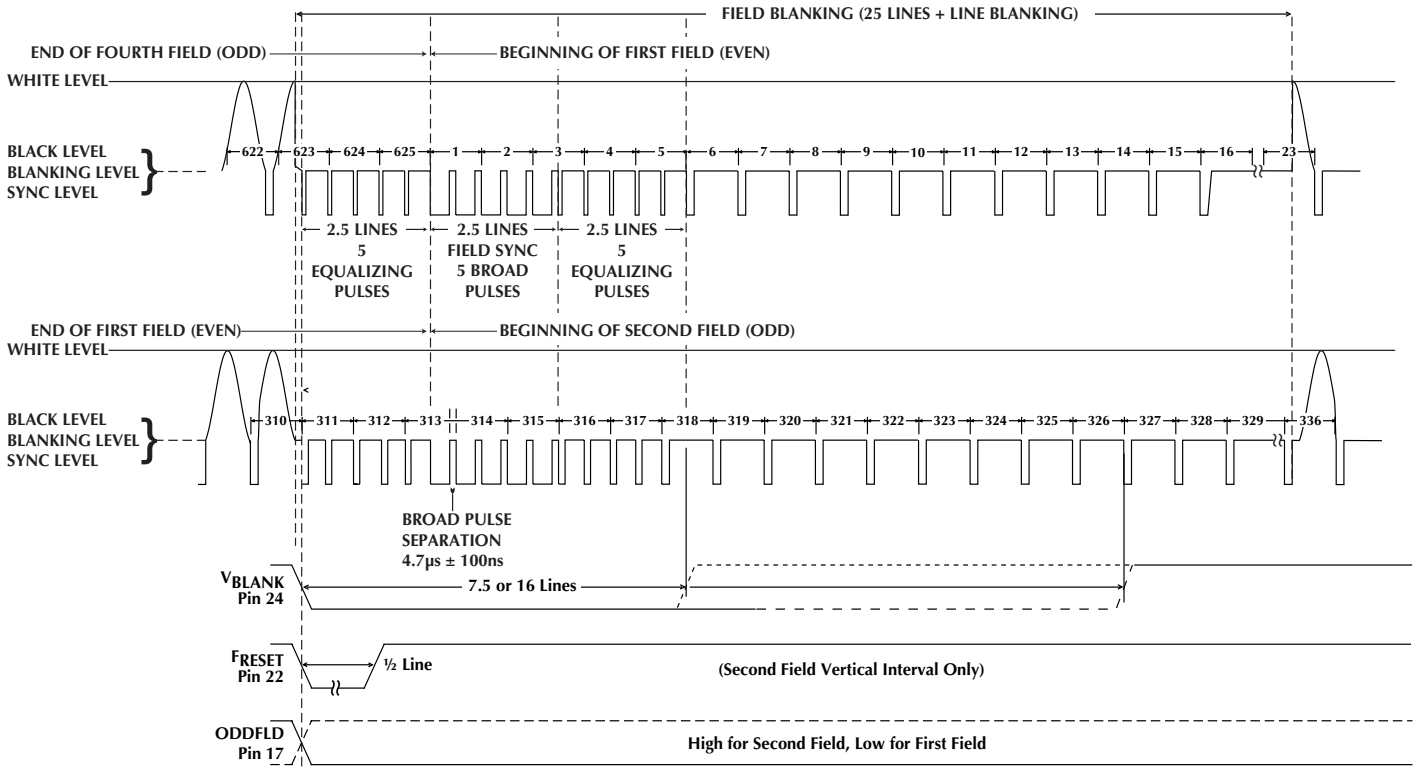


Figure 3. PAL 625 Field Rate Waveforms

FUNCTIONAL DESCRIPTION (Continued)

FREERUN MODE

Both the ML6430 and ML6431 can be used in Freerun mode. The ML6431 is recommended for applications requiring a more robust Freerun mode of operations. Figure 4 and Figure 4a describe the state diagrams for both the ML6430 and ML6431. Note that the ML6431 includes a faster path to go from FREERUN MODE #1 to FREERUN MODE #2.

Freerun mode: FREERUN MODE #1 is entered when the freerun pin is toggled high while the ML6430/ ML6431 is horizontally locked (i.e. internal horizontal locked signal is present). In this mode, the digital frequency value stored in the line-locked PLL is held and the ML6430/ML6431 will freerun at a frequency very close to that of the last locked video source. Freerun mode #1 is best used by physically tying the NoSignal pin to the freerun pin as shown in Figures 9 or 10. FREERUN MODE #2 is entered when the freerun pin is toggled high while the ML6430/Ml6431 is not horizontally locked to a video source. In this mode, a ROM lookup table is used to set the freerun frequency of the ML6430/ML6431. In this mode the output frequency is as accurate as the Crystal plus the accuracy of the look up table. See Figures 4 and 4a for the NoSignal-Locked-Freerun state machine diagram.

NoSignal: NoSignal will go low if video is present for one entire field. NoSignal will be high if video is not present for one entire field.

Locked (ML6430): The ML6430 must be line (horizontal) locked to an input video source and also be vertically locked before the locked detect signal goes high. When a video source is removed, the locked signal may be high or low. Please note that the locked pin is the logical AND of the internal horizontal locked and vertical locked signals. For example, the internal horizontal locked signal may be high even though the locked pin is asserted low.

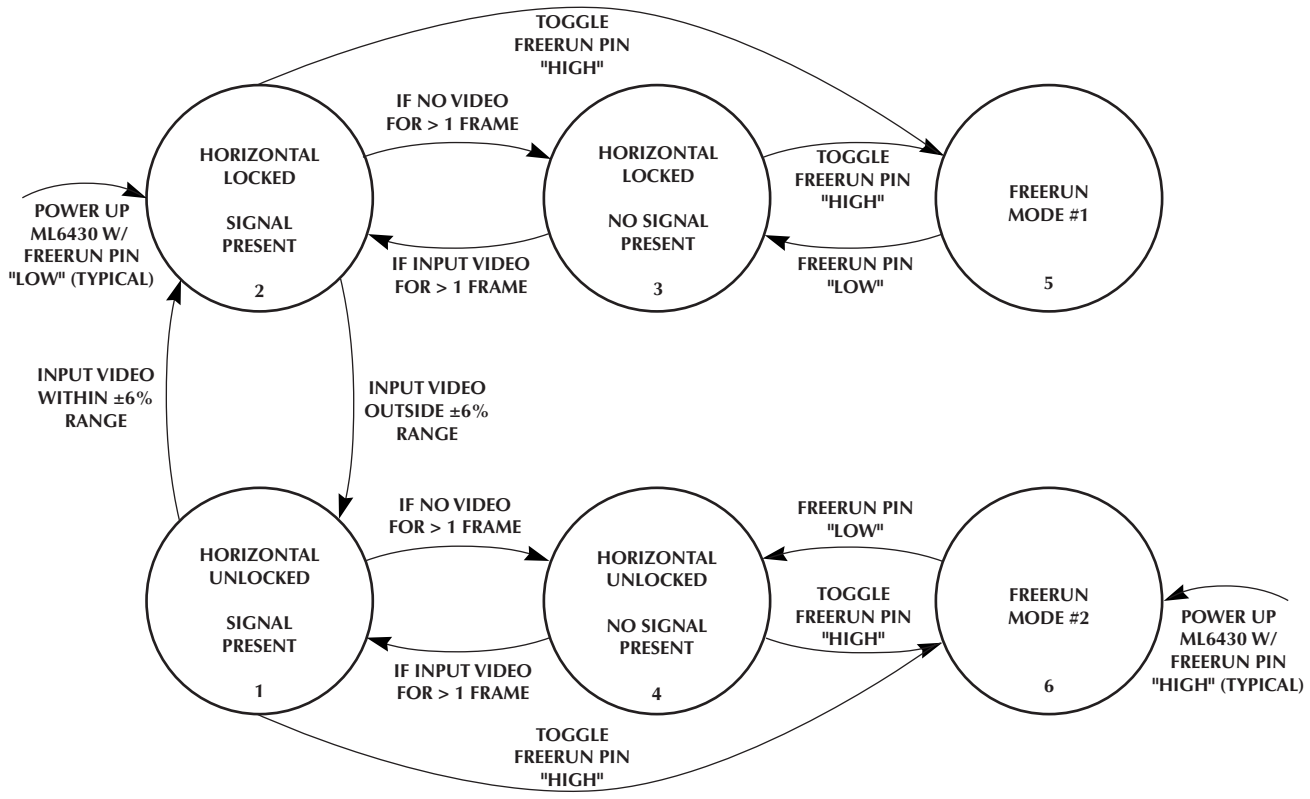


Figure 4. ML6430 Freerun Mode State Diagram

FUNCTIONAL DESCRIPTION (Continued)

Locked (ML6431): The ML6431 must be line (horizontal) locked to an input video source for at least two fields and also be vertically locked before the locked detect signal goes high. When a video source is removed, the ML6431 will lose horizontal lock after two entire fields with no video present. However, vertical lock may be lost before horizontal lock. Because the locked pin is the logical AND of the internal horizontal locked and vertical locked signals the locked pin may go low before the internal horizontal locked signal.

VGA CLOCKS

For VGA applications the ML6431 is recommended. Table 6 provides a list of the VGA clocks that can be generated using the ML6431. To use the information in Table 6 first find the resolution and refresh rate required. Determine which crystal, PAL or NTSC is needed. Change the crystal to the proper frequency if necessary. Over the serial-bus, program the registers as indicated in Table 6. Supply to pin 6 an horizontal sync signal at TTL or CMOS levels and at the specified frequency. Trigger an oscilloscope on the falling edge of the horizontal input to view the outputs. The VGA pixel clock will be found on pin 18. Other useful signals are noted in table 6. External logic may be needed to produce usable vertical sync pulses.

AUDIO CLOCKS

The audio modes can be activated via serial bus (Register 7). When this mode is activated an audio clock frequency can be selected via serial bus (Register 8). See Table 9.

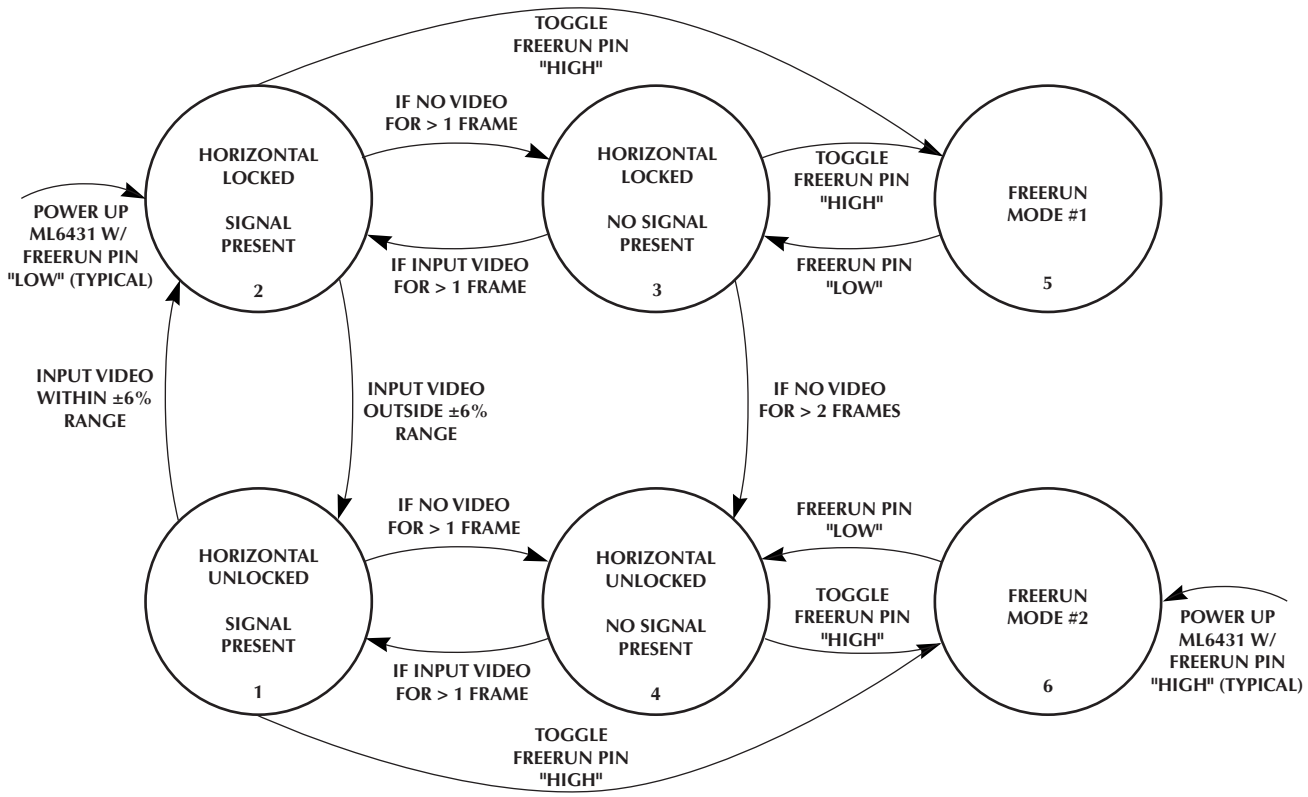


Figure 4a. ML6431 Freerun Mode State Diagram

							ML6431 Data Register Settings*								
Resolution	**# Pixels per Line**	**Refresh Rate**	**Horizontal Frequency**	**Pixel Frequency**	**Standard Type**	**Original Standard #**	**Freq. Std.**	**PALXtal**	**Pixel Reg**	**PherrOut**	**VGA**	**External Xtal Used**	**Pixel Clk Output**	**Horizontal Pulses**	**Vertical Pulses**
640 x 480	800	60 Hz	31.5 KHz	25.175 MHz	Industry		NTSC Sq Pix =000	1	572	0	1	4.43	2X	"Hsync,Hreset"	Vreset
	832	72 Hz	37.9 KHz	31.500 MHz	VESA	VS901101	NTSC Sq Pix =000	0	640	0	1	4.43	2X	"Hsync,Hreset"	Vreset
	840	75 Hz	37.5 KHz	31.500 MHz	VESA	VDMT75HZ	NTSC Sq Pix =000	0	656	0	1	4.43	2X	"Hsync,Hreset"	Vreset**
800 x 600	1024	56 Hz	35.1 KHz	36.000 MHz	VESA	VG900601	PAL 4FSC =101	1	512	1	1	4.43	4X	"Hsync,Hreset"	Vreset
	1056	60 Hz	37.9 KHz	40.000 MHz	VESA	VG900602	NTSC Sq Pix =000	1	544	1	1	3.58	4X	"Hsync,Hreset"	Vreset**
	1040	72 Hz	48.1 KHz	50.000 MHz	VESA	VS900603A	NTSC Sq Pix =000	1	528	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
	1056	75 Hz	46.9 KHz	49.500 MHz	VESA	VDMT75HZ	NTSC Sq Pix =000	1	544	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
1024 x 768	1264	43 Hz/Int	35.5 KHz	44.900 MHz	Industry		PAL 4FSC =101	0	752	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
	1344	60 Hz	48.4 KHz	65.000 MHz	VESA	VG901101A	PAL 601 = 011	0	832	1	1	4.43	4X	"Hsync,Hreset"	Vreset**
	1328	70 Hz	56.5 KHz	75.000 MHz	VESA	VS910801-2	PAL 4FSC =101	0	816	1	1	3.58	4X & clk doubler	No	No

*For Data Register Settings: TTL = High, VGA = On, VCR = Off, Noise Gating = On, Dis Auto Ver Det = 1

** w/ external glue logic

Table 6. VGA Rates Supported

FUNCTIONAL DESCRIPTION (Continued)

PRESET PIN CONTROL

The ML6430/ML6431 may be controlled via a set of four preset mode pins. These pins do not allow access to all the programmable features of the ML6430/ML6431, but are intended to provide a simpler interface for most applications.

PULSE OUTPUTS

Pulse outputs are defined in Table 12. Note that the pulse widths and start times are chosen to the nearest clock edge, and indicated errors assume nominal clock operating frequency.

P3	P2	P1	P0	STD	CLOCK RATE	CRYSTAL
0	1	0	1	NTSC	Square pixel	3.58MHz
1	0	0	1	NTSC	CCIR601	3.58MHz
1	1	0	1	NTSC	4Fsc	3.58MHz
0	1	1	1	PAL	Square pixel	3.58MHz
1	0	1	1	PAL	CCIR601	3.58MHz
1	1	1	1	PAL	4Fsc	3.58MHz
0	1	0	Z	NTSC	Square pixel	4.43MHz
1	0	0	Z	NTSC	CCIR601	4.43MHz
1	1	0	Z	NTSC	4Fsc	4.43MHz
0	1	1	Z	PAL	Square pixel	4.43MHz
1	0	1	Z	PAL	CCIR601	4.43MHz
1	1	1	Z	PAL	4Fsc	4.43MHz
0	Z	0	1	NTSC	Square pixel	14.32MHz
Z	0	0	1	NTSC	CCIR601	14.32MHz
Z	Z	0	1	NTSC	4Fsc	14.32MHz
0	Z	1	1	PAL	Square pixel	14.32MHz
Z	0	1	1	PAL	CCIR601	14.32MHz
Z	Z	1	1	PAL	4Fsc	14.32MHz
0	Z	0	Z	NTSC	Square pixel	17.72MHz
Z	0	0	Z	NTSC	CCIR601	17.72MHz
Z	Z	0	Z	NTSC	4Fsc	17.72MHz
0	Z	1	Z	PAL	Square pixel	17.72MHz
Z	0	1	Z	PAL	CCIR601	17.72MHz
Z	Z	1	Z	PAL	4Fsc	17.72MHz
Z	1	0	1	NTSC	Square pixel, VGA	3.58MHz
1	Z	0	1	NTSC	CCIR601,VGA	3.58MHz
0	0	0	1	NTSC	4Fsc, VGA	3.58MHz
Z	1	1	1	PAL	Square pixel, VGA	3.58MHz
1	Z	1	1	PAL	CCIR601, VGA	3.58MHz
0	0	1	1	PAL	4Fsc, VGA	3.58MHz
Z	1	0	Z	NTSC	Square pixel, VGA	4.43MHz
1	Z	0	Z	NTSC	CCIR601, VGA	4.43MHz
0	0	0	Z	NTSC	4Fsc, VGA	4.43MHz
Z	1	1	Z	PAL	Square pixel, VGA	4.43MHz
1	Z	1	Z	PAL	CCIR601, VGA	4.43MHz
0	0	1	Z	PAL	4Fsc, VGA	4.43MHz
X	X	X	0		Serial control mode	

Z = Floating input, 0 = Low input, 1 = High input, X = Don't care

Table 7. Preset Pin Modes

FUNCTIONAL DESCRIPTION (Continued)

CONTROL REGISTER INFORMATION

REGISTER	SETTING
PulsePol[2:0]	000
Clk4X	0
Pixel[10:0]	Determined by PRESET pin
Burst	0
CSyncRaw	0
RawClamp	0
TTL Sync	0
WideBlank	0
HDelay[6:0]	1000000
Noise Gating	0
Test 3,1,4	0, 0, 0
External 54 Clock IN	0
FAud[1:0]	01
VCR	0
SLEEP	0
Thresh[1:0]	11
VGA	Determined by PRESET pin
Div4	Determined by PRESET pin
Fstd[2:0]	Determined by PRESET pin
$PALX_{TAL}$	Determined by PRESET pin

Table 8. Default Control Register Settings for Preset Mode

REGISTER DESCRIPTION

SLEEP: Enables or disables sleep mode. When using serial bus control, ALL registers must be programmed to their intended state after power up to ensure correct operation of the ML6430/ML6431.

CSR: Composite sync register bit controls whether composite sync output is from the sync separator, (raw C_{SYNC}) or from the internal pulse generator (regenerated C_{SYNC}).

Pulse Polarity Control: The active state of output sync pulses, blanking pulses, or clamp pulses may be programmed to either 0 or 1 state by use of these bits.

P0: C_{SYNC} pulse output is high active when 1, low active when 0.

P1: H_{BLANK}, and V_{BLANK} pulse outputs are high active when 1, low active when 0.

P2: S_{CLAMP} and B_{CLAMP} pulse outputs are high active when 1, low active when 0.

Burst: Controls the length of Burst Gate so pulse can be used for either burst gating in encoder applications or back porch clamping.

RawClamp: Controls the source of the S_{CLAMP} (sync clamp) pulse. Pulse is timed relative to incoming sync edge, or regenerated sync edge.

PALXTAL: Controls the expected crystal frequency at the oscillator inputs. 0 = NTSC 3.58MHz, or 1 = PAL 4.43MHz.

Thresh1,Thresh0: Selects the pixel error threshold at which relock is initiated. Values are:

0,0: 2.5 pixels
0,1: 2.5 pixels
1,0: 1.0 pixels
1,1: 4.0 pixels

Noise Gating: Enables a 3/4 line window to lockout any unwanted horizontal sync pulses.

VGA: Produces non-interlaced progressive scan outputs.

Div4: Controls the prescaler in the M/N loop. High means that 4Fs external oscillator signals are expected, low assumes a PAL or NTSC Fs crystal will be used.

VCR: Controls the gain range and locking maneuvers of the digital loop. Provides better locking to the unpredictability of VCR headswitches and jitter.

Blanking Width Control: The number of blanked lines in the vertical interval is programmable to either 9 or 16.

XTAL: external Crystal Control: 0=NTSC 3.58MHz, or 1=PAL 4.43MHz, for both local crystal and external oscillator mode.

External 54MHz Clock: This mode permits injecting a 54MHz clock (or other 4X clock) directly into the horizontal pixel counter via the $\overline{SLEEP}$ pin. All timing pulses are synchronous to the 54MHz clock (or other 4X clock).

Serial Bus Control: To place the Ml6430/ML6431 in serial mode, take P0 (Preset) to logical '0' or ground. The serial control system is written to by the external processor in 8-bit bytes. Each of these bytes is partitioned into an address (upper 4 bits of serial byte) and a data register (lower 4 bits of serial byte). In Table 10, the Register heading refers to the 4-bit address, and Data Bit refers to a particular bit in the 4-bit register (Bit0 is LSB).

Pixel: Program all bits to zero to enable default values for each standard. Otherwise use the following equation:

$$P[10:0] = 2 \times (\text{number of pixels per line}) - 1024 \quad (1)$$

Test: All test bits must be programmed to zero.

FUNCTIONAL DESCRIPTION (Continued)

Audio Clock: The Ml6430/ML6431 outputs a clock at 32kHz, 44.1kHz, or 48kHz. This clock is locked in frequency to the basic video clock regardless of the standard being used. With VCR head switches, the phase correction required to track the timing is removed from the audio clock by a patented circuit. This prevents the audio clock from being modulated by step changes in video timing. See the Table 9 for the audio clock rates supported and how they are derived internally.

ADDITIONAL CONTROL REGISTERS (ML6431 ONLY)

DisAutoVCR: Disables the auto VCR detect circuit.

Register 7, Bit 0: DisAutoVCR

PHERROUT: MUX phase error signal onto AUDIOCLK/PHERROUT pin.

Register 7, Bit 3: PHERROUT enable

This bit controls the source of AUDIOCLK/PHERROUT. When this bit is low, AUDIOCLK/PHERROUT provides the audio clock output. When this bit is high, AUDIOCLK/PHERROUT provides the 1-bit digital phase error of each Hsync edge.

Additionally, when both PHERROUT enable and VGA bits are logic high, the reset point of the pixel counter is changed from 512 to 256. This changes the equation for calculating the number of pixels per line verses the Pixel Counter bits to the following:

$$P[10:0] = 2 \times (\text{number of pixels per line}) - 512 \quad (2)$$

VIDEO STANDARD	AUDIO RATE	AUDIO/PIXEL CLOCK RATIO	AUDIO/FRAME RATE RATIO
CCIR601 NTSC	48kHz	(96000 ÷ 27MHz) × 13.5MHz	(8008 ÷ 5) × 29.97Hz
CCIR601 NTSC	44.1kHz	(88200 ÷ 27MHz) × 13.5MHz	(147147 ÷ 100) × 29.97Hz
CCIR601 NTSC	32kHz	(64000 ÷ 27MHz) × 13.5MHz	(16016 ÷ 15) × 29.97Hz
CCIR601 PAL	48kHz	(96000 ÷ 27MHz) × 13.5MHz	(1920) × 25Hz
CCIR601 PAL	44.1kHz	(88200 ÷ 27MHz) × 13.5MHz	(1764) × 25Hz
CCIR601 PAL	32kHz	(64000 ÷ 27MHz) × 13.5MHz	(1280) × 25Hz
NTSC Square Pixel	48kHz	(105600 ÷ 27MHz) × 12.27MHz	(8008 ÷ 5) × 29.97Hz
NTSC Square Pixel	44.1kHz	(97020 ÷ 27MHz) × 12.27MHz	(147147 ÷ 100) × 29.97Hz
NTSC Square Pixel	32kHz	(70400 ÷ 27MHz) × 12.27MHz	(16016 ÷ 15) × 29.97Hz
PAL Square Pixel	48kHz	(96000 ÷ 29.5MHz) × 14.75MHz	(1920) × 25Hz
PAL Square Pixel	44.1kHz	(88200 ÷ 29.5MHz) × 14.75MHz	(1764) × 25Hz
PAL Square Pixel	32kHz	(64000 ÷ 29.5MHz) × 14.75MHz	(1280) × 25Hz
NTSC 4xFSC	48kHz	(105600 ÷ 31.5MHz) × 14.32MHz	(8008 ÷ 5) × 29.97Hz
NTSC 4xFSC	44.1kHz	(92400 ÷ 30MHz) × 14.32MHz	(147147 ÷ 100) × 29.97Hz
NTSC 4xFSC	32kHz	(70400 ÷ 31.5MHz) × 14.32MHz	(16016 ÷ 15) × 29.97Hz
PAL 4xFSC	48kHz	(76800 ÷ 28.37MHz) × 17.72MHz	(1920) × 25Hz
PAL 4xFSC	44.1kHz	(70560 ÷ 28.37MHz) × 17.72MHz	(1764) × 25Hz
PAL 4xFSC	32kHz	(51200 ÷ 28.37MHz) × 17.72MHz	(1280) × 25Hz

Table 9. Audio Clock Generation (ML6430/ML6431)

REGISTER	DATA BIT	DESCRIPTION		VALUE RANGE	BIT CODE RANGE
0	0	PulsePol 0	C_{SYNC} Polarity	High Active-Low Active	0 or 1
0	1	PulsePol 1	H/V Blank Polarity	High Active-Low Active	0 or 1
0	2	PulsePol 2	S/B Clamp Polarity	High Active-Low Active	0 or 1
0	3	Clk 4X	Select 4X Clock	Low 1X Clock = 13.5MHz High 4X Clock = 54MHz	0 or 1
1	0	Pixel0	Pix Counter Load Bit 0	Numerical value taken as unsigned binary. Actual no. of pixels is: $512 + \frac{P[10:0]}{2}$ Do not vary pixel [10:0] by more than ±6% from nominal. 1024 > no. of pixels > 512 and $f_{NOM} \times 1.06 > f_{NEW} > f_{NOM} \times 0.94$	nom = ~011 0000 0000 max = 011 0011 0000 min = 010 1101 0000
1	1	Pixel1	Pix Counter Load Bit 1		
1	2	Pixel2	Pix Counter Load Bit 2		
1	3	Pixel3	Pix Counter Load Bit 3		
2	0	Pixel4	Pix Counter Load Bit 4		
2	1	Pixel5	Pix Counter Load Bit 5		
2	2	Pixel6	Pix Counter Load Bit 6		
2	3	Pixel7	Pix Counter Load Bit 7		
3	0	Pixel8	Pix Counter Load Bit 8		
3	1	Pixel9	Pix Counter Load Bit 9		
3	2	Pixel10	Pix Counter Load Bit 10		
3	3	Burst	Burst Gate Enable	Low = Back Porch Clamp High = Burst Gate	0 or 1
4	0	CSyncRaw	(or C_{SYNC} Regen)	Low = regenerated C_{SYNC} High = raw C_{SYNC}	0 or 1
4	1	RawClamp	(or Clamp Regen)	Low = regenerated Clamp High = raw Clamp	0 or 1
4	2	TTL Sync	TTL horizontal + vertical Sync Input	Low = sync separator active High = TTL horiz + vert sync input	0 or 1
4	3	WideBlank	(or Narrow)	Low = narrow blanking High = wide blanking	0 or 1
5	0	HDelay0	H Delay parameter allows moving the entire constellation of output pulses relative to the incoming H_{SYNC}. Exception: Sync Tip clamp may be selected for delay or triggered from incoming sync depending on application.	7-bit Horizontal Delay parameter. Values: –64p< Hdly < 63p, p = $1/F_{4XCLK}$	0000000 to 1111111: 0000000 means –64p 1111111 means +63p 1000000 means 0p
5	1	HDelay1			
5	2	HDelay2			
5	3	HDelay3			
6	0	HDelay4			
6	1	HDelay5			
6	2	HDelay6			
6	3	Noise Gating	3/4 line lockout	Low = noise gating on High = noise gating off	0 or 1

Table 10. ML6430 Register Map

REGISTER	DATA BIT	DESCRIPTION		VALUE RANGE	BIT CODE RANGE
7	0	Test 3	For test mode only: No user programmable features	Set to 0	0
7	1	Test 1	For test mode only: No user programmable features	Set to 0	0
7	2	Ext 54 Clock IN		Low = Pin 3 is $\overline{\text{SLEEP}}$ High = Pin 3 is 54MHz Clock	0 or 1
7	3	Test 4	For test mode only: No user programmable features	Set to 0	0
8	0	FAud0	AudioClk Freq Bit 0	00 = 48kHz, 01 = 44.1kHz, 10 = 32kHz	00 to 10
8	1	FAud1	AudioClk Freq Bit 1		
8	2	VCR	Enable VCR Mode	High = Enabled, Low = Disabled	
8	3	SLEEP	Power Down Mode	High = Power Down, Low = Normal	0 or 1
9	0	Thresh0	Select 'Out of Lock' Threshold	00 = 2.5 Pixels 10 = 1.0 Pixels	00 to 11
9	1	Thresh1		01 = 2.5 Pixels 11 = 4.0 Pixels	
9	2	VGA	Enable VGA Mode	High = Enabled, Low = Disabled	0 or 1
9	3	Div4	Enable /4 on M/N Loop	High = Enabled, Low = Disabled	0 or 1
10	0	FStd0	Freq Std Sel Bit 0	000 = NTSC Sq Pix 011 = PAL 601	000 to 101
10	1	FStd1	Freq Std Sel Bit 1	001 = PAL Sq Pix 100 = NTSC 4Fsc	
10	2	FStd2	Freq Std Sel Bit 2	010 = NTSC 601 101 = PAL 4Fsc	
10	3	$PALX_{TAL}$	Enable PAL Ref Freq	High = Enabled, Low = Disabled	0 or 1

Table 10. ML6430 Register Map (Continued)

REGISTER	DATA BIT	DESCRIPTION		VALUE RANGE	BIT CODE RANGE
0	0	PulsePol 0	C_{SYNC} Polarity	High Active-Low Active	0 or 1
0	1	PulsePol 1	H/V Blank Polarity	High Active-Low Active	0 or 1
0	2	PulsePol 2	S/B Clamp Polarity	High Active-Low Active	0 or 1
0	3	Clk 4X	Select 4X Clock	Low 1X Clock = 13.5MHz High 4X Clock = 54MHz	0 or 1
1	0	Pixel0	Pix Counter Load Bit 0	Numerical value taken as unsigned binary. Actual no. of pixels is: $512 + \frac{P[10:0]}{2}$ Do not vary pixel [10:0] by more than ±6% from nominal. 1024 > no. of pixels > 512 and $f_{NOM} \times 1.06 > f_{NEW} > f_{NOM} \times 0.94$ If PHERR enable and VGA = 1, the actual no. of pixels is: P[10:0]=2x(no. of pixels per line)–512	nom = ~011 0000 0000 max = 011 0011 0000 min = 010 1101 0000
1	1	Pixel1	Pix Counter Load Bit 1		
1	2	Pixel2	Pix Counter Load Bit 2		
1	3	Pixel3	Pix Counter Load Bit 3		
2	0	Pixel4	Pix Counter Load Bit 4		
2	1	Pixel5	Pix Counter Load Bit 5		
2	2	Pixel6	Pix Counter Load Bit 6		
2	3	Pixel7	Pix Counter Load Bit 7		
3	0	Pixel8	Pix Counter Load Bit 8		
3	1	Pixel9	Pix Counter Load Bit 9		
3	2	Pixel10	Pix Counter Load Bit 10		
3	3	Burst	Burst Gate Enable	Low = Back Porch Clamp High = Burst Gate	0 or 1
4	0	CSyncRaw	(or C_{SYNC} Regen)	Low = regenerated C_{SYNC} High = raw C_{SYNC}	0 or 1
4	1	RawClamp	(or Clamp Regen)	Low = regenerated Clamp High = raw Clamp	0 or 1
4	2	TTL Sync	TTL horizontal + vertical Sync Input	Low = sync separator active High = TTL horiz + vert sync input	0 or 1
4	3	WideBlank	(or Narrow)	Low = narrow blanking High = wide blanking	0 or 1
5	0	HDelay0	H Delay parameter allows moving the entire constellation of output pulses relative to the incoming H_{SYNC}. Exception: Sync Tip clamp may be selected for delay or triggered from incoming sync depending on application.	7-bit Horizontal Delay parameter. Values: –64p < Hdly < 63p, p = $1/F_{4XCLK}$	0000000 to 1111111: 0000000 means –64p 1111111 means +63p 1000000 means 0p
5	1	HDelay1			
5	2	HDelay2			
5	3	HDelay3			
6	0	HDelay4			
6	1	HDelay5			
6	2	HDelay6			
6	3	Noise Gating	3/4 line lockout	Low = noise gating on High = noise gating off	0 or 1

Table 11. ML6431 Register Map

REGISTER	DATA BIT	DESCRIPTION		VALUE RANGE	BIT CODE RANGE
7	0	DisAutoVCR		0=Auto VCR Detect ON 1=Disable Auto VCR Detect	0 or 1
7	1	Test 1	For test mode only: No user programmable features.	Set to 0	0
7	2	Ext 54 Clock IN		Low = Pin 3 is $\overline{\text{SLEEP}}$ High = Pin 3 is Ext 54MHz Clock	0 or 1
7	3	PHERROUT or AUDIOCLK		Low=Pin 16 is Audio CLK, Pin 3 is $\overline{\text{SLEEP}}$ High=Pin 16 is PHERROUT, Pin 3 is $\overline{\text{RESET}}$	0 or 1
8	0	FAud0	AudioClk Freq Bit 0	00 = 48kHz, 01 = 44.1kHz, 10 = 32kHz	00 to 10
8	1	FAud1	AudioClk Freq Bit 1		
8	2	VCR	Enable VCR Mode	High = Enabled, Low = Disabled	
8	3	SLEEP	Power Down Mode	High = Power Down, Low = Normal	
9	0	Thresh0	Select 'Out of Lock' Threshold	00 = 2.5 Pixels 10 = 1.0 Pixels	00 to 11
9	1	Thresh1		01 = 2.5 Pixels 11 = 4.0 Pixels	
9	2	VGA	Enable VGA Mode	High = Enabled, Low = Disabled	0 or 1
9	3	Div4	Enable /4 on M/N Loop	High = Enabled, Low = Disabled	0 or 1
10	0	FStd0	Freq Std Sel Bit 0	000 = NTSC SqPix 011 = PAL 601	000 to 100
10	1	FStd1	Freq Std Sel Bit 1	001 = PAL Sq Pix 100 = NTSC 4Fsc	
10	2	FStd2	Freq Std Sel Bit 2	010 = NTSC 601	
10	3	$PALX_{TAL}$	Enable PAL Ref Freq	High = Enabled, Low = Disabled	0 or 1

Table 11. ML6431 Register Map (Continued)

FUNCTIONAL DESCRIPTION (Continued)

SERIAL BUS OPERATION

The serial bus control in the ML6430/ML6431 has two levels of addressing: Device Addressing and Register Addressing.

Device Addressing: Figure 5 shows the physical waveforms generated in order to address the ML6430/ML6431. There are six basic parts of the waveform:

1. Start Indication: Clock Cycle 0
2. Device Address Shifted: Clock Cycle 1 through 8
3. Device Address Strobed and Decoded: Clock Cycle 9
4. Data Shifted : Clock Cycle 10 through 17
5. Data Strobed into Appropriate Register: Clock Cycle 18
6. Stop indication: Clock Cycle 19

Register Addressing: Figure 6 shows the register map of the ML6430/6431. There are two basic parts of each received data byte: Address Nibble and Data Nibble

1. Address Nibble: The upper 4 bits of the data byte gives the register number in which to place the data.
2. Data Nibble: The lower 4 bits of the data byte is the data to be placed in the currently addressed register nibble.

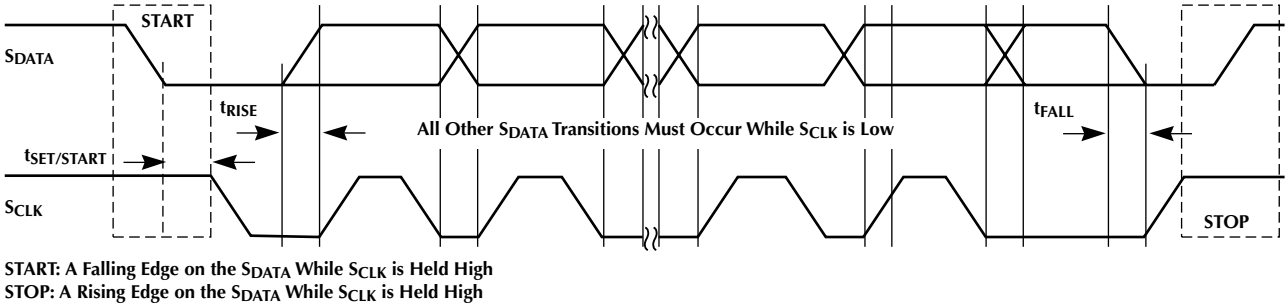


Figure 5. Definition of START & STOP on Serial Data Bus

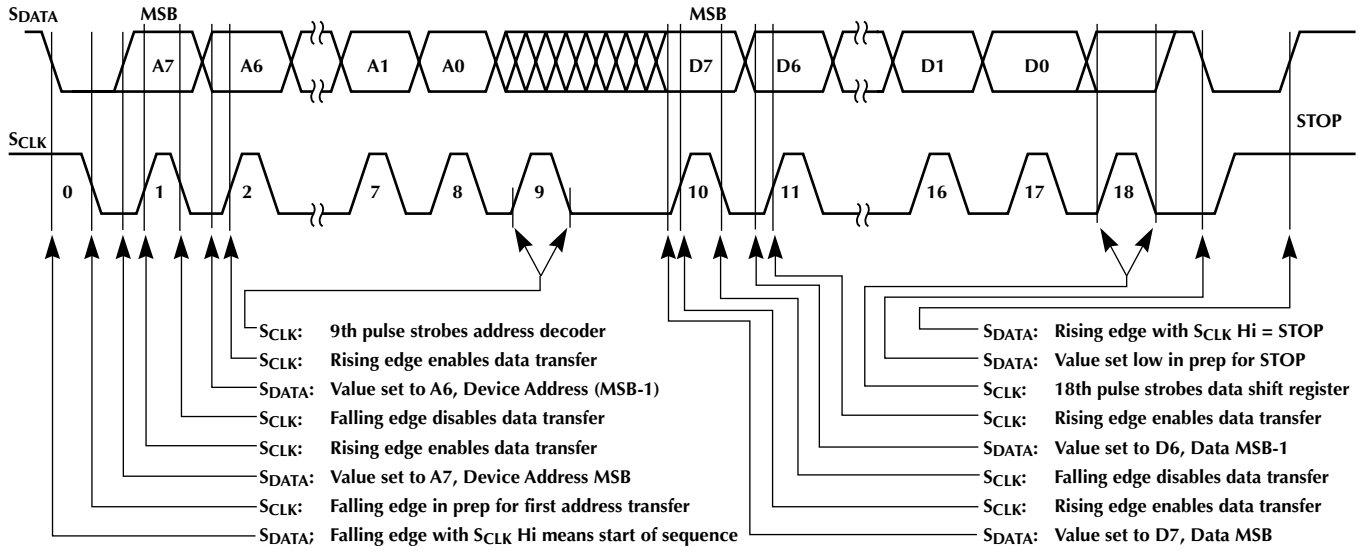


Figure 6. Definition of DATA FORMAT on Serial Data Bus

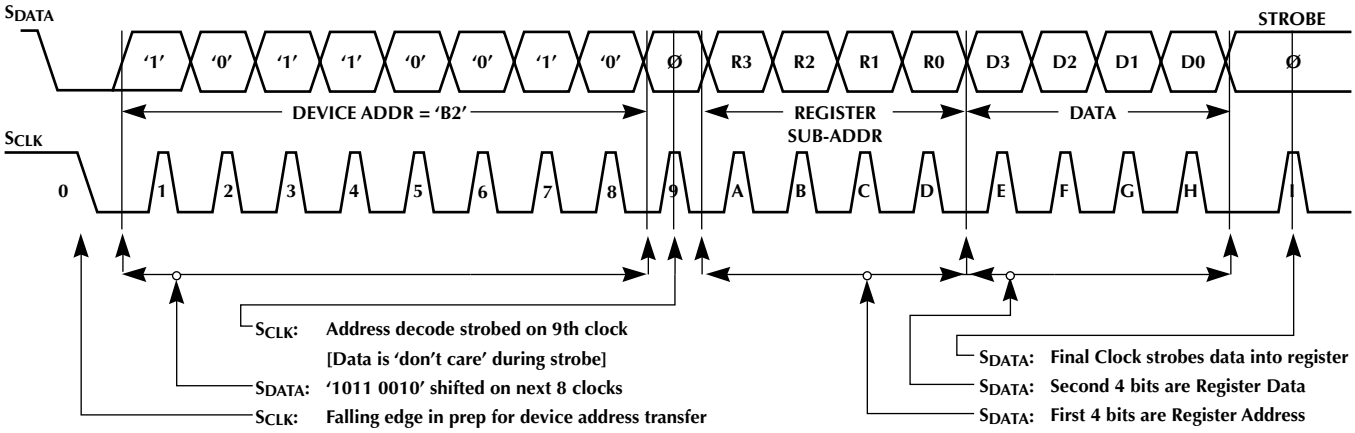


Figure 7. Typical Serial Bus Command

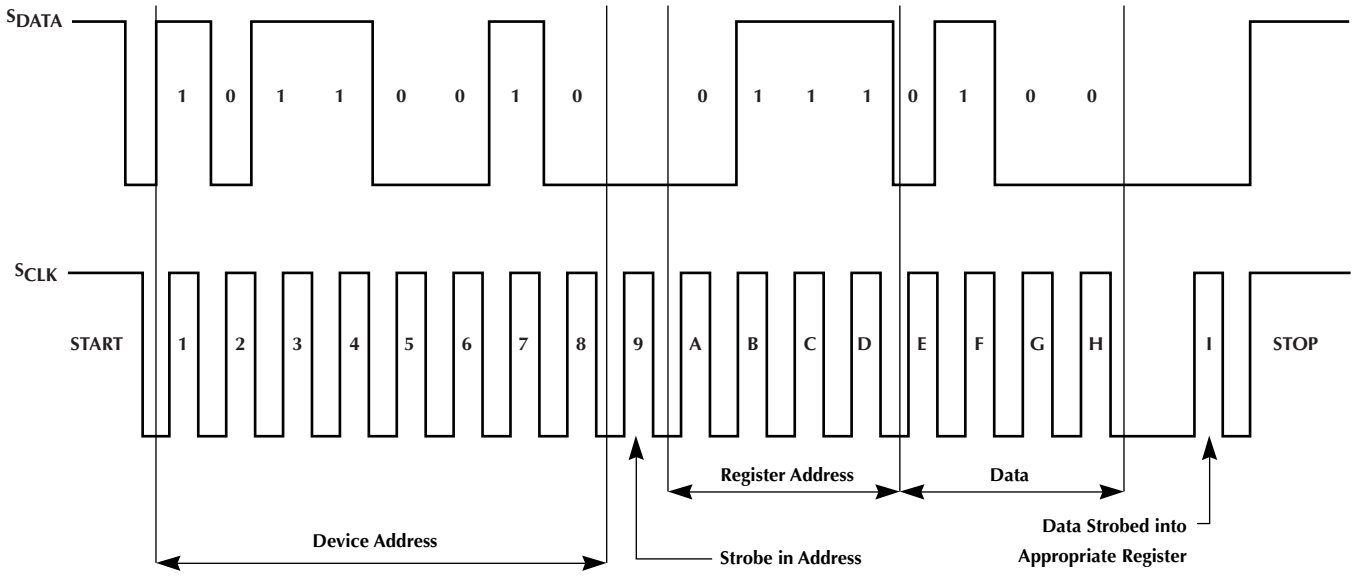


Figure 8. Serial Bus Command to Set Bit #2 in Register 7

APPLICATIONS

The ML6430 and ML6431 can be used for a variety of applications. The following figures provide a basic setup for the various applications listed below:

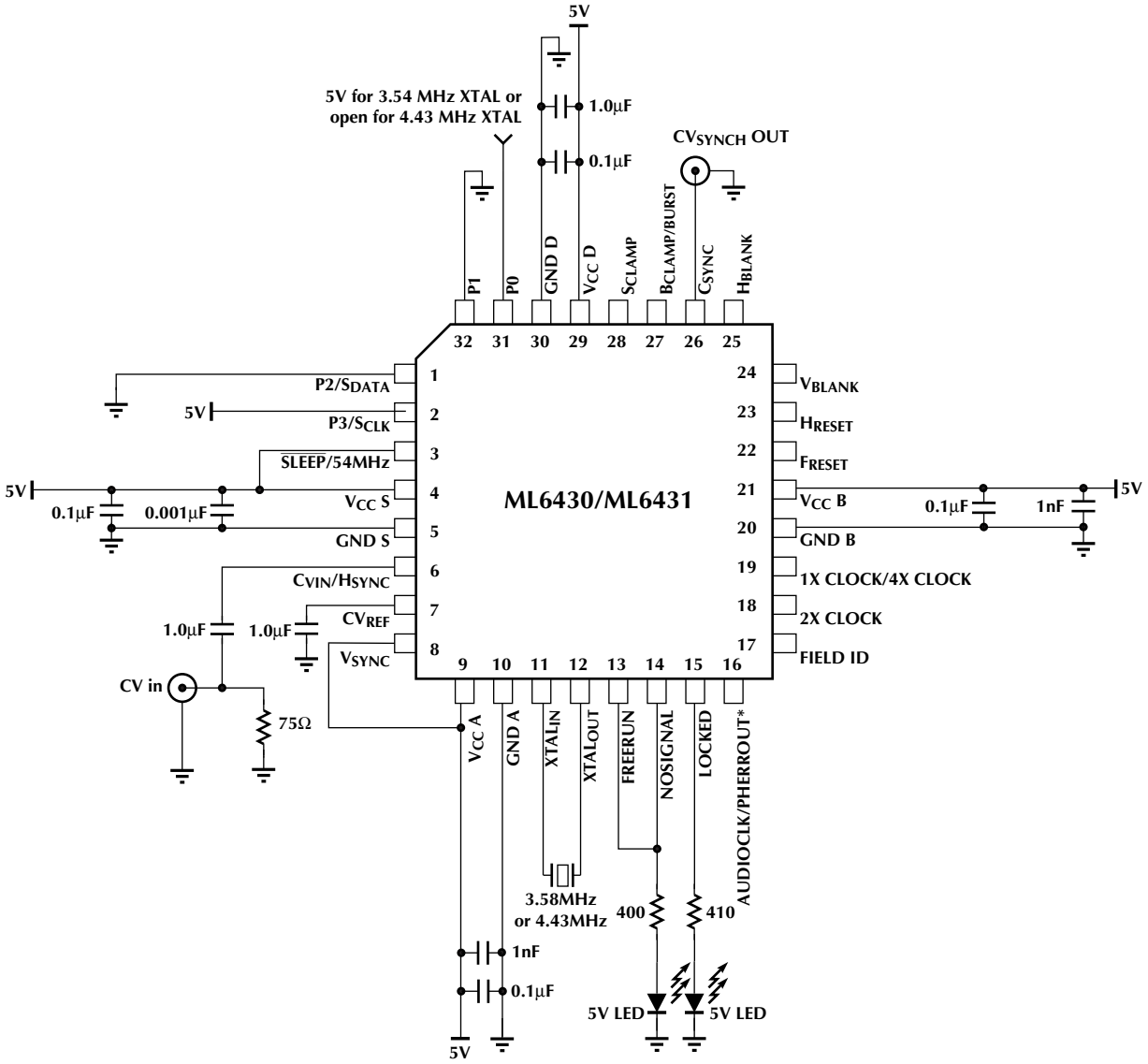
Figure 9: ML6430 or ML6431 in NTSC CCIR Applications

Figure 10: ML6430 or ML6431 in PAL CCIR Applications

Figure 11: ML6431 in VGA Application

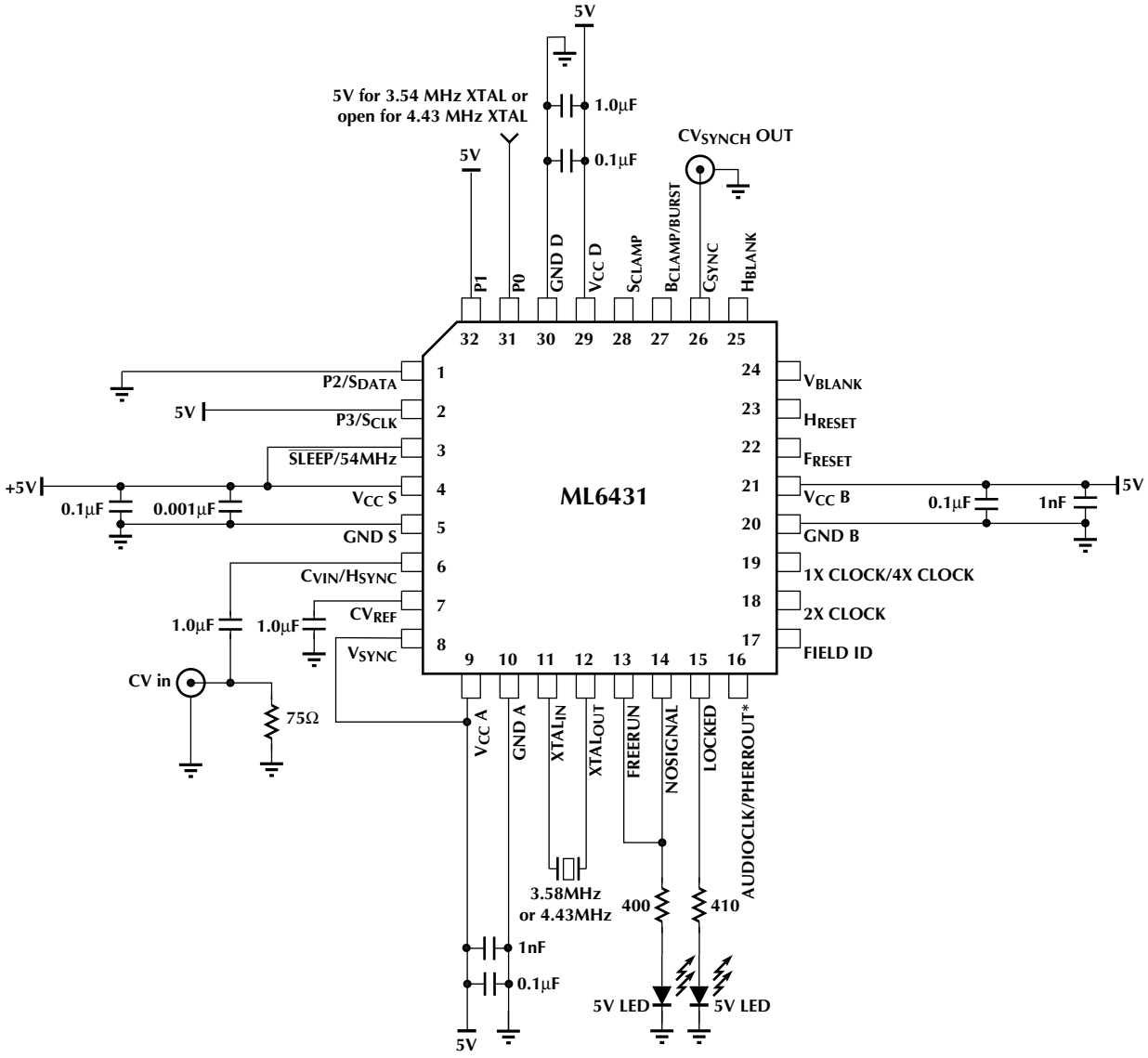
Figure 12: ML6430 or ML6431 in Audio Applications

Figure 13: ML6430 or ML6431 in Pulse Generator Applications



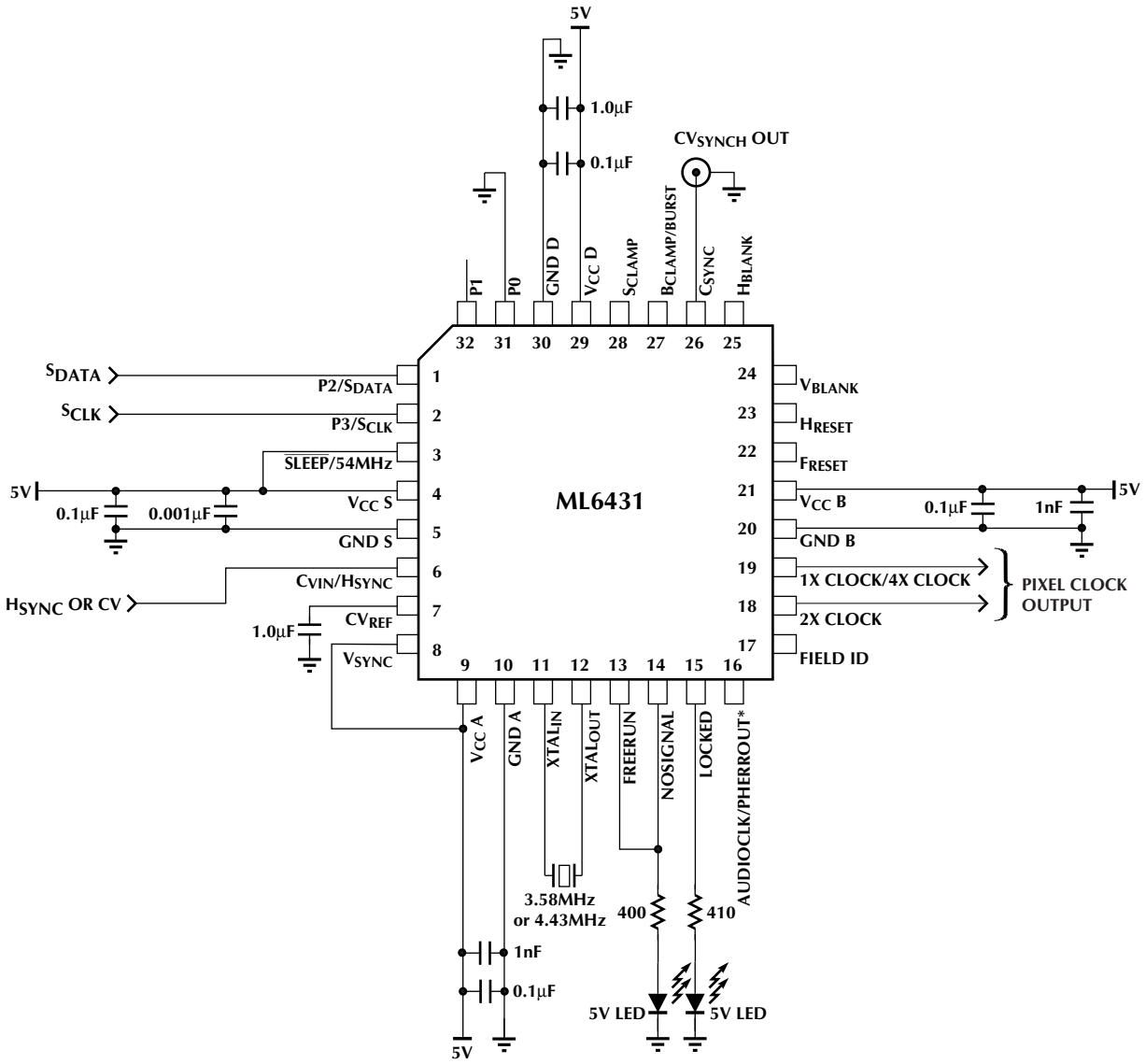
Note 1. For minimum V_{CC} bypassing, connect capacitors V_{CC}A only. (V_{CC}A to GND A)
*PHERROUT is only available with the ML6431

Figure 9. ML6430/ML6431 in NTSC CCIR Applications Programmed via Preset Pins



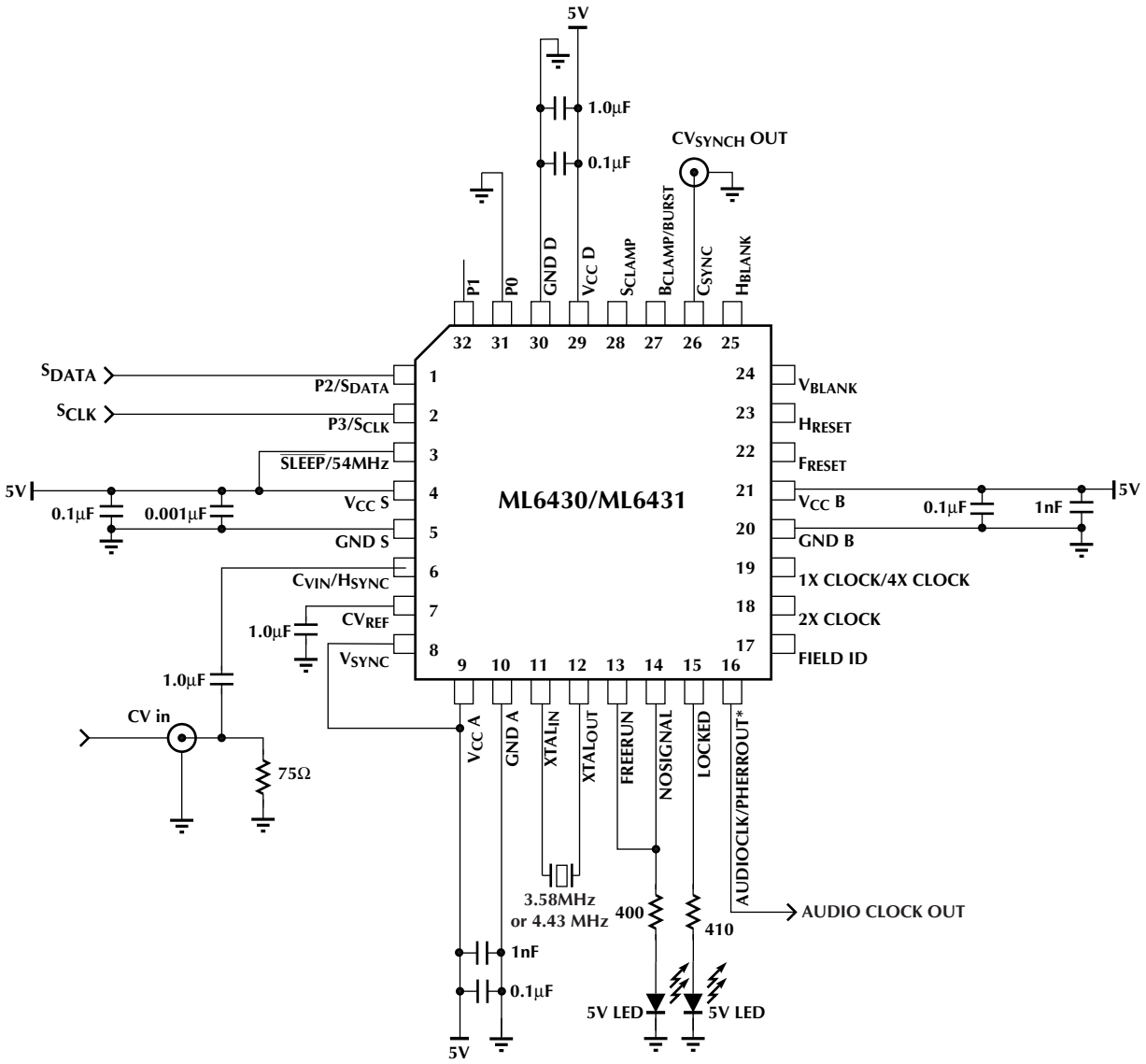
Note 1. For minimum V_{CC} bypassing, connect capacitors V_{CC}A only. (V_{CC}A to GND A)
*PHERROUT is only available with the ML6431

Figure 10. ML6430/ML6431 in PAL CCIR Applications Programmed via Preset Pins



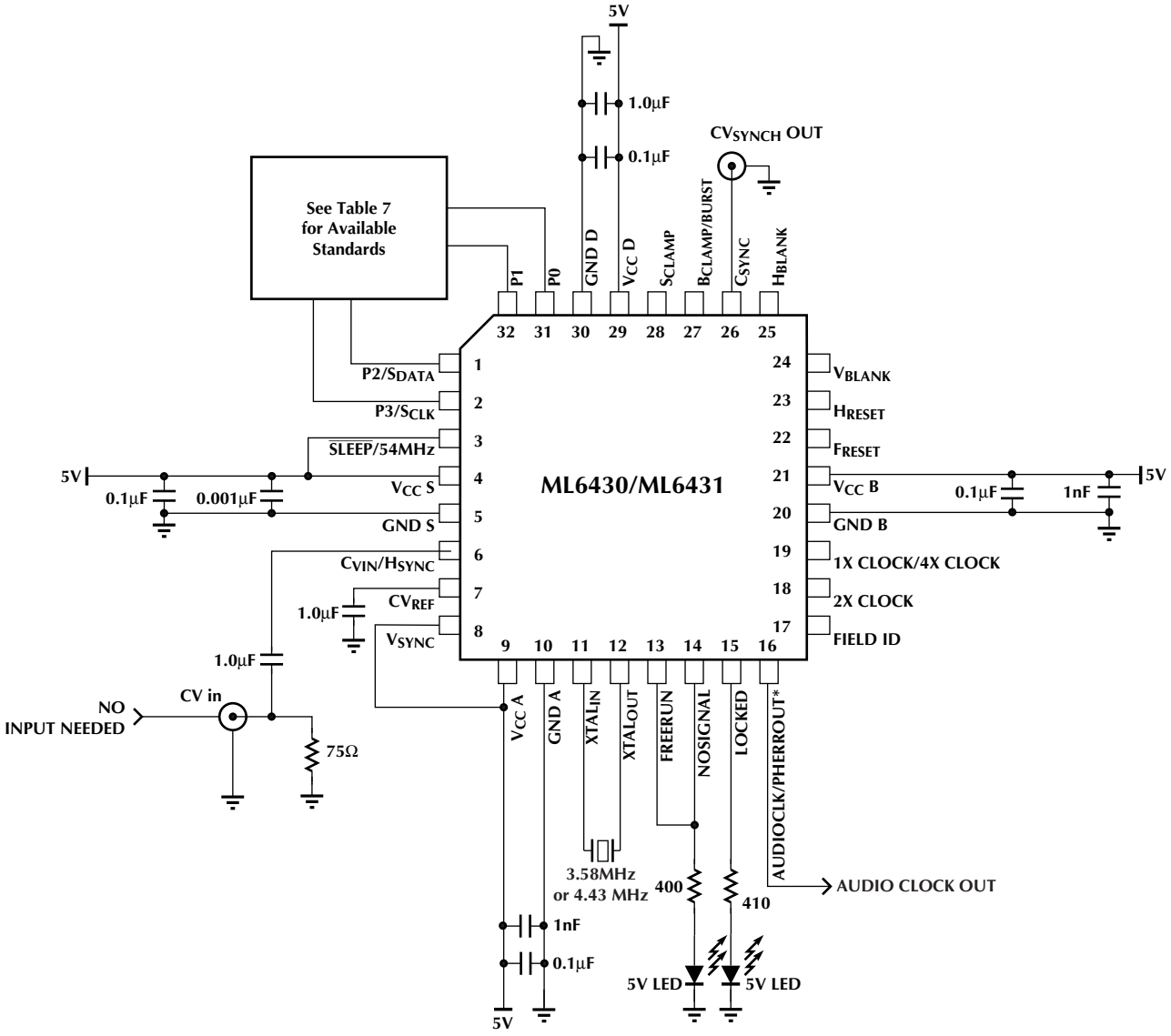
Note 1. For minimum V_{CC} bypassing, connect capacitors $V_{CC}A$ only. ($V_{CC}A$ to GND A)
*PHERROUT is only available with the ML6431

Figure 11. ML6431 in VGA Applications



Note 1. For minimum V_{CC} bypassing, connect capacitors V_{CC}A only. (V_{CC}A to GND A)
Note 2. See Table 4 for audio clock frequencies and registers
*PHERROUT is only available with the ML6431

Figure 12. ML6430/ML6431 in Audio Applications



Note 1. For minimum V_{CC} bypassing, connect capacitors V_{CC}A only. (V_{CC}A to GND A)
Note 2. See Table 4 for audio clock frequencies and registers
*PHERROUT is only available with the ML6431

Figure 13. ML6430/ML6431 in Pulse Generator Applications

NTSC AT SQUARE PIXEL RATE

SYMBOL	NAME: DESCRIPTION	CCIR 601STD	TYP	UNITS
N_{HA}	Clocks per H: Active	640	648	cycles
N_H	Clocks per H: Whole Line	780	780	cycles
N_{VA}	H per Frame: Active	486	493,507	lines
N_V	H per Frame: Whole Line	525	525	lines
N_{VBLKW}	Lines of Blanking: Wide	16	15	lines
N_{VBLKN}	Lines of Blanking: Narrow	9	9	lines
t_H	H Line Time	63.55	63.55	µs
t_{HS}	H Sync Time	0.0	0.0	µs
t_{HSW}	H Sync Width	4.7	4.73	µs
t_{HRW}	H Reset Width		41	µs
t_{HEQW}	Equalizer Sync Width	2.35	2.28	µs
t_{HSERRW}	Serration Sync Width		27.05	µs
t_{HSTC}	Sync Tip Clamp Pulse	300	122	ns
t_{HSTCW}	Sync Tip Clamp Width	1.5	1.47	µs
t_{HBPC}	BurstPulse	300	326	ns
t_{HBPGW}	BurstWidth	2.51	2.44	µs
t_{HBPCW}	B Clamp Width	4.0	3.91	µs
t_{HBLK}	H Blanking Pulse	–1.5	–1.39	µs
t_{HBLKW}	H Blanking Pulse Width	10.9	10.76	µs

PAL AT SQUARE PIXEL RATE

SYMBOL	NAME: DESCRIPTION	CCIR 601STD	TYP	UNITS
N_{HA}	Clocks per H: Active	768	767	cycles
N_H	Clocks per H: Whole Line	944	944	cycles
N_{VA}	H per Frame: Active		609, 616	lines
N_V	H per Frame: Whole Line	625	625	lines
N_{VBLKW}	Lines of Blanking: Wide		15	lines
N_{VBLKN}	Lines of Blanking: Narrow		9	lines
t_H	H Line Time	64.0	64.0	µs
t_{HS}	H Sync Time	0.0	0.0	µs
t_{HSW}	H Sync Width	4.7	4.68	µs
t_{HRW}	H Reset Width		34	µs
t_{HEQW}	Equalizer Sync Width	2.35	2.31	µs
t_{HSERRW}	Serration Sync Width	27.3	27.32	µs
t_{HSTC}	Sync Tip Clamp Pulse	300	102	ns
t_{HSTCW}	Sync Tip Clamp Width	1.5	1.49	µs
t_{HBPC}	BurstPulse	300	339	ns
t_{HBPGW}	BurstWidth	2.43	2.44	µs
t_{HBPCW}	B Clamp Width	4.0	4.0	µs
t_{HBLK}	H Blanking Pulse	–1.5	–1.49	µs
t_{HBLKW}	H Blanking Pulse Width	12.0	12.0	µs

Table 12. Pulse Output Timing

NTSC AT 4 X FS RATE

SYMBOL	NAME: DESCRIPTION	CCIR 601STD	TYP	UNITS
N_{HA}	Clocks per H: Active	768	752	cycles
N_H	Clocks per H: Whole Line	910	910	cycles
N_{VA}	H per Frame: Active	486	493,507	lines
N_V	H per Frame: Whole Line	525	525	lines
N_{VBLKW}	Lines of Blanking: Wide	16	15	lines
N_{VBLKN}	Lines of Blanking: Narrow	9	9	lines
t_H	H Line Time	63.55	63.55	µs
t_{HS}	H Sync Time	0.0	0.0	µs
t_{HSW}	H Sync Width	4.7	4.68	µs
t_{HRW}	H Reset Width		35	µs
t_{HEQW}	Equalizer Sync Width	2.35	2.30	µs
t_{HSERRW}	Serration Sync Width	27.05	27.02	µs
t_{HSTC}	Sync Tip Clamp Pulse	300	105	ns
t_{HSTCW}	Sync Tip Clamp Width	1.5	1.47	µs
t_{HBPC}	BurstPulse	300	349	ns
t_{HBPGW}	BurstWidth	2.51	2.51	µs
t_{HBPCW}	B Clamp Width	4.0	3.98	µs
t_{HBLK}	H Blanking Pulse	–1.5	–1.54	µs
t_{HBLKW}	H Blanking Pulse Width	10.9	11.03	µs

PAL AT 4 X FS RATE

SYMBOL	NAME: DESCRIPTION	CCIR 601STD	TYP	UNITS
N_{HA}	Clocks per H: Active	922	922	cycles
N_H	Clocks per H: Whole Line	1135.0064	1135	cycles
N_{VA}	H per Frame: Active		609, 616	lines
N_V	H per Frame: Whole Line	625	625	lines
N_{VBLKW}	Lines of Blanking: Wide		15	lines
N_{VBLKN}	Lines of Blanking: Narrow		9	lines
t_H	H Line Time	64.0	64.0	µs
t_{HS}	H Sync Time	0.0	0.0	µs
t_{HSW}	H Sync Width	4.7	4.74	µs
t_{HRW}	H Reset Width		28	µs
t_{HEQW}	Equalizer Sync Width	2.35	2.25	µs
t_{HSERRW}	Serration Sync Width	27.3	27.29	µs
t_{HSTC}	Sync Tip Clamp Pulse	300	169	ns
t_{HSTCW}	Sync Tip Clamp Width	1.5	1.58	µs
t_{HBPC}	BurstPulse	300	225	ns
t_{HBPGW}	BurstWidth	2.43	2.48	µs
t_{HBPCW}	B Clamp Width	4.0	4.06	µs
t_{HBLK}	H Blanking Pulse	–1.5	–1.52	µs
t_{HBLKW}	H Blanking Pulse Width	12.0	12.12	µs

Table 12. Pulse Output Timing (Continued)

NTSC AT CCIR601 RATE

SYMBOL	NAME: DESCRIPTION	CCIR 601STD	TYP	UNITS
N_{HA}	Clocks per H: Active	720	709	cycles
N_H	Clocks per H: Whole Line	858	858	cycles
N_{VA}	H per Frame: Active	486	493, 507	lines
N_V	H per Frame: Whole Line	525	525	lines
N_{VBLKW}	Lines of Blanking: Wide	16	15	lines
N_{VBLKN}	Lines of Blanking: Narrow	9	9	lines
t_H	H Line Time	63.55	63.55	µs
t_{HS}	H Sync Time	0.0	0.0	µs
t_{HSW}	H Sync Width	4.7	4.67	µs
t_{HRW}	H Reset Width		37	µs
t_{HEQW}	Equalizer Sync Width	2.35	2.37	µs
t_{HSERRW}	Serration Sync Width	27.05	27.04	µs
t_{HSTC}	Sync Tip Clamp Pulse	300	111	ns
t_{HSTCW}	Sync Tip Clamp Width	1.5	1.48	µs
t_{HBPC}	BurstPulse	300	370	ns
t_{HBPGW}	BurstWidth	2.51	2.44	µs
t_{HBPCW}	B Clamp Width	4.0	4.10	µs
t_{HBLK}	H Blanking Pulse	–1.5	–1.55	µs
t_{HBLKW}	H Blanking Pulse Width	10.9	11.03	µs

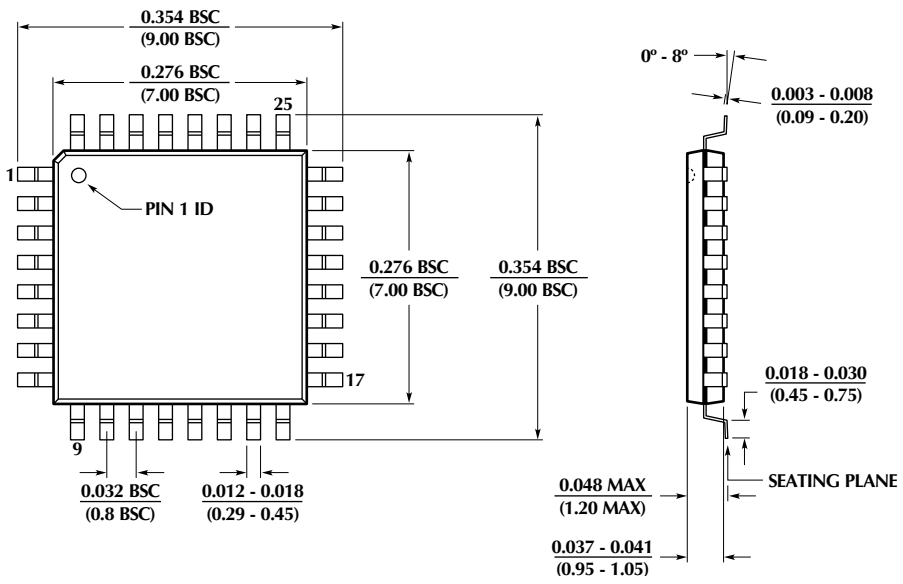
PAL AT CCIR601 RATE

SYMBOL	NAME: DESCRIPTION	CCIR 601STD	TYP	UNITS
N_{HA}	Clocks per H: Active	720	702	cycles
N_H	Clocks per H: Whole Line	864	864	cycles
N_{VA}	H per Frame: Active		609, 616	lines
N_V	H per Frame: Whole Line	625	625	lines
N_{VBLKW}	Lines of Blanking: Wide		15	lines
N_{VBLKN}	Lines of Blanking: Narrow		9	lines
t_H	H Line Time	64.0	64.0	µs
t_{HS}	H Sync Time	0.0	0.0	µs
t_{HSW}	H Sync Width	4.7	4.67	µs
t_{HRW}	H Reset Width		37	µs
t_{HEQW}	Equalizer Sync Width	2.35	2.30	µs
t_{HSERRW}	Serration Sync Width	27.30	27.33	µs
t_{HSTC}	Sync Tip Clamp Pulse	300	111	ns
t_{HSTCW}	Sync Tip Clamp Width	1.5	1.48	µs
t_{HBPC}	BurstPulse	300	370	ns
t_{HBPGW}	BurstWidth	2.43	2.44	µs
t_{HBPCW}	B Clamp Width	4.0	4.0	µs
t_{HBLK}	H Blanking Pulse	–1.5	–1.48	µs
t_{HBLKW}	H Blanking Pulse Width	12.0	12.0	µs

Table 12. Pulse Output Timing (Continued)

PHYSICAL DIMENSIONS inches (millimeters)

Package: H32-7
32-Pin (7 x 7 x 1mm) TQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6430CH	0°C to 70°C	32-Pin TQFP (H32-7)
ML6431CH (EOL)	**0°C to 70°C**	**32-Pin TQFP (H32-7)**

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