

**PRELIMINARY**  
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 some parametric limits are subject to change.

MITSUBISHI SOUND PROCESSOR

# M62420SP/FP

SOUND CONTROLLER FOR TV

## Tone and Volume Controller by I<sup>2</sup>C Bus System

### OUTLINE

M62420SP/FP is the tone and volume controller which is controlled by I<sup>2</sup>C bus. This IC can apply the broad application because of low noise and distortion.

### FEATURE

- TONE(Bass/Treble) control and 1dB step volume control are enabled .
- Low noise and low distortion .  
 $V_{NO} = 4.5\mu V_{rms}$ ,  $CTHD = 0.1\%$  max
- Controlling by serial data in conformity to the I<sup>2</sup>C bus format .

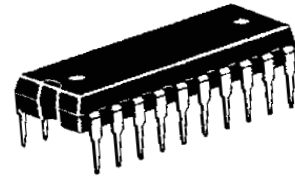
### APPLICATION

- TV, Mini-Stereo , etc

### RECOMMENDED OPERATING CONDITION

- |                       |                   |                    |
|-----------------------|-------------------|--------------------|
| •Supply voltage range | 8.5~9.5V (analog) | 4.5~5.5V (digital) |
| •Rated supply voltage | 9V (analog)       | 5V (digital)       |

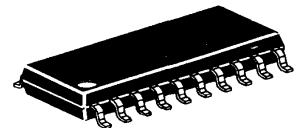
### PACKAGE OUTLINE



**20 P 4 B ( SP )**

PITCH : 1.78 mm

SIZE : 19.0 mm X 6.3 mm X 3.3 mm

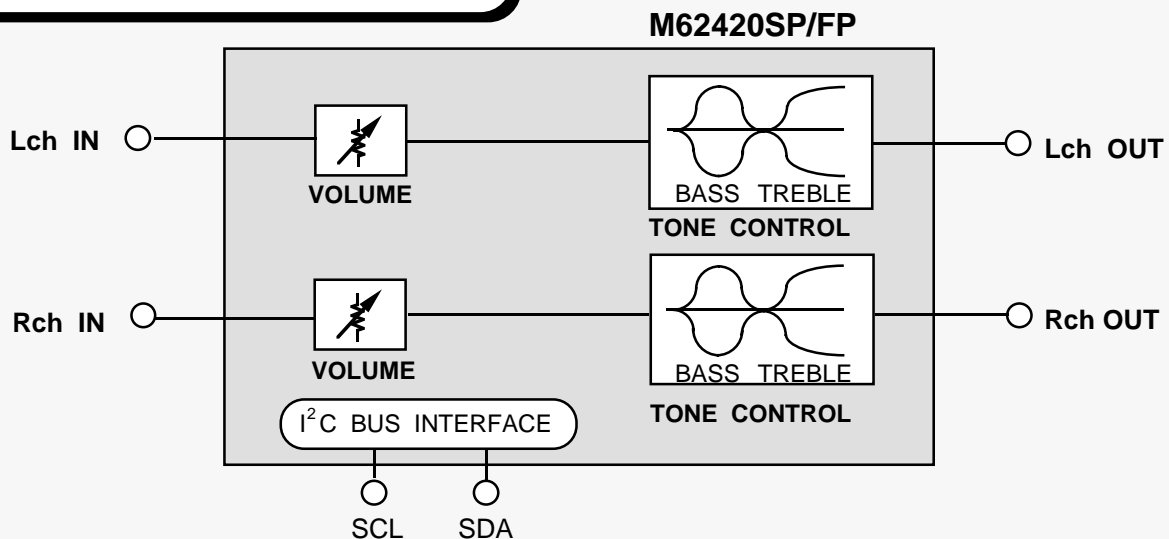


**20 P 2 N ( FP )**

PITCH : 1.27 mm

SIZE : 5.3 mm X 12.6 mm X 1.8 mm

### SYSTEM BLOCK DIAGRAM



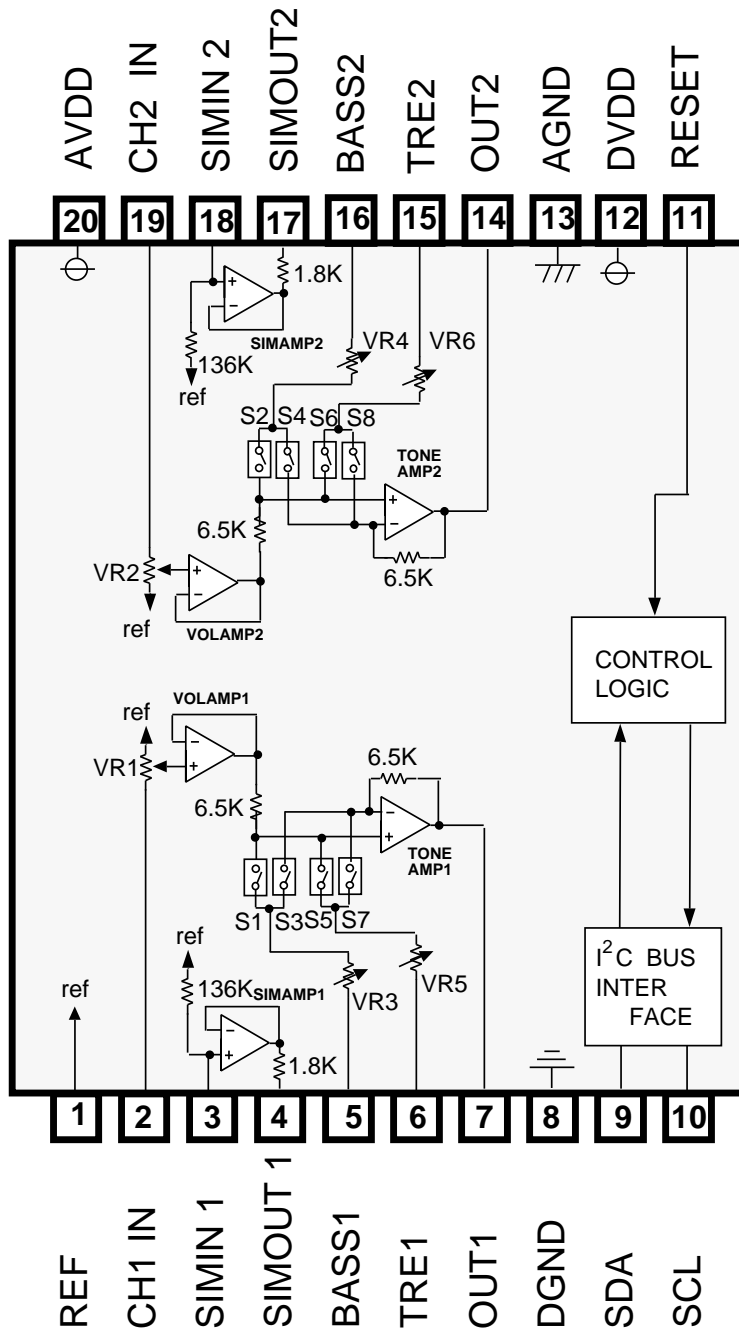
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## BLOCK DIAGRAM



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SOUND CONTROLLER FOR TV

## PIN DESCRIPTION

PIN No.	PIN NAME	I/O	DESCRIPTION
1	REF	I	Reference voltage terminal for analog
2	CH1 IN	I	Input terminal (ch1)
3	SIMIN 1	I	Pin for capacitor of simulated inductor 1
4	SIMOUT 1	O	Pin for capacitor of simulated inductor 1
5	BASS1	I	Pin for capacitor of ch1-side bass setting
6	TRE1	I	Pin for capacitor of ch1-side treble setting
7	VOL OUT1	O	Output terminal (ch1)
8	DGND	I	Digital GND
9	SDA	I/O	I/O terminal of DATA I <sup>2</sup> C bus format
10	SCL	I	Input terminal of CLOCK I <sup>2</sup> C bus format
11	RESET	I	RESET terminal of built-in logic circuit
12	DVDD	I	VDD for digital circuit
13	AGND	I	GND for analog circuit
14	VOL OUT2	O	Output terminal (ch2)
15	TRE2	I	Pin for capacitor of ch2-side treble setting
16	BASS2	I	Pin for capacitor of ch2-side bass setting
17	SIMOUT2	O	Pin for capacitor of simulated inductor 2
18	SIMIN 2	I	Pin for capacitor of simulated inductor 2
19	CH2 IN	I	Input terminal (ch2)
20	AVDD	I	VCC for analog circuit

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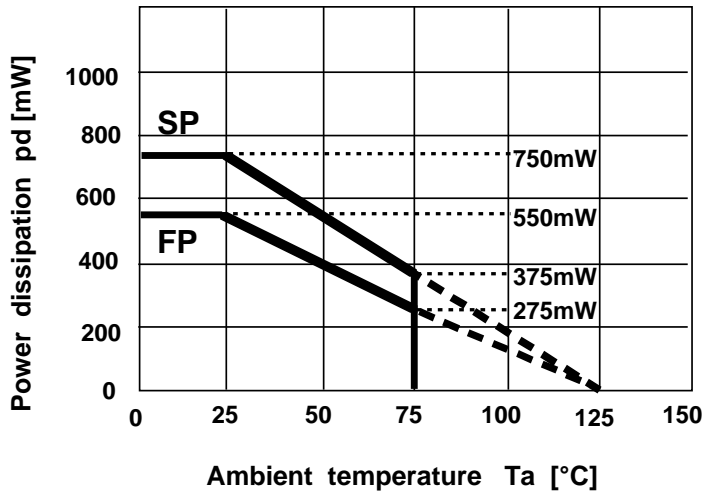
# M62420SP/FP

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## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITION	LIMITS	UNIT
AVdd	Analog supply voltage		10.0	V
DVdd	Digital supply voltage		7.0	V
Pd	Power dissipation	Ta ≤ 25°C	750	mW
Kθ	Thermal Derating ratio	Ta > 25°C	7.5	mW/°C
Topr	Operating temperature		-20~+75	°C
Tstg	Storage temperature		-40~+125	°C

### Thermal Derating



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SOUND CONTROLLER FOR TV

## RECOMMENDED OPERATING CONDITION

( Ta=25°C unless otherwise noted )

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD		8.5	9.0	9.5	V
Digital supply voltage	DVDD		4.5	5.0	5.5	V
H level input voltage (logic circuit)	VIH		0.7 DVDD	—	VDD	V
L level input voltage (logic circuit)	VIL		0	—	0.3 DVDD	V

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## ELECTRIC CHARACTERISTICS

( Ta=25°C, AVDD=9V,DVDD=5V and tone,bassboost=0dB unless otherwise noted )

### ( 1 ) SUPPLY VOLTAGE

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Analog supply current	Icc	•AVdd=9.0V •mesure terminal=20 pin •no signal input	—	10	20	mA
Digital supply current	Idd	•DVdd= 5V •mesure terminal=12 pin •no signal input	—	0	2	μA

### ( 2 ) I / O CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Maximum input voltage	VIM	2,19pin input,7,14pin output RL=10K , THD=1%,f=1kHz ATT=-6dB	2.0	3.2	—	Vrms
Output voltage	Vodc	7pin,14pin, no signal	4.35	4.5	4.65	V
Gain	Gv	Vin=0dBm,FLAT,f=1kHz 2- 7PIN 19-14PIN gain	-2	0	2	dB
Output noise voltage	Vono	JIS-A filter no signal Rg=10K 7,14pin	—	4.5	30	μ Vrms
Total harmonic distortion	THD	7pin,14pin f=1kHz Vo=0.5Vrms , RL=10K LPF=30kHz	—	0.05	0.1	%
Channel separation	CT	RL=10K S:Vin=1Vrms,f=1kHz M:Rg=10k ,JIS-A filter	—	-100	-70	dB

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### ( 3 ) TONE CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Tone controll gain (bass)	Gbassb	f=100Hz	9	12	15	dB
	Gbassc		-15	-12	-9	dB
Tone controll gain (treble)	Gtrebb	f=10KHz	9	12	15	dB
	Gtrebc		-15	-12	-9	dB

### ( 4 ) VOLUME CHARACTERISTICS

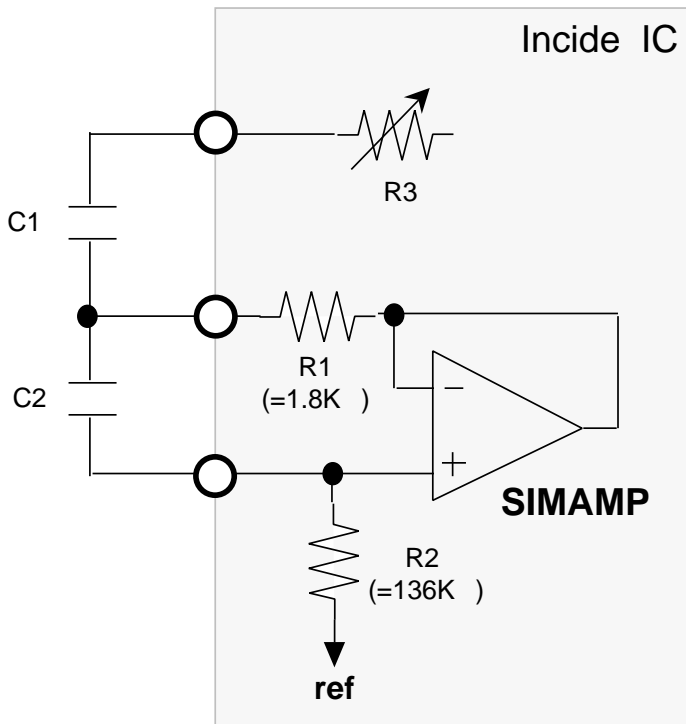
ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Maximum attenuation	ATTmax	f=1KHz, Vin=0dBm 2pin~7pin	-108	-100	-80	dB
Minimum attenuation	ATTmin	19pin~14pin gain JIS-A filter	-1.5	0	1.5	dB

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**FUNCTION EXPLANATION**

( 1 ) EQUIVARATION CIRCUIT OF TONE CONTROL

The resonance circuit is able to construct by using built-in amplifier for simurated inductor. (Shows the constant as follow)



Center frequency

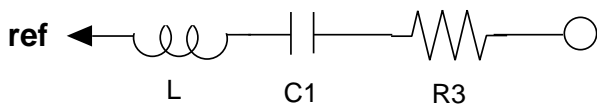
$$f_0 = 1 / 2 \sqrt{C1 \cdot C2 \cdot R1 \cdot R2} \text{ [Hz]}$$

$$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$$

( EX ) BASS band ( f=100Hz )  
 R1=1.8K , R2=136K  
 C1=0.47μ , C2=0.022μ

FIG1. The circuit used simurated inductor.

FIG1 is equal to FIG2.  
 The following relation is concluded.



$$L = C2 \cdot ER1 \cdot ER2$$

FIG2. The equivalent circuit used L.



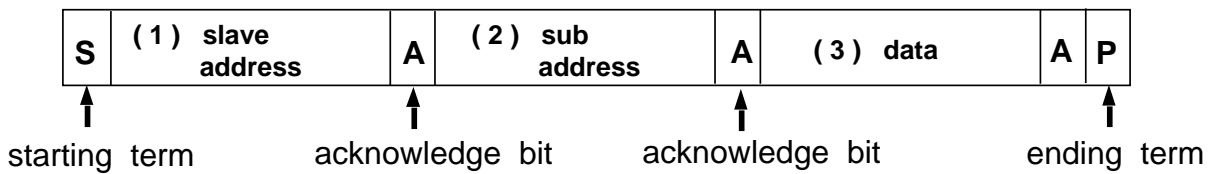
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SOUND CONTROLLER FOR TV

## I<sup>2</sup>C BUS INPUT DATA FORMAT

← Input direction



### ( 1 ) slave address

The following slave address is assigned at this IC.

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	

### ( 2 ) sub address

The following sub address is defined at this IC.

subA7	subA6	subA5	subA4	subA3	subA2	subA1	subA0
← empty slot →			MUTE mode	TREBLE level mode	BASS level mode	channel2 volume mode	channel1 volume mode
			1: ON 0: OFF	1: ON 0: OFF	1: ON 0: OFF	1: ON 0: OFF	1: ON 0: OFF

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SOUND CONTROLLER FOR TV

### (3) -1: volume control

The volume control is enabled at following condition.

subA0 : 0 , 1 , 1  
 subA1 : 1 , 0 , 1 (either bit is 1)

subA2 : 0  
 subA3 : 0 (both bits are 0)

#### volume code

ATT	D4	D3	D2	D1	D0
0dB	H	H	H	H	H
2dB	H	H	H	H	L
4dB	H	H	H	L	H
6dB	H	H	H	L	L
8dB	H	H	L	H	H
10dB	H	H	L	H	L
12dB	H	H	L	L	H
14dB	H	H	L	L	L
16dB	H	L	H	H	H
18dB	H	L	H	H	L
20dB	H	L	H	L	H
22dB	H	L	H	L	L
24dB	H	L	L	H	H
26dB	H	L	L	H	L
28dB	H	L	L	L	H
30dB	H	L	L	L	L
32dB	L	H	H	H	H
34dB	L	H	H	H	L
36dB	L	H	H	L	H
38dB	L	H	H	L	L
40dB	L	H	L	H	H
42dB	L	H	L	H	L
46dB	L	H	L	L	H
50dB	L	H	L	L	L
54dB	L	L	H	H	H
58dB	L	L	H	H	L
62dB	L	L	H	L	H
66dB	L	L	H	L	L
70dB	L	L	L	H	H
74dB	L	L	L	H	L
78dB	L	L	L	L	H
dB	L	L	L	L	L

ATT	D6	D5
0dB	H	H
1dB	H	L
* 2dB	L	H
* 3dB	L	L

\* 2dB,3dB setting is enabled at less than 42dB step.

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## ( 4 ) -2 : tone level control

The tone level controlling is enabled at following condition.

subA0 :  0      (both bits are 0)      subA2 :  0 ,  1 ,  1  
 subA1 :  0      subA3 :  1 ,  0 ,  1      (either bit is 1)

### tone code

	BASS				TREBLE			
	D7	D6	D5	D4	D3	D2	D1	D0
12dB	L	H	H	L	L	H	H	L
10dB	L	H	L	H	L	H	L	H
8dB	L	H	L	L	L	H	L	L
6dB	L	L	H	H	L	L	H	H
4dB	L	L	H	L	L	L	H	L
2dB	L	L	L	H	L	L	L	H
0dB	L	L	L	L	L	L	L	L
-2dB	H	L	L	H	H	L	L	H
-4dB	H	L	H	L	H	L	H	L
-6dB	H	L	H	H	H	L	H	H
-8dB	H	H	L	L	H	H	L	L
-10dB	H	H	L	H	H	H	L	H
-12dB	H	H	H	L	H	H	H	L

non-used code      HHHH  
                                  LHHH  
                                  HLLL

## ( 5 ) -3 : Mute mode

The mute mode is enabled at following condition.

subA0 : no definition      subA2 : no definition      subA4 : 1  
 subA1 : no definition      subA3 : no definition

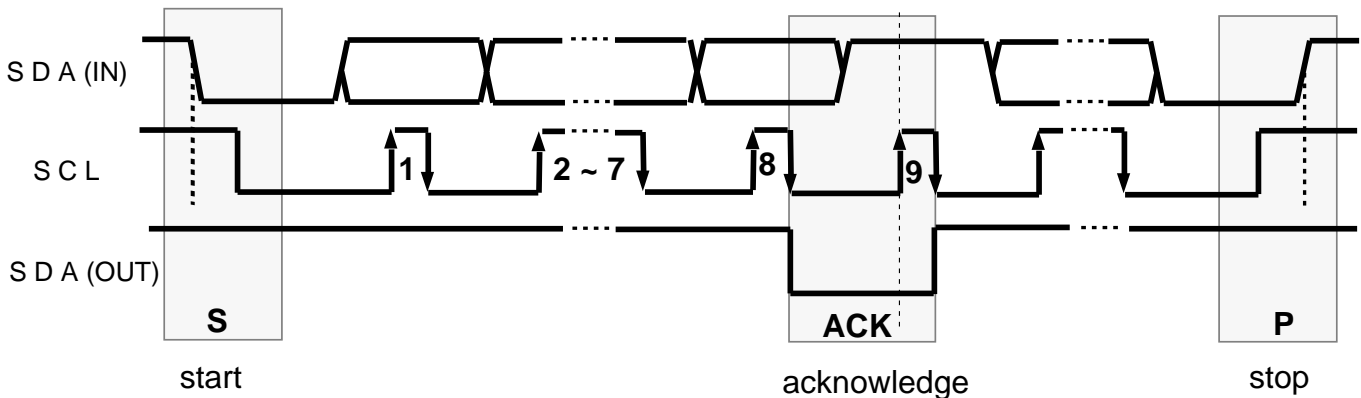
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## DATA and CLOCK



### start

This term is defined by SDA(in) falling edge at SCL H .

### stop

This term is defined by SDA(in) rising edge at SCL H .

### CAUTION

The SDA(IN) level never change at SCK=H  
except start and stop .

### data transmisson

The SDA(IN) is enabled at SCL rising edge and H .

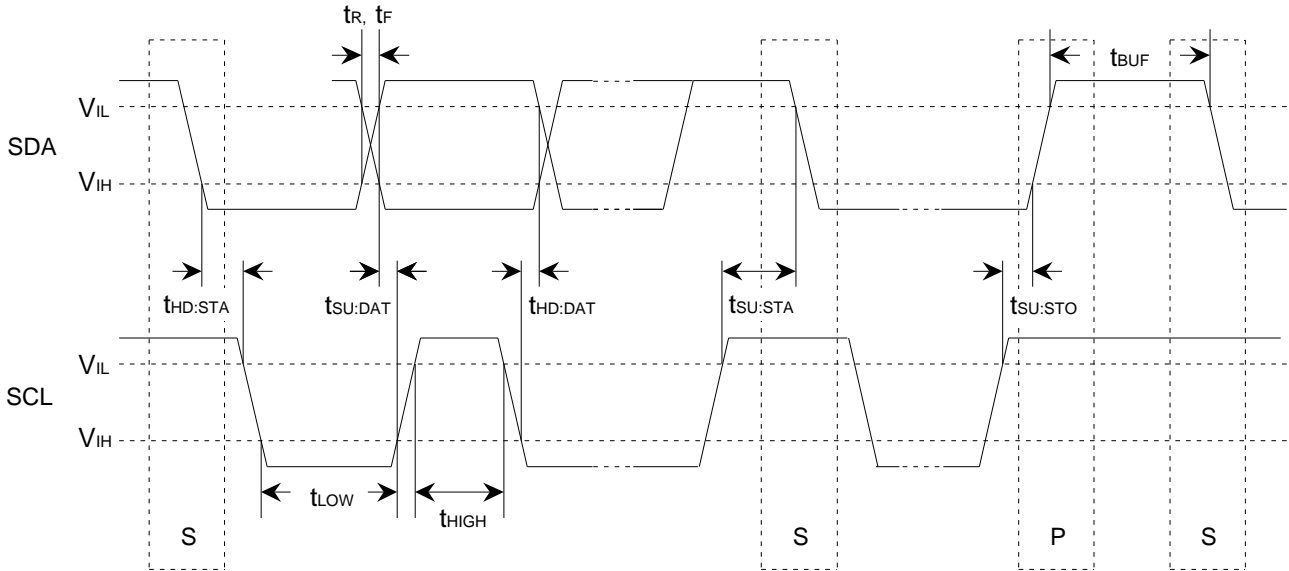
### acknowledge

Transmitter must send H during ninth clock pulse of SCL .

The case of finished receiving , the receiver replies L synchronized to falling edge of eighth pulse . And restart receiving the transmitted data synchronized to falling edge of ninth pulse .

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**BUS LINE TIMMING SPECIFICATION**



parameter	symbol	MIN	MAX	units
min. input low voltage	$V_{IL}$	-0.5	1.5	V
max. input high voltage	$V_{IH}$	3.0	5.5	V
SCL clock frequency	$f_{SCL}$	0	100	KHz
Time the bus must be free before a new transmission can start	$t_{BUF}$	4.7	-	$\mu s$
Hold time start condition. After this period the first clock pulse is generated	$t_{HD:STA}$	4.0	-	$\mu s$
The LOW preiod of the clock	$t_{LOW}$	4.7	-	$\mu s$
The HIGH period of the clock	$t_{HIGH}$	4.0	-	$\mu s$
Set up time for start condition ( Only relevant for a repeated start condition )	$t_{SU:STA}$	4.7	-	$\mu s$
Hold time DATA	$t_{HD:DAT}$	0	-	$\mu s$
Set-up time DATA	$t_{SU:DAT}$	250	-	ns
Rise time of both SDA and SCL lines	$t_R$	-	1000	ns
Fall time of both SDA and SCL lines	$t_F$	-	300	ns
Set-up time for stop condition	$t_{SU:STO}$	4.0	-	$\mu s$

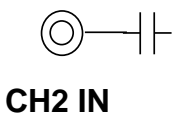
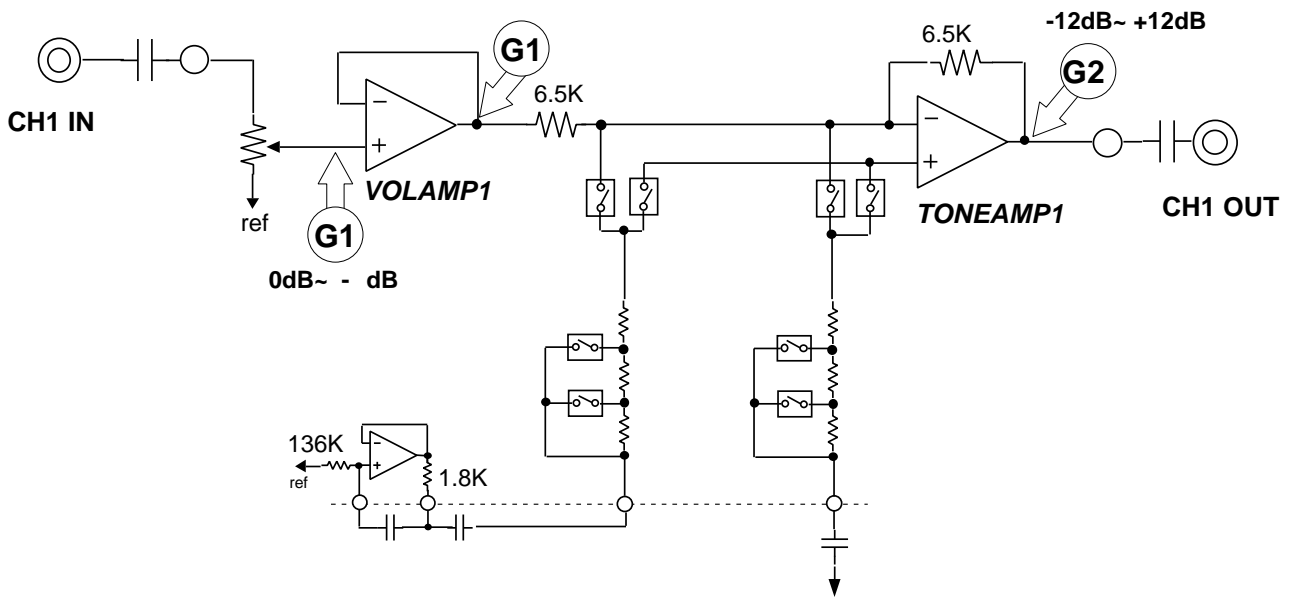
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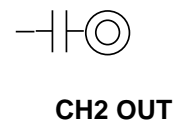
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## LEVEL DIAGRAM



same to CH1



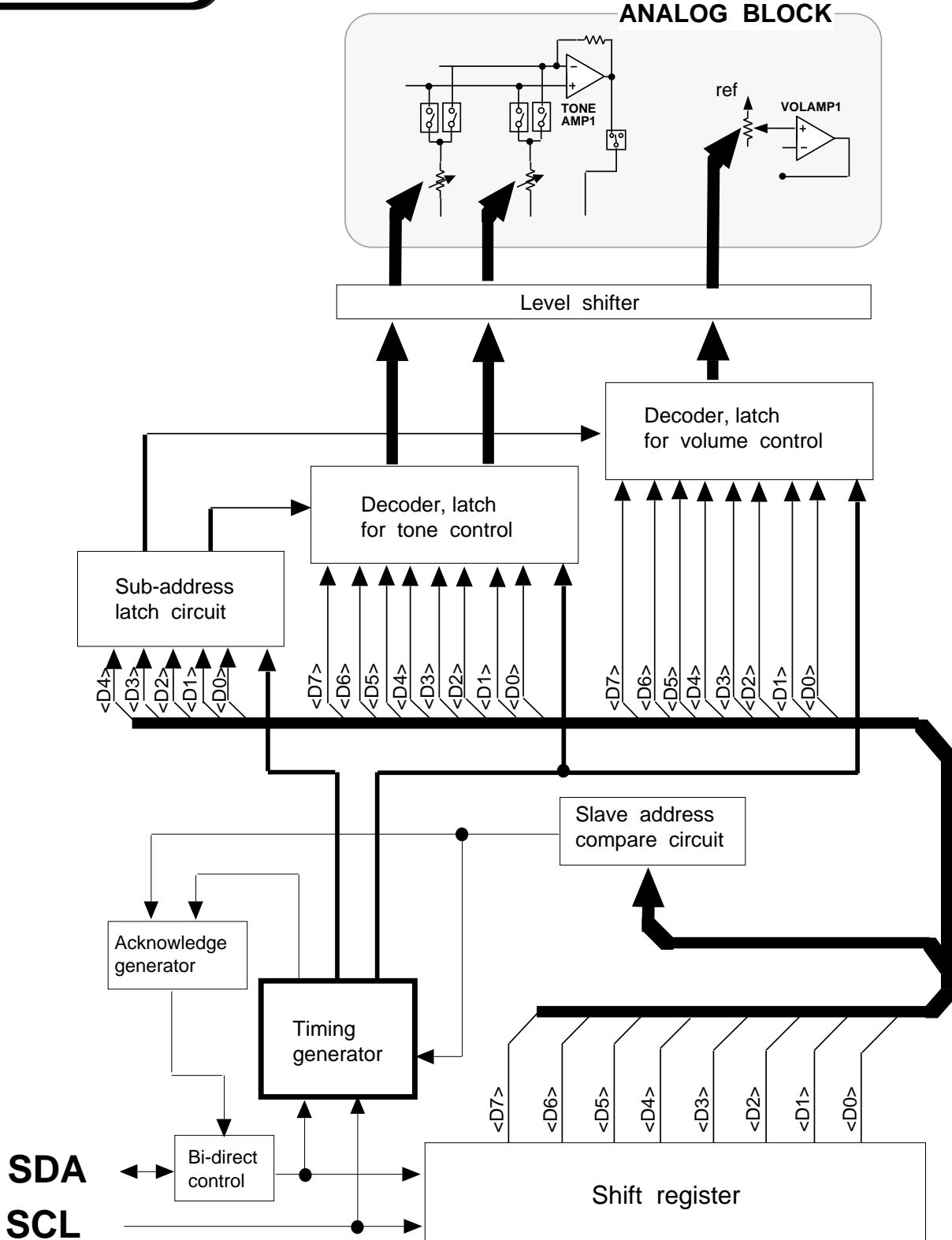
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## LOGIC CIRCUIT



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## APPLICATION EXAMPLE

