

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2224/EL2224C

Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

ELANTEC INC

T-79-25

EL2224/EL2224C

1

Features

- Unity gain stable
- Wide bandwidth—60 MHz
- High slew rate—200 V/ μ s
- High power bandwidth ($\pm 10 V_{out}$) 3 MHz
- Large open loop gain 75 dB
- Low power—5 mA/amplifier
- Low input offset—1 mV typ.
- Wide supply voltage range $V_s = \pm 5V$ to $\pm 15V$
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers

Ordering Information

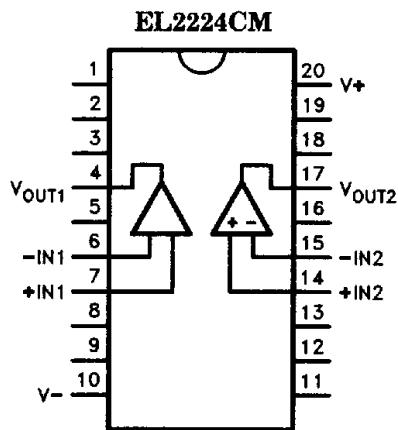
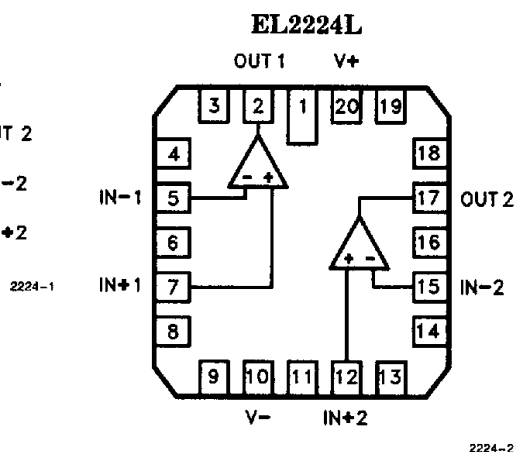
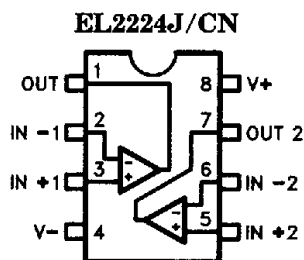
Part No.	Temp. Range	Package	Outline #
EL2224CJ	0°C to +75°C	CerDIP	MDP0010
EL2224CN	0°C to +75°C	P-DIP	MDP0031
EL2224J	-55°C to +125°C	CerDIP	MDP0010
EL2224J/883B	-55°C to +125°C	CerDIP	MDP0010
EL2224L/883B	-55°C to +125°C	LCC	MDP0007
EL2224CM	0°C to +75°C	SOL	MDP0027

General Description

The EL2224 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This amplifier features unity gain stability, high slew rate and wide bandwidth, along with an excellent speed power relationship. The dual 60 MHz EL2224 consumes only 10 mA, making it ideal for video applications. The EL2224 has short circuit protected outputs and will operate from $\pm 5V$ to $\pm 15V$. It is fabricated using Elantec's Complementary Bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: "Elantec's Military Processing, Monolithic Integrated Circuits".

Connection Diagrams



This product covered under U.S. Patent No. 4,837,523

July 1991 Rev B

EL2224/EL2224C

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Dual, 60 MHz, Unity Gain Stable, Operational Amplifier**Absolute Maximum Ratings** ($T_A = 25^\circ\text{C}$)

Voltage Between V+ and V-	35V	Operational Temperature Range	
Differential Input Voltage	$\pm 6\text{V}$	EL2224	-55°C to $+125^\circ\text{C}$
Internal Power Dissipation	See Curves	EL2224C	0°C to $+75^\circ\text{C}$
Peak Output Current	Short Circuit Protected	Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Output Short Circuit Duration (Note 1)	Continuous	Maximum Junction Temperature	
		CerDIP, LCC	175°C
		Plastic DIP, SOL	150°C
		Lead Temperature	
		DIP Package	300°C
		SOL Package	
		Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

DC Electrical Characteristics $V_S = \pm 15\text{V}$; $R_L = 2\text{k}\Omega$, unless otherwise specified

Parameter	Description	EL2224					EL2224C				Units
		Temp	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V _{OS}	Offset Voltage	+25°C		0.5	5	I		0.5	5	I	mV
		Full			8	I			8	III	mV
TCV _{OS}	Average Offset Voltage Drift	Full		20		V		20		V	$\mu\text{V}/^\circ\text{C}$
I _B	Bias Current	+25°C		1.5	4	I		1.5	4	I	μA
		Full			6	I			6	III	μA
I _{OS}	Offset Current	+25°C		0.2	2	I		0.2	2	I	μA
		Full			3	I			3	III	μA
R _{IN}	Input Resistance	+25°C		40		V		40		V	k Ω
C _{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V _{CM}	Common Mode Input Range	Full	± 10	± 12		I	± 10	± 12		II	V
e _{IN}	Input Noise Voltage ($f = 1\text{ kHz}$, $R_G = 0\Omega$)	+25°C		15		V		15		V	$\text{nV}/\sqrt{\text{Hz}}$
A _{VOL}	Large Signal Voltage Gain (Notes 2, 3)	+25°C	4k	6k		I	4k	6k		I	V/V
		Full	2.5k				2.5k			III	V/V

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EL2224/EL2224C**Dual, 60 MHz, Unity Gain Stable, Operational Amplifier**

EL2224/EL2224C

DC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2 k\Omega$, unless otherwise specified — Contd.

Parameter	Description	EL2224					EL2224C				Units
		Temp	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	80		I	60	80		II	dB
V_O	Output Voltage Swing	Full	± 11	± 12.5		I	± 11	± 12.5		II	V
I_{SC}	Short Circuit Current	25°C		± 50	± 70	I		± 50	± 70	I	mA
R_O	Output Resistance	25°C		40		V		40		V	Ω
I_s	Supply Current	Full		9.5	13	I		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	60	75		I	60	75		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2 k\Omega$, unless otherwise specified

Parameter	Description	EL2224					EL2224C				Units
		Temp	Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	25°C		60		V		60		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	25°C	2.4	3.1		I	2.4	3.1		I	MHz
t_r	Rise Time (Note 8)	25°C		6		V		6		V	ns
OS	Overshoot (Note 8)	25°C		20		V		20		V	%
SR	Slew Rate (Note 8)	25°C	150	200		I	150	200		I	V/ μ s
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%	25°C		120		V		120		V	ns
Ch S_p	Channel Separation ($f = 10$ MHz)	Full		70		V		70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: $V_O = \pm 10V$.Note 3: $R_L = 2 k\Omega$.Note 4: Two tests are performed. $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0$ to $-10V$.Note 5: Two tests are performed. $V_+ = 15V$, and V_- is changed from $-5V$ to $-15V$. $V_- = -15V$, and V_+ is changed from $+5V$ to $+15V$.Note 6: $V_O = 100$ mV.Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \text{Slew Rate} / 2 \pi V_{PEAK}$.

Note 8: Refer to Test Circuit section of data sheet.

Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.

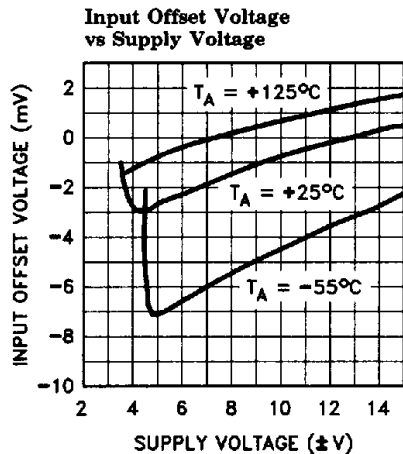
Note 10: $A_V = +1$, $R_L = 2 k\Omega$.

EL2224/EL2224C

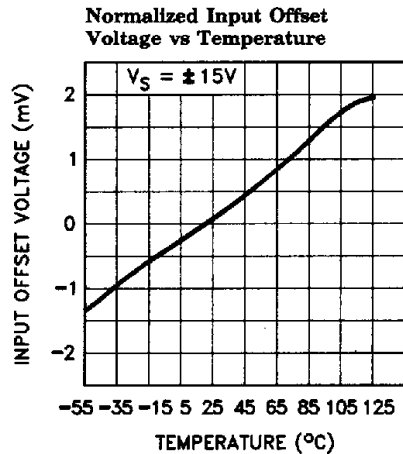
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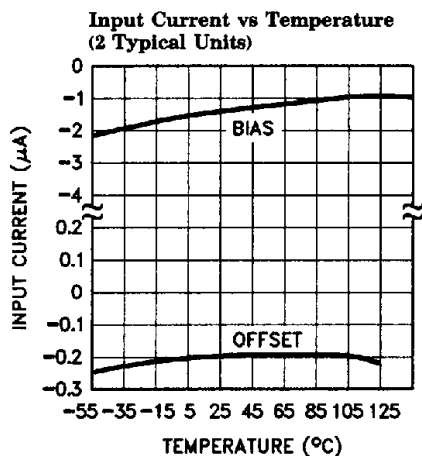
Typical Performance Curves



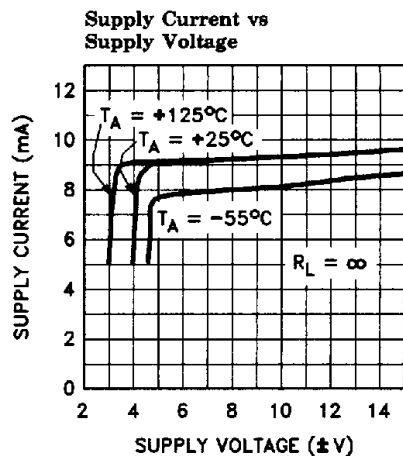
2224-4



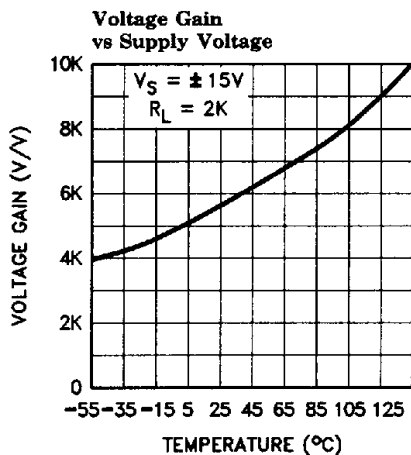
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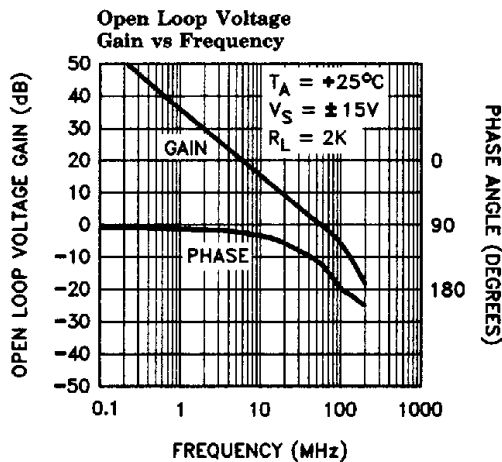
2224-6



2224-7



2224-8



2224-9

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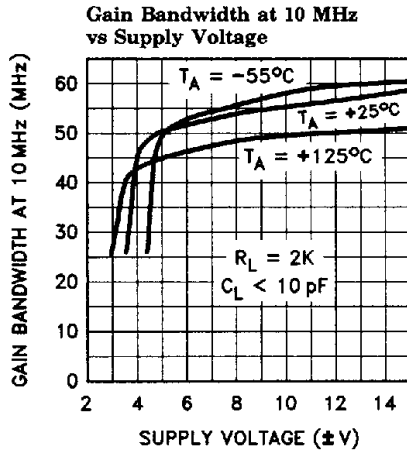
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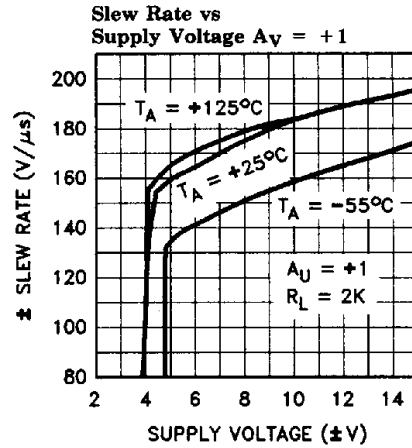
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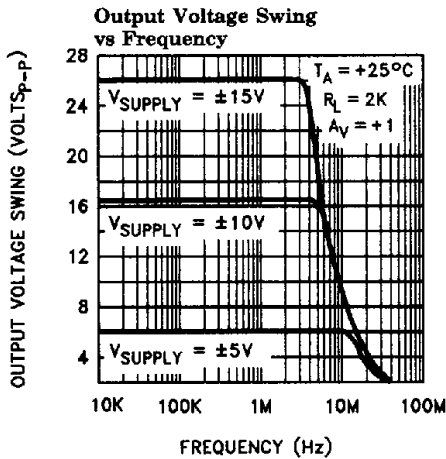
Typical Performance Curves — Contd.



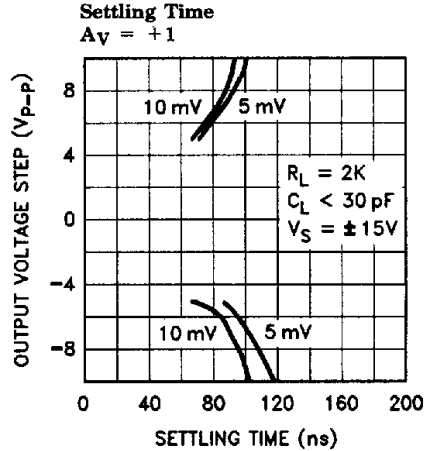
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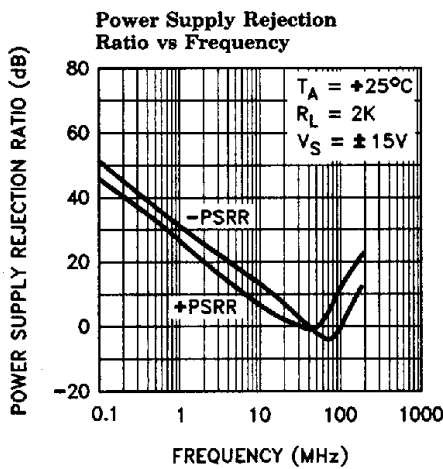
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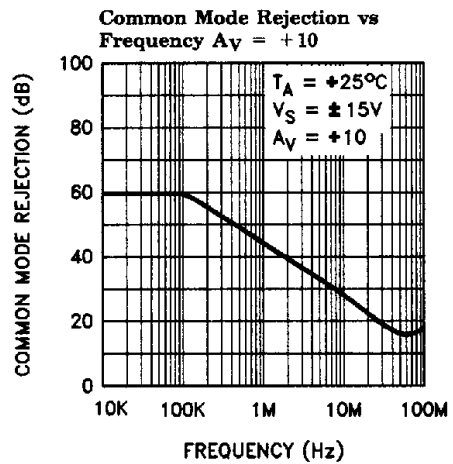
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2224-13



2224-14

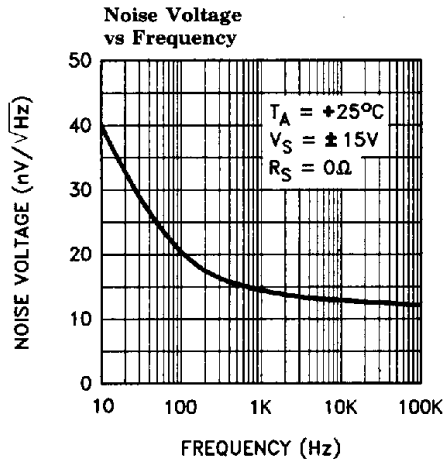


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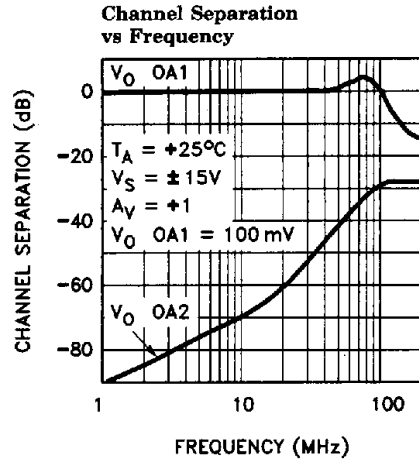
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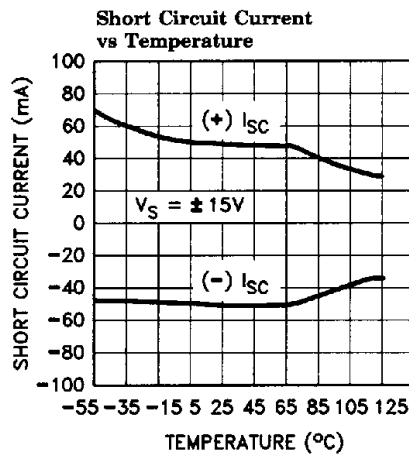
Typical Performance Curves — Contd.



2224-16

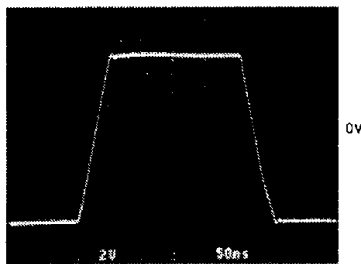


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2224-18

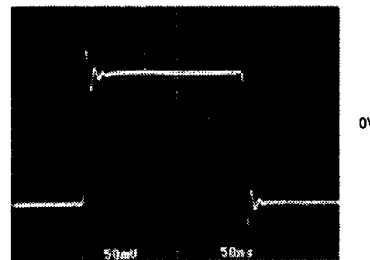
Large Signal Response



$A_V = +1$
 $V_{IN} = \pm 5\text{V}$
 $V_O = \pm 5\text{V}$
 $R_L = 2\text{k}$

2224-19

Small Signal Response



$A_V = +1$
 $V_{IN} = \pm 100 \text{ mV}$
 $V_O = \pm 100 \text{ mV}$
 $R_L = 2\text{k}$

2224-20

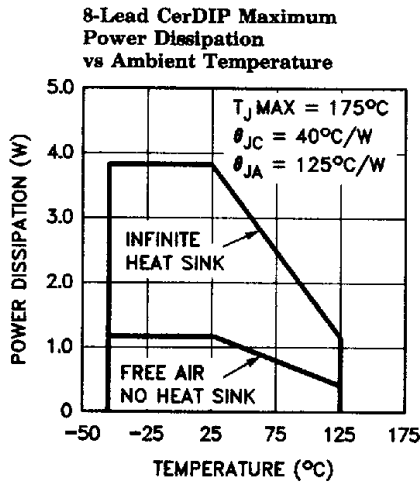
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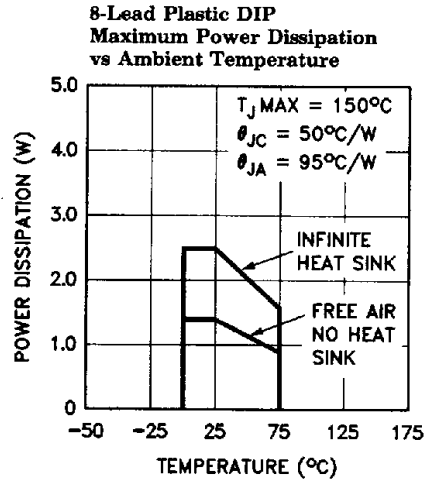
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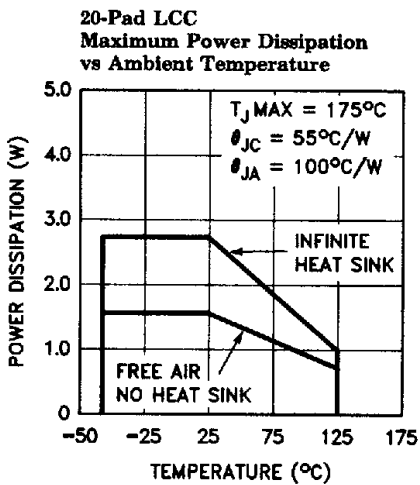
Typical Performance Curves — Contd.



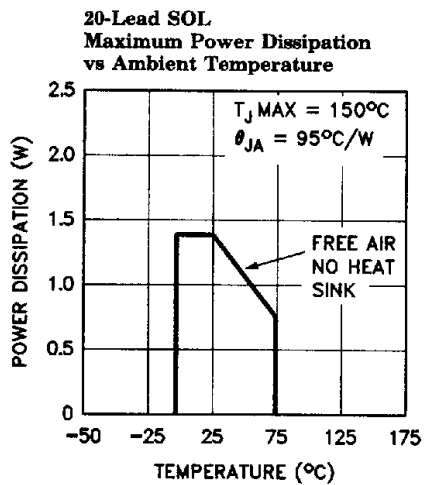
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2224-22

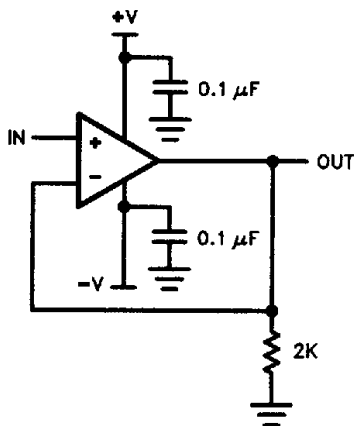


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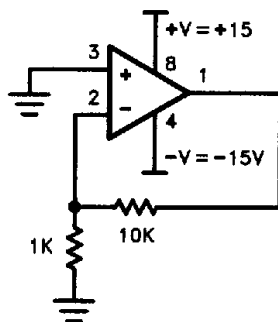
2224-24

Test Circuit



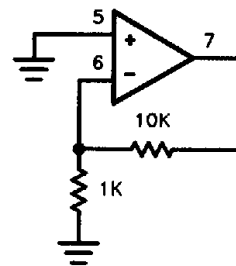
2224-27

Burn-In Circuit



2224-28

Pin numbers are for the 8-lead CerDIP.
 Burn-in circuit is identical for all package types.



2224-29

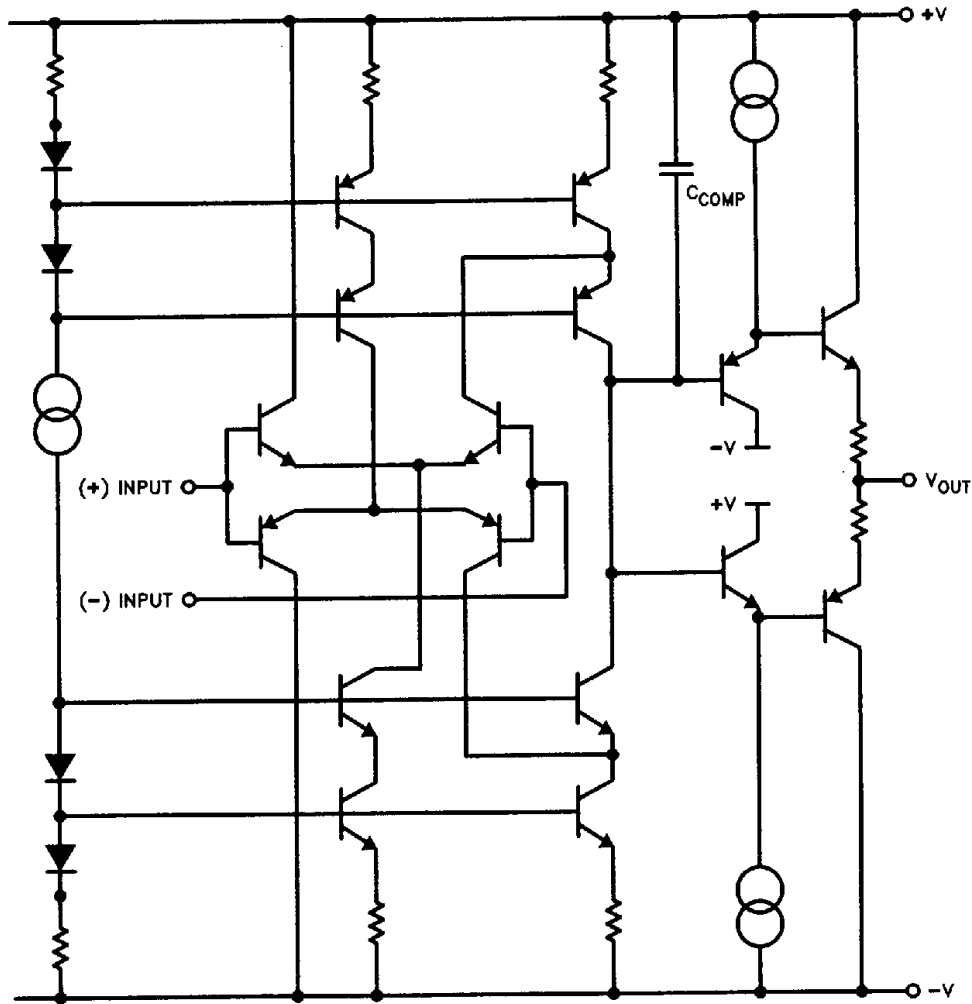
$A_V = +1$
 $C_L \leq 10 \text{ pF}$ Scope Probe

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Simplified Schematic (one amplifier)



2224-26

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EL2224 Macromodel

```

* Connections:      + input
*                  |
*                  | -input
*                  | + Vsupply
*                  | -Vsupply
*                  | output
*                  |
.subckt M2224      3   2   7   4   6

```

* Input stage

```

ie 37 4 4.5mA
r6 36 37 75
r7 38 37 75
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 2.6
rdiff 33 0 1Meg

```

* Compensation Section

```

ga 0 34 33 0 3m
rh 34 0 1Meg
ch 34 0 15pF
rc 34 40 300
cc 40 0 1pF

```

* Poles

```

ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 3pF
rpb 42 43 50
cpb 43 0 3pF

```

* Output Stage

```

ios1 7 50 0.5mA
ios2 51 4 0.5mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25

```

* models

```

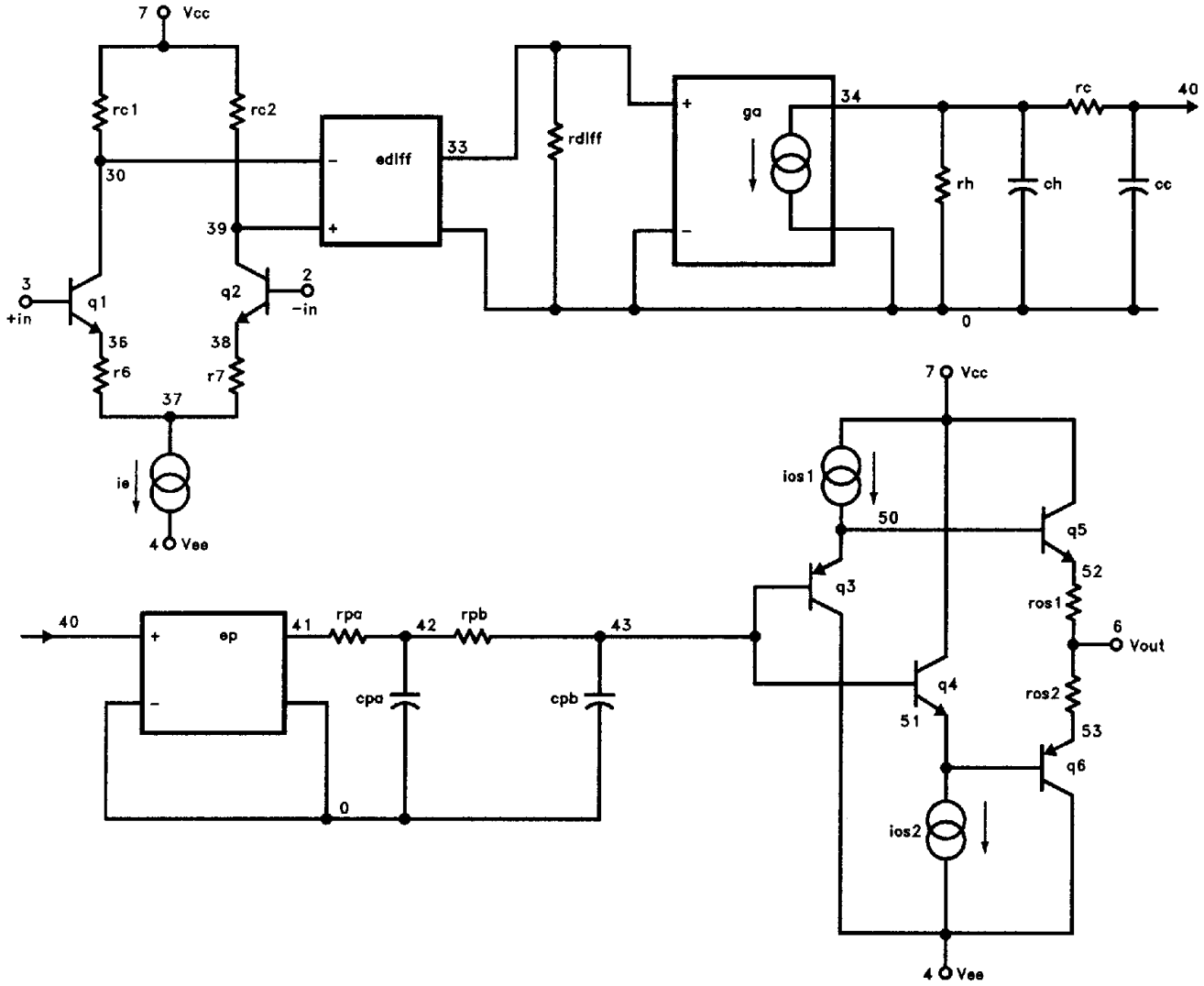
.model qn npn(is = 800.0E-18 bf = 350 tf = 0.2nS)
.model qna npn(is = 864E-18 bf = 400 tf = 0.2nS)
.model qp pnp(is = 800E-18 bf = 60 tf = 0.2nS)
.ends

```

1

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EL2224 Macromodel — Contd.

2224-30