National Semiconductor

February 1995

LM612
Dual-Channel Comparator and Reference

General Description

The dual-channel comparator consists of two individual comparators, having an input voltage range that extends down to the negative supply voltage V^-. The common open-collector output can be driven low by either half of the LM612. This configuration makes the LM612 ideal for use as a window comparator. The input stages of the comparator have lateral PNP input transistors which maintain low input currents for large differential input voltages and swings above V^+.

The 1.2V voltage reference, referred to the V^- terminal, is a two-terminal shunt-type band-gap similar to the LM185-1.2 series, with voltage accuracy of ±0.6% available. The reference features operation over a shunt current range of 17 μA to 20 mA, low dynamic impedance, and broad capacitive load range.

As a member of National's Super-Block™ family, the LM612 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

- Low operating current — 300 μA
- Wide supply voltage range — 4V to 36V
- Open-collector outputs
- Input common-mode range — V^- to (V^+ − 1.8V)
- Wide differential input voltage — ±36V

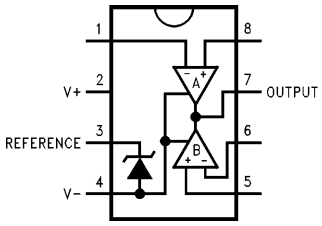
REFERENCE

- Fixed output voltage — 1.24V
- Tight initial tolerance available — ±0.6% (25°C)
- Wide operating current range — 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Voltage window comparator
- Power supply voltage monitor
- Dual-channel fault monitor

Connection Diagram



TL/H/11058–1

Top View

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corporation headquarters.

Reference Tolerances	Temperature Range		Package	NSC Package Number
	Military $-55°C \le T_J \le +125°C$	Industrial $-40°C \le T_J + 85°C$		
±0.6% at 25°C, 80 ppm/°C Max	LM612AMN	LM612AIN	8-Pin Molded DIP	N08E
	LM612AMJ/883 (Note 13)		8-Pin Ceramic DIP	J08A
±2.0% at 25°C, 150 ppm/°C Max	LM612MN	LM612IN	8-Pin Molded DIP	N08E
		LM612IM	8-Pin Narrow Surface Mount	M08A

Super-Block™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)
(Note 2) 36V (Max)
(Note 3) −0.3V (Min)

Current through Any Input Pin and V_R Pin ±20 mA

Differential Input Voltage ±36V

Output Short-Circuit Duration (Note 4)

Storage Temperature Range $-65°C \le T_J \le +150°C$

Maximum Junction Temperature 150°C

Thermal Resistance, Junction-to-Ambient (Note 5)
N Package 100°C/W

Soldering Information
N Package
Soldering (10 seconds) 260°C

ESD Tolerance (Note 6) ±1 kV

Operating Temperature Range

LM612AI, LM612I $-40°C \le T_J \le +85°C$
LM612AM, LM612M $-55°C \le T_J \le +125°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
COMPARATORS						
I_S	Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $3V \le V^+ \le 36V$	150 **170**	250 **300**	250 **300**	µA Max µA Max
V_{OS}	Offset Voltage over V^+ Range	$4V \le V^+ \le 36V$, $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV Max mV Max
V_{OS}	Offset Voltage over V_{CM} Range	$0V \le V_{CM} \le (V^+ - 1.8V)$ $V^+ = 30V$, $R_L = 15\ k\Omega$	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV Max mV Max
$\frac{\Delta V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			µV/°C
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA Max nA Max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA Max nA Max
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V, $2V \le V_{OUT} \le 27V$	500 **100**	50	50	V/mV Min V/mV
t_R	Large Signal Response Time	$V_{+IN} = 1.4V$, V_{-IN} = TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			µs µs
I_{SINK}	Output Sink Current	$V_{+IN} = 0V$, $V_{-IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA Min mA Min
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA Min mA Min
I_L	Output Leakage Current	$V_{+IN} = 1V$, $V_{-IN} = 0V$, $V_{OUT} = 36V$	0.1 **0.2**	10	10	µA Max µA

Electrical Characteristics These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
VOLTAGE REFERENCE (Note 9)						
V_R	Reference Voltage		1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V Min V Max
$\frac{\Delta V_R}{\Delta T}$	Average Drift with Temperature	(Note 10)	**18**	**80**	**150**	ppm/°C Max
$\frac{\Delta V_R}{kH}$	Average Drift with Time	$T_J = 40°C$ $T_J = 150°C$	400 1000			ppm/kH ppm/kH
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[17\ \mu A]}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV Max mV Max
		$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV Max mV Max
R	Resistance	$\Delta V_{R[10\ mA\ to\ 0.1\ mA]}/9.9\ mA$ $\Delta V_{R[100\ \mu A\ to\ 17\ \mu A]}/83\ \mu A$	0.2 0.6	**0.56** **13**	**0.56** **13**	Ω Max Ω Max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R[V+ = 5V]} - V_{R[V+ = 36V]}$	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV Max mV Max
		$V_{R[V+ = 5V]} - V_{R[V+ = 3V]}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV Max mV Max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is not allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting the Output to V^- will not cause power dissipation, so it may be continuous. However, shorting the Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If this total power causes the junction temperature to exceed 150°C, degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for $T_J = 25°C$ (standard type face) or over the full operating temperature range **(bold type face)**.

Note 9: V_R is the reference output voltage, nominally 1.24V.

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/V_{R[25°C]} \bullet \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

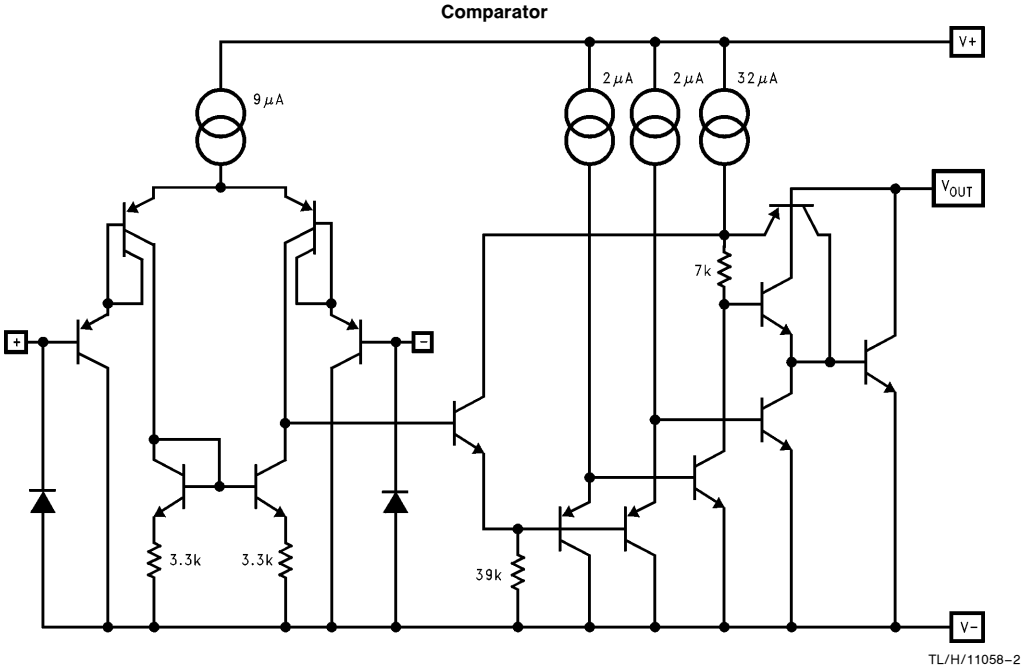
Note 11: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiralling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETS 612AMX electrical test specification is available on request. The military screened parts can also be procured as a Standard Military Drawing.

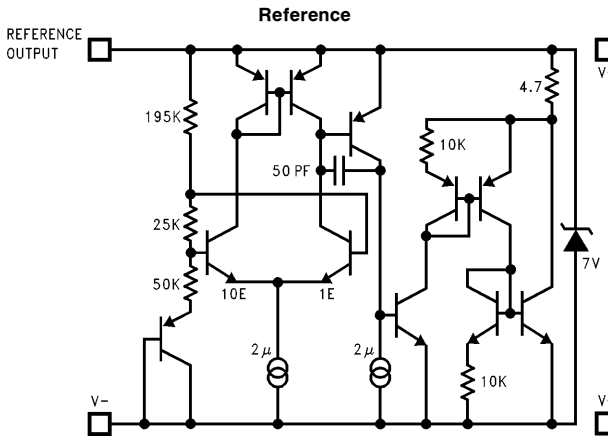
Simplified Schematic Diagrams

Comparator

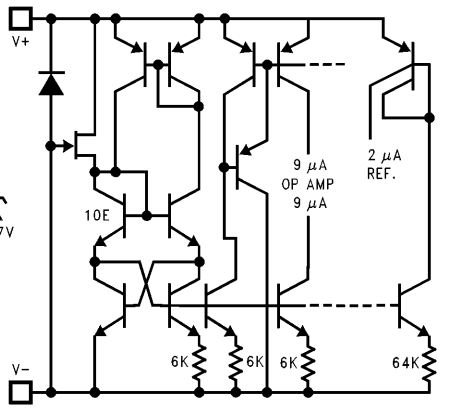


TL/H/11058–2

Reference



Bias

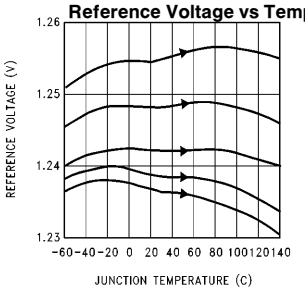


TL/H/11058–3

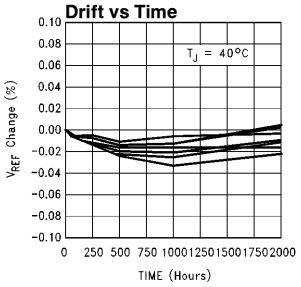
Typical Performance Characteristics (Reference)

T_J = 25°C, V^- = 0V, unless otherwise noted

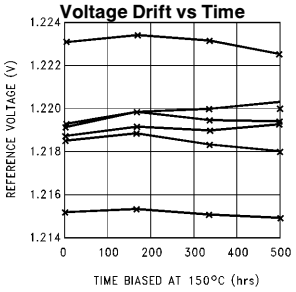
Reference Voltage vs Temp.



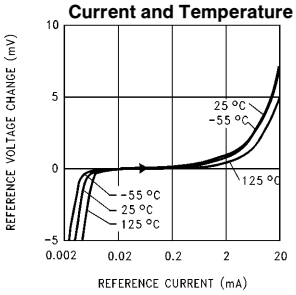
Reference Voltage Drift vs Time



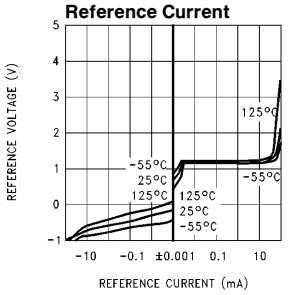
Accelerated Reference Voltage Drift vs Time



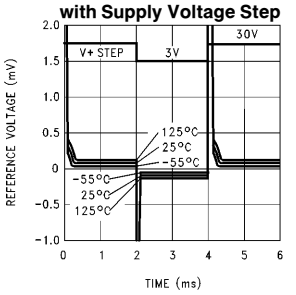
Reference Voltage vs Current and Temperature



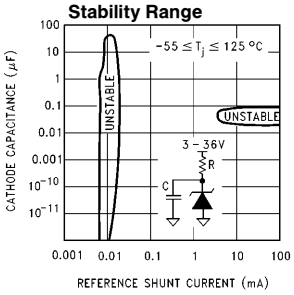
Reference Voltage vs Reference Current



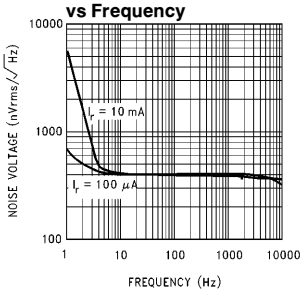
Reference Voltage Change with Supply Voltage Step



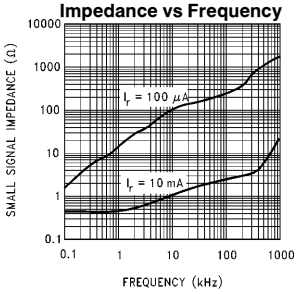
Reference AC Stability Range



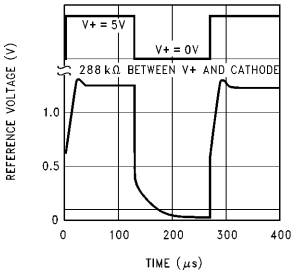
Reference Noise Voltage vs Frequency



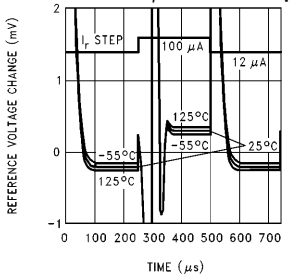
Reference Small-Signal Impedance vs Frequency



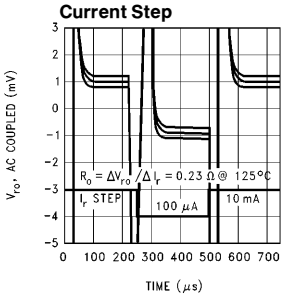
Reference Power-Up Time



Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step

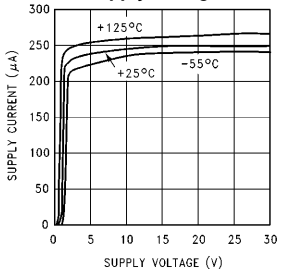


TL/H/11058–4

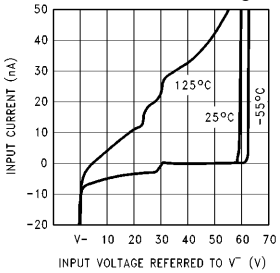
Typical Performance Characteristics (Comparators)

$T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$

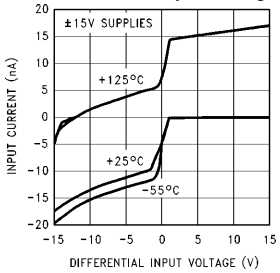
Supply Current vs Supply Voltage



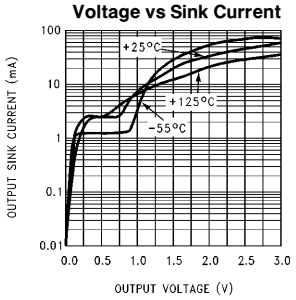
Input Bias Current vs Common-Mode Voltage



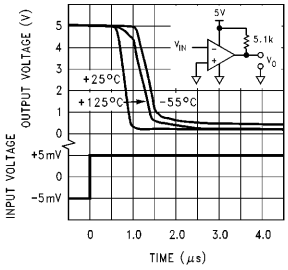
Input Current vs Differential Input Voltage



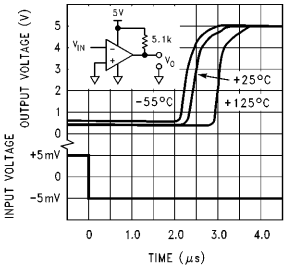
Output Saturation Voltage vs Sink Current



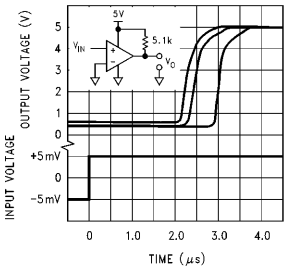
Small-Signal Response Times—Inverting Input, Negative Transition



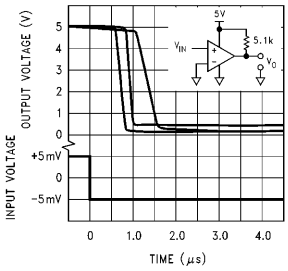
Small-Signal Response Times—Inverting Input, Positive Transition



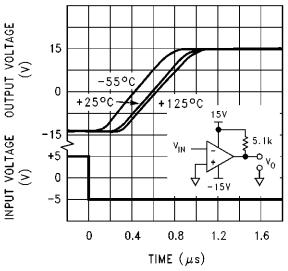
Small-Signal Response Times—Non-Inverting Input, Positive Transition



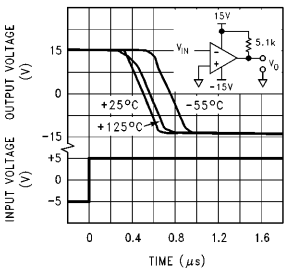
Small-Signal Response Times—Non-Inverting Input, Negative Transition



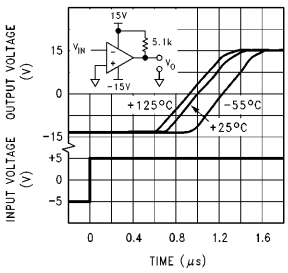
Large-Signal Response Times—Inverting Input, Positive Transition



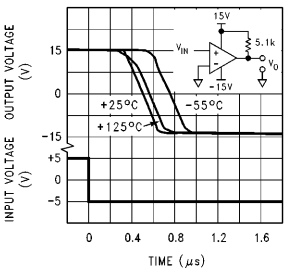
Large-Signal Response Times—Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



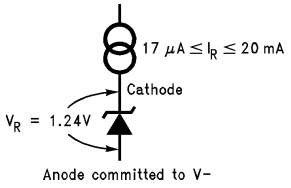
TL/H/11058–6

Application Information

VOLTAGE REFERENCE

Reference Biasing

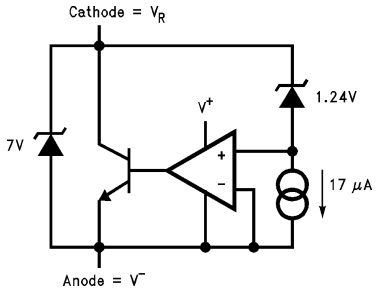
The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_R flowing in the ''forward'' direction there is the familiar diode transfer function. I_R flowing in the reverse direction forces the reference voltage to be developed from cathode to anode.



TL/H/11058–8

FIGURE 1. 1.24V Reference is Developed between Cathode and Anode; Current Source I_R is External

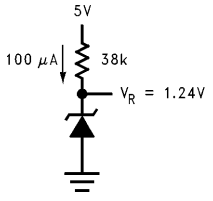
The reference equivalent circuit reveals how V_R is held at the constant 1.2V by feedback for a wide range of reverse current.



TL/H/11058–9

FIGURE 2. Reference Equivalent Circuit

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage to the Reference Output pin. Varying that voltage, and so varying I_R, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_R.



TL/H/11058–10

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA the reference is stable for any value of capacitance. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering when necessary.

Reference Hysteresis

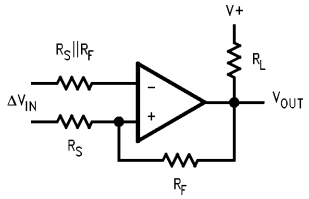
The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the datasheet for any given device. Do not assume that no specification means no hysteresis.

COMPARATORS

Either comparator or the reference may be biased in any way with no effect on the other sections of the LM612, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparator will still operate correctly. The inverting input of an unused comparator should be tied to V^- and the non-inverting tied to V^+.

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in *Figure 4*.



TL/H/11058–11

FIGURE 4. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in *Figure 4* is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \qquad \text{for } R_F >> R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV

Application Information (Continued)

of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

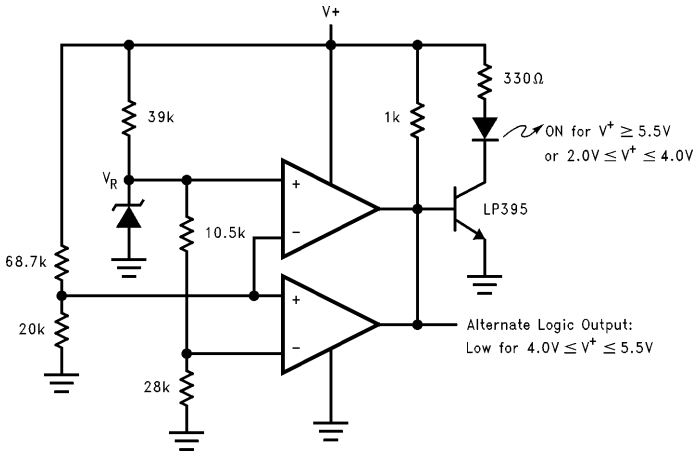
The guaranteed common-mode input voltage range for an LM612 is $V^- \leq V_{CM} \leq (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than ($V^- + 32V$), even if this is greater than V^+, the output will be at the correct state. If, however, either or both inputs are driven below V^-, and either input current exceeds 10 μA, the output state is not guaranteed to be correct. If both inputs are above ($V^+ - 1.8V$), the output state is also not guaranteed to be correct.

Output Stage

The comparators have a common open-collector output stage which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

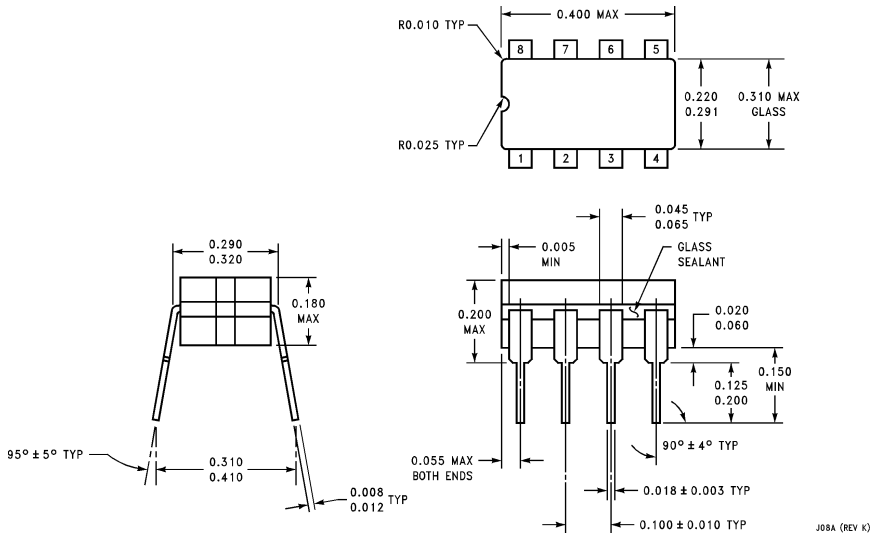
Typical Applications



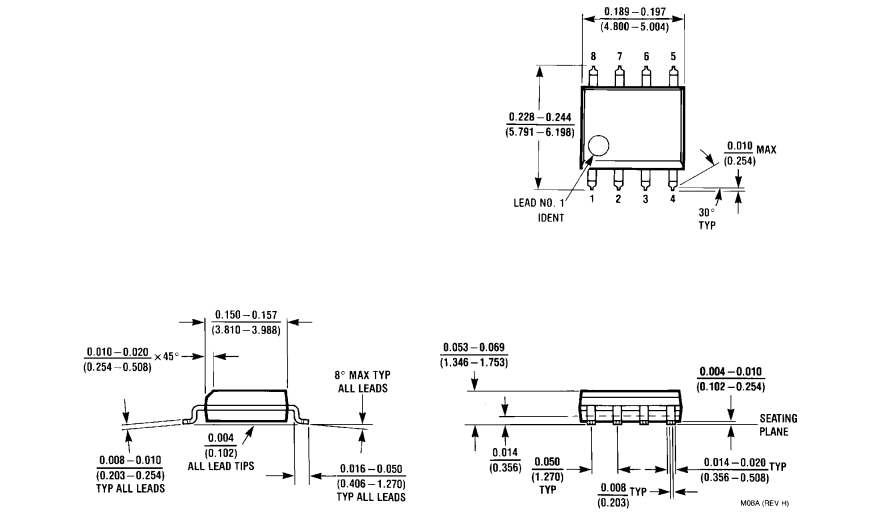
TL/H/11058–12

Power Supply Monitor with Indicator

Physical Dimensions inches (millimeters)

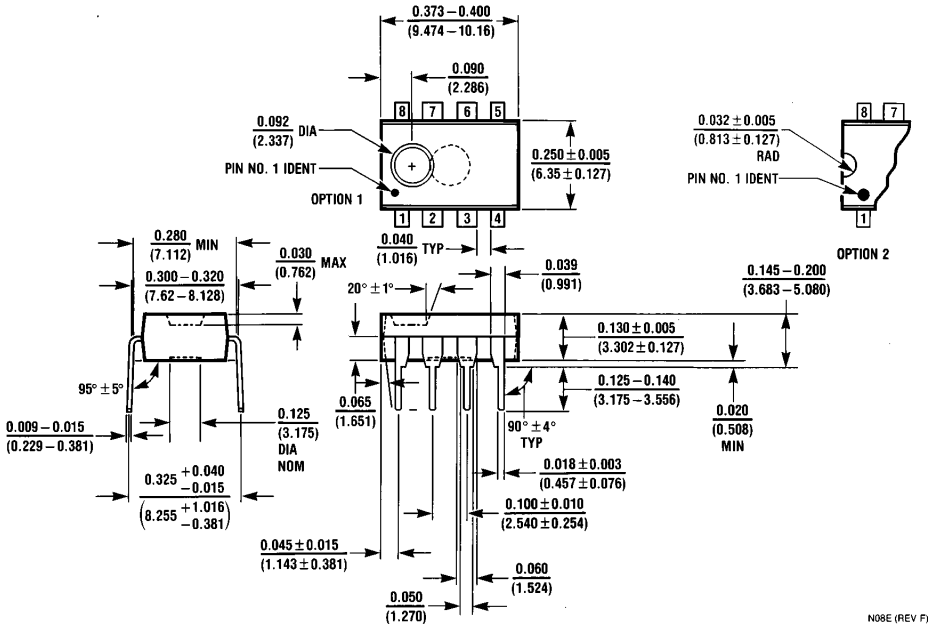


8-Pin Ceramic Dual-In-Line Package (J)
Order Number LM612AMJ/883
NS Package Number J08A



8-Pin Surface Mount Package (M)
Order Number LM612IM
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



8-Pin Molded Dual-In-Line Package (N)
Order Number LM612AMJ/883, LM612AMN, LM612AIN, LM612MN or LM612IN
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408