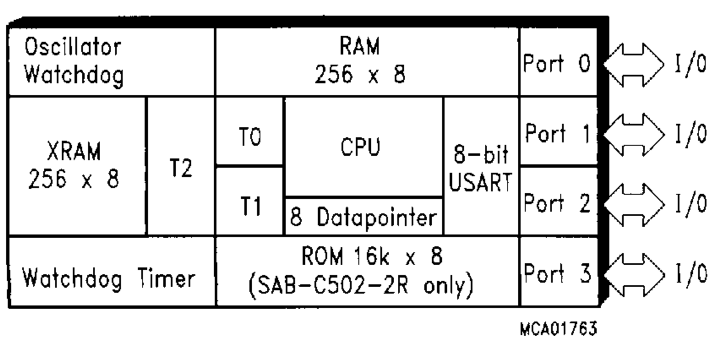
SIEMENS

8-Bit CMOS Microcontroller SAB-C502

Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12 / 20 MHz operating frequency
- 16 K × 8 ROM (SAB-C502-2R only)
- 256 × 8 RAM
- 256 × 8 XRAM (additional on-chip RAM)
- Eight datapointers for indirect addressing of program and external data memory (including XRAM)
- Four 8-bit ports
- Three 16 -bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART with programmable 10-bit Baudrate-Generator
- Six interrupt sources, two priority levels
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- P-DIP-40 package and P-LCC-44 package
- Temperature ranges: SAB-C502 T_A: 0 °C to 70 °C
  SAF-C502 T_A: – 40 °C to 85 °C

SAB-C502



The SAB-C502-L/C502-2R described in this document is compatible with the SAB 80C52 and can be used for all present SAB 80C52 applications.

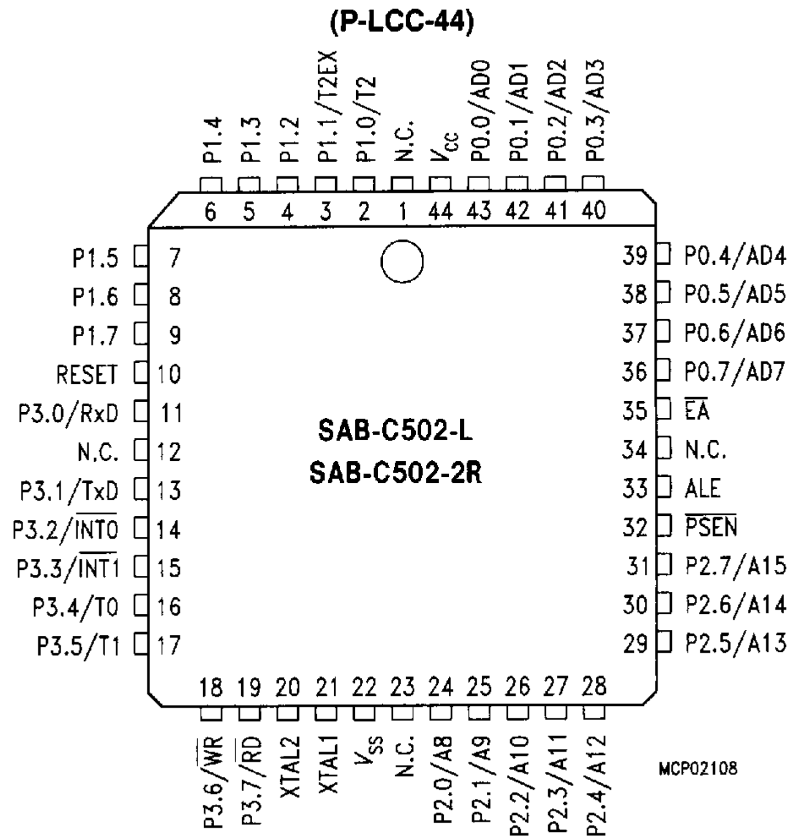
The SAB-C502-2R contains a non-volatile 16 K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers/counters, a six source, two priority level interrupt structure, a serial port and versatile fail save mechanisms. The SAB-C502-L/C502-2R incorporates 256 × 8 additional on-chip RAM called XRAM. For higher performance eight datapointers are implemented. The SAB-C502-L is identical, except that it lacks the program memory on chip. Therefore the term SAB-C502 refers to both versions within this specification unless otherwise noted.

Ordering Information

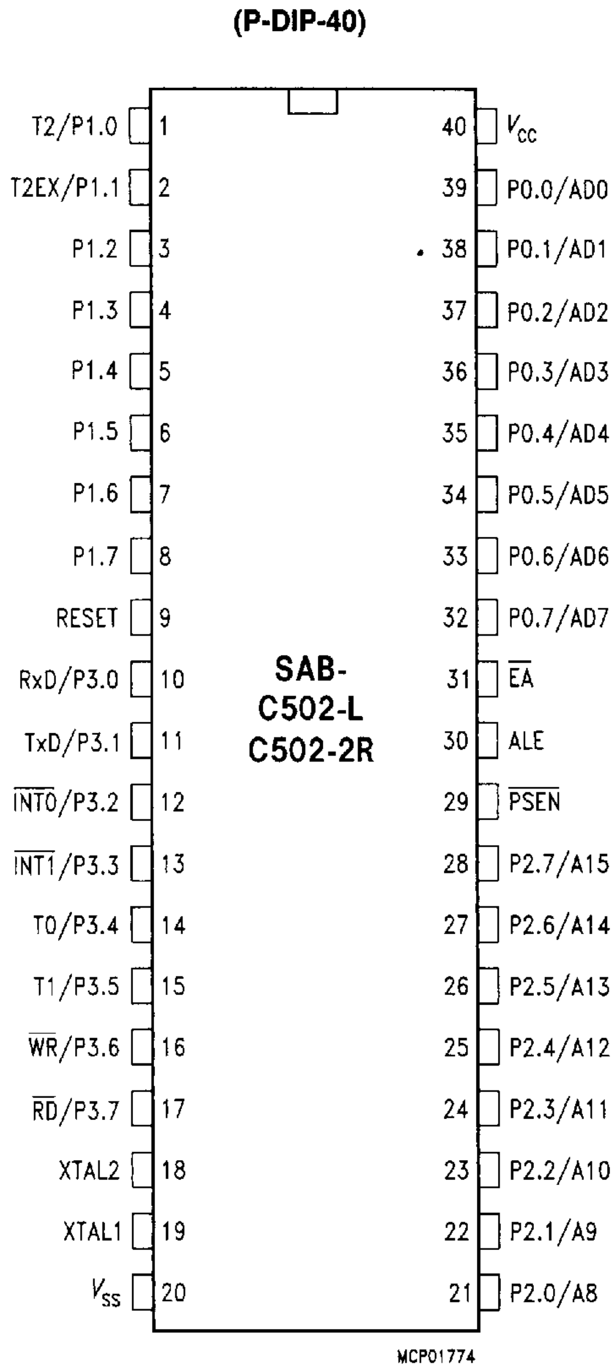
Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C502-LN SAB-C502-LP	Q67120-C838 Q67120-C889	P-LCC-44 P-DIP-40	for external memory 12 MHz
SAB-C502-2RN SAB-C502-2RP	Q67120-C839 Q67120-C890	P-LCC-44 P-DIP-40	with mask-programmable ROM, 12 MHz
SAB-C502-L20N SAB-C502-L20P	Q67120-C885 Q67120-C891	P-LCC-44 P-DIP-40	for external memory 20 MHz
SAB-C502-2R20N SAB-C502-2R20P	Q67120-C884 Q67120-C892	P-LCC-44 P-DIP-40	with mask-programmable ROM, 20 MHz
SAF-C502-LN SAF-C502-LP	Q67120-C883 Q67120-C893	P-LCC-44 P-DIP-40	for external ROM, 12 MHz, ext. temp. – 40 ˚C to 85 ˚C
SAF-C502-2RN SAF-C502-2RP	Q67120-C886 Q67120-C894	P-LCC-44 P-DIP-40	with mask-programmable ROM, 12 MHz, ext. temp. – 40 ˚C to 85 ˚C
SAF-C502-L20N SAF-C502-L20P	Q67120-C887 Q67120-C895	P-LCC-44 P-DIP-40	for external memory, 20 MHz, ext. temp. – 40 ˚C to 85 ˚C
SAF-C502-2R20N SAF-C502-2R20P	Q67120-C888 Q67120-C896	P-LCC-44 P-DIP-40	with mask-programmable ROM, 20 MHz, ext. temp. – 40 ˚C to 85 ˚C

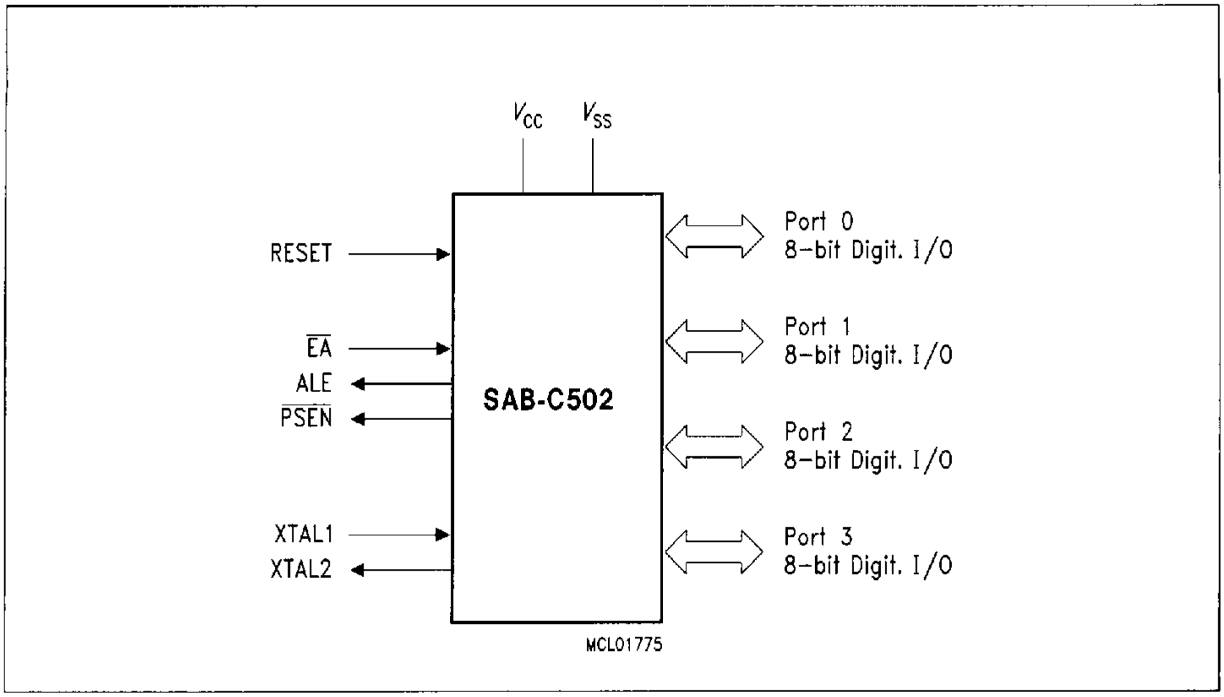
Note: Extended temperature range – 40 ˚C to 110 ˚C (SAH-C502) on request.

Pin Configuration
(top view)



Pin Configuration
(top view)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
P1.7 – P1.0	9–2	8–1	I	**Port 1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows:
	2	1		P1.0 T2 Input to counter 2
	3	2		P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count

*) I = Input
O = Output

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Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
P3.0 – P3.7	11, 13–19	10–17	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	11	10		P3.0 RxD receiver data input (asynchronous) or data input/ output (synchronous) of serial interface 0
	13	11		P3.1 TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12		P3.2 $\overline{\text{INT0}}$ interrupt 0 input/timer 0 gate control
	15	13		P3.3 $\overline{\text{INT1}}$ interrupt 1 input/timer 1 gate control
	16	14		P3.4 T0 counter 0 input
	17	15		P3.5 T1 counter 1 input
	18	16		P3.6 $\overline{\text{WR}}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17		P3.7 $\overline{\text{RD}}$ the read control signal enables the external data memory to port 0
XTAL2	20	18	–	XTAL2 Output of the inverting oscillator amplifier

*)I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
XTAL1	21	19	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	I/O	**Port 2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	29	O	The **$\overline{\text{Program Store Enable}}$** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-LCC-44	P-DIP-40		
RESET	10	9	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
ALE	33	30	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	35	31	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (SAB-C502-2R only) when the PC is less than 4000_H. When held at low level, the SAB-C502 fetches all instructions from external program memory. For the SAB-C502-L this pin must be tied low.
P0.0 – P0.7	43–36	39–32	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB-C502-2R. External pull-up resistors are required during program verification.
V_{SS}	22	20	–	**Circuit ground potential**
V_{CC}	44	40	–	**Supply terminal** for all operating modes
N.C.	1, 12, 23, 34	–	–	**No connection**

*) I = Input
O = Output

Functional Description

The SAB-C502 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the SAB 80C52. While maintaining all architectural and operational characteristics of the SAB 80C52 the SAB-C502 incorporates some enhancements in the Timer2 and Fail Save Mechanism Unit.

Figure 1 shows a block diagram of the SAB-C502.

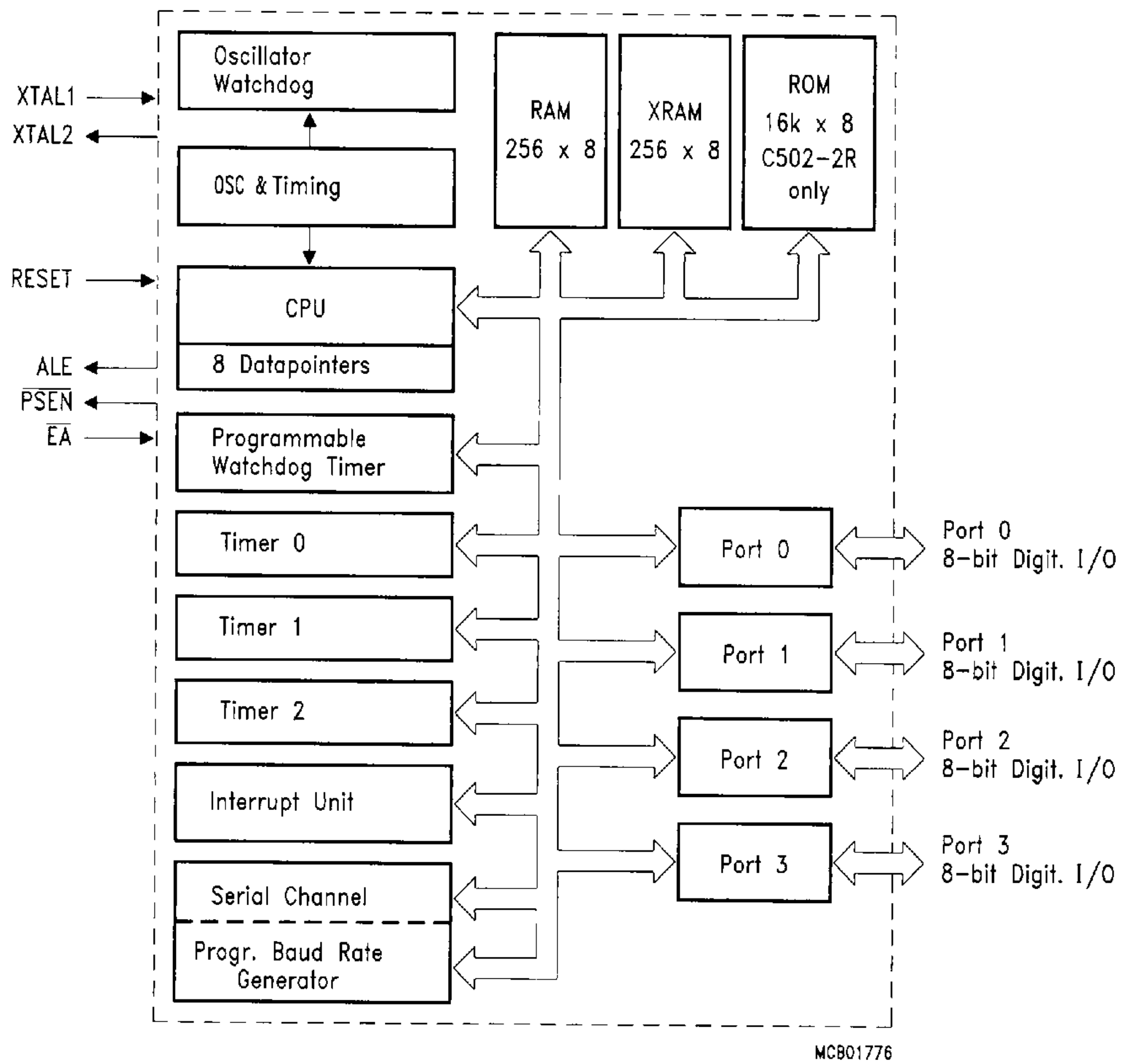

Figure 1
Block Diagram of the SAB-C502

CPU

The SAB-C502 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions execute in 1.0 µs (18 MHz : 667 ns).

Special Function Register PSW

	MSB							LSB	
Bit No	7	6	5	4	3	2	1	0	
Addr. $D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		**Carry Flag**
AC		**Auxiliary Carry Flag** (for BCD operations)
F0		**General Purpose Flag**
RS1	**RS0**	**Register Bank select control bits**
0	0	Bank 0 selected, data address 00_H - 07_H
0	1	Bank 1 selected, data address 08_H - $0F_H$
1	0	Bank 2 selected, data address 10_H - 17_H
1	1	Bank 3 selected, data address 18_H - $1F_H$
OV		**Overflow Flag**
F1		**General Purpose Flag**
P		**Parity Flag.** Set/cleared by hardware each instruction cycle to indicate an odd/even number of “one” bits in the accumulator, i.e. even parity.

Reset value of PSW is 00H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 36 special function register (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2** and **table 3**. In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the SAB-C502. **Table 3** illustrates the contents of the SFRs.

Table 1
Special Function Register in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** 1)	**FF_H**	**98_H**	**SCON** 1)	**00_H**
81_H	SP	07_H	99_H	SBUF	XX_H 2)
82_H	DPL	00_H	$9A_H$	reserved	XX_H 2)
83_H	DPH	00_H	$9B_H$	reserved	XX_H 2)
84_H	reserved		$9C_H$	reserved	XX_H 2)
85_H	reserved		$9D_H$	reserved	XX_H 2)
86_H	WDTREL	00_H	$9E_H$	reserved	XX_H 2)
87_H	PCON	$000X0000_B$ 2)	$9F_H$	reserved	XX_H 2)
88_H	**TCON** 1)	**00_H**	**$A0_H$**	**P2** 1)	**FF_H**
89_H	TMOD	00_H	$A1_H$	reserved	XX_H 2)
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H 2)
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H 2)
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H 2)
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H 2)
$8E_H$	reserved	XX_H 2)	$A6_H$	reserved	XX_H 2)
$8F_H$	reserved	XX_H 2)	$A7_H$	reserved	XX_H 2)
90_H	**P1** 1)	**FF_H**	**$A8_H$**	**IE** 1)	**$0X000000_B$** 2)
91_H	XPAGE	00_H	$A9_H$	reserved	XX_H 2)
92_H	DPSEL	$XXXXX000_B$ 2)	AA_H	SRELL	$0D9_H$
93_H	reserved	XX_H 2)	AB_H	reserved	XX_H 2)
94_H	XCON	$0F8_H$	AC_H	reserved	XX_H 2)
95_H	reserved	XX_H 2)	AD_H	reserved	XX_H 2)
96_H	reserved	XX_H 2)	AE_H	reserved	XX_H 2)
97_H	reserved	XX_H 2)	AF_H	reserved	XX_H 2)

1): Bit-addressable Special Function Register
2): X means that the value is indeterminate and the location is reserved

Table 1
Special Function Register in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3**[1]	**FF_H**	**$D8_H$**	**BAUD**	**$0XXXXXXX_B$**[2]
$B1_H$	SYSCON	$XXXXXX01_B$[2]	$D9_H$	reserved	XX_H[2]
$B2_H$	reserved	XX_H[2]	DA_H	reserved	XX_H[2]
$B3_H$	reserved	XX_H[2]	DB_H	reserved	XX_H[2]
$B4_H$	reserved	XX_H[2]	DC_H	reserved	XX_H[2]
$B5_H$	reserved	XX_H[2]	DD_H	reserved	XX_H[2]
$N6_H$	reserved	XX_H[2]	DE_H	reserved	XX_H[2]
$B7_H$	reserved	XX_H[2]	DF_H	reserved	XX_H[2]
$B8_H$	**IP**[1]	**$XX000000_B$**[2]	**$E0_H$**	**ACC**[1]	**00_H**
$B9_H$	reserved	XX_H[2]	$E1_H$	reserved	XX_H[2]
BA_H	SRELH	$XXXXXX11_B$[2]	$E2_H$	reserved	XX_H[2]
BB_H	reserved	XX_H[2]	$E3_H$	reserved	XX_H[2]
BC_H	reserved	XX_H[2]	$E4_H$	reserved	XX_H[2]
BD_H	reserved	XX_H[2]	$E5_H$	reserved	XX_H[2]
BE_H	reserved	XX_H[2]	$E6_H$	reserved	XX_H[2]
BF_H	reserved	XX_H[2]	$E7_H$	reserved	XX_H[2]
$C0_H$	**WDCON**[1]	**$XXXX0000_B$**[2]	**$E8_H$**	reserved	XX_H[2]
$C1_H$	reserved	XX_H[2]	$E9_H$	reserved	XX_H[2]
$C2_H$	reserved	XX_H[2]	EA_H	reserved	XX_H[2]
$C3_H$	reserved	XX_H[2]	EB_H	reserved	XX_H[2]
$C4_H$	reserved	XX_H[2]	EC_H	reserved	XX_H[2]
$C5_H$	reserved	XX_H[2]	ED_H	reserved	XX_H[2]
$C6_H$	reserved	XX_H[2]	EE_H	reserved	XX_H[2]
$C7_H$	reserved	XX_H[2]	EF_H	reserved	XX_H[2]
$C8_H$	**T2CON**[1]	**00_H**	**$F0_H$**	**B**[1]	**00_H**
$C9_H$	T2MOD	$XXXXXXX0_B$[2]	$F1_H$	reserved	XX_H[2]
CA_H	RC2L	00_H	$F2_H$	reserved	XX_H[2]
CB_H	RC2H	00_H	$F3_H$	reserved	XX_H[2]
CC_H	TL2	00_H	$F4_H$	reserved	XX_H[2]
CD_H	TH2	00_H	$F5_H$	reserved	XX_H[2]
CE_H	reserved	XX_H[2]	$F6_H$	reserved	XX_H[2]
CF_H	reserved	XX_H[2]	$F7_H$	reserved	XX_H[2]
$D0_H$	**PSW**[1]	**00_H**	**$F8_H$**	reserved	**XX_H**[2]
$D1_H$	reserved	XX_H[2]	$F9_H$	reserved	XX_H[2]
$D2_H$	reserved	XX_H[2]	FA_H	reserved	XX_H[2]
$D3_H$	reserved	XX_H[2]	FB_H	reserved	XX_H[2]
$D4_H$	reserved	XX_H[2]	FC_H	reserved	XX_H[2]
$D5_H$	reserved	XX_H[2]	FD_H	reserved	XX_H[2]
$D6_H$	reserved	XX_H[2]	FE_H	reserved	XX_H[2]
$D7_H$	reserved	XX_H[2]	FF_H	reserved	XX_H[2]

[1]: Bit-addressable Special Function Register
[2]: X means that the value is indeterminate and the location is reserved

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Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$**[1)]	00_H
	B	B-Register	**$F0_H$**[1)]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data pointer select register	92_H	XXXX X000 B[3)]
	PSW	Program Status Word Register	**$D0_H$**[1)]	00_H
	SP	Stack Pointer	81_H	07_H
Interrupt System	IE	Interrupt Enable Register	**$A8_H$**[1)]	0X00 0000 B[3)]
	IP	Interrupt Priority Register	**$B8_H$**[1)]	XX00 0000 B[3)]
Ports	P0	Port 0	**80_H**[1)]	FF_H
	P1	Port 1	**90_H**[1)]	FF_H
	P2	Port 2	**$A0_H$**[1)]	FF_H
	P3	Port 3	**$B0_H$**[1)]	FF_H
XRAM	XPAGE	Page addr. reg. for XRAM	91_H	00_H
	XCON	XRAM startaddress (highbyte)	94_H	$F8_H$
	SYSCON	XRAM control register	$B1_H$	XXXX XX01B[3)]
Serial Channels	PCON[2)]	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Reg.	99_H	XX_H[3)]
	SCON	Serial Channel Control Reg.	**98_H**[1)]	00_H
	SRELL	Baudrate Generator Reloadvalue, Lowbyte	AA_H	$D9_H$
	SRELH	Baudrate Generator Reloadvalue, Highbyte	BA_H	XXXX XX11B[3)]
	BAUD	Baudrate Generator Enable Bit	**$D8_H$**[1)]	0XXX XXXXB[3)]
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H**[1)]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$**[1)]	00_H
	T2MOD	Timer 2 Mode Register	$C9_H$	XXXX XXX0 B[3)]
	RC2L	Timer 2, Reload Capture Register, Low Byte	CA_H	00_H
	RC2H	Timer 2, Reload Capture Register, High Byte	CB_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
Watchdog	WDCON	Watchdog Timer Control Register	**$C0_H$**[1)]	XXXX 0000B[3)]
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H
Pow. Sav. Modes	PCON[2)]	Power Control Register	87_H	000X 0000B[3)]

1): Bit-addressable special function registers
2): This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3): X means that the value is indeterminate and the location is reserved

Table 3
Contents of SFR's, SFR's in Numeric Order

Address	Register	Bit 7	6	5	4	3	2	1	0
80_H	P0								
81_H	SP								
82_H	DPL								
83_H	DPH								
86_H	WDTREL								
87_H	PCON	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88_H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0
$8A_H$	TL0								
$8B_H$	TL1								
$8C_H$	TH0								
$8D_H$	TH1								
90_H	P1								
91_H	XPAGE								
92_H	DPSEL	–	–	–	–	–	.2	.1	.0
94_H	XCON								
98_H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF								
$A0_H$	P2								
$A8_H$	IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
AA_H	SRELL								

(solid cell dividers) bit and byte addressable

(dashed cell dividers) not bit addressable

– = reserved

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Table 3
Contents of SFRs, SFRs in Numeric Order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
$B0_H$	P3								
$B1_H$	SYSCON	–	–	–	–	–	–	XMAP1	XMAP0
$B8_H$	IP	–	PADC	PT2	PS	PT1	PX1	PT0	PX0
BA_H	SRELH								
$C0_H$	WDCON	–	–	–	–	OWDS	WDTS	WDT	SWDT
$C8_H$	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	–	–	–	–	–	–	–	DCEN
CA_H	RC2L								
CB_H	RC2H								
CC_H	TL2								
CD_H	TH2								
$D0_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$	BAUD	BD	–	–	–	–	–	–	–
$E0_H$	ACC								
$F0_H$	B								

(solid cell dividers) bit and byte addressable

(broken cell dividers) not bit addressable

– = reserved

Timer/Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**:

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/12 \times 32$	$f_{OSC}/24 \times 32$
1	16-bit timer/counter	X	X	0	1	$f_{OSC}/12$	$f_{OSC}/24$
2	8-bit timer/counter with 8-bit auto-reload	X	X	1	0	$f_{OSC}/12$	$f_{OSC}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/24$

In “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

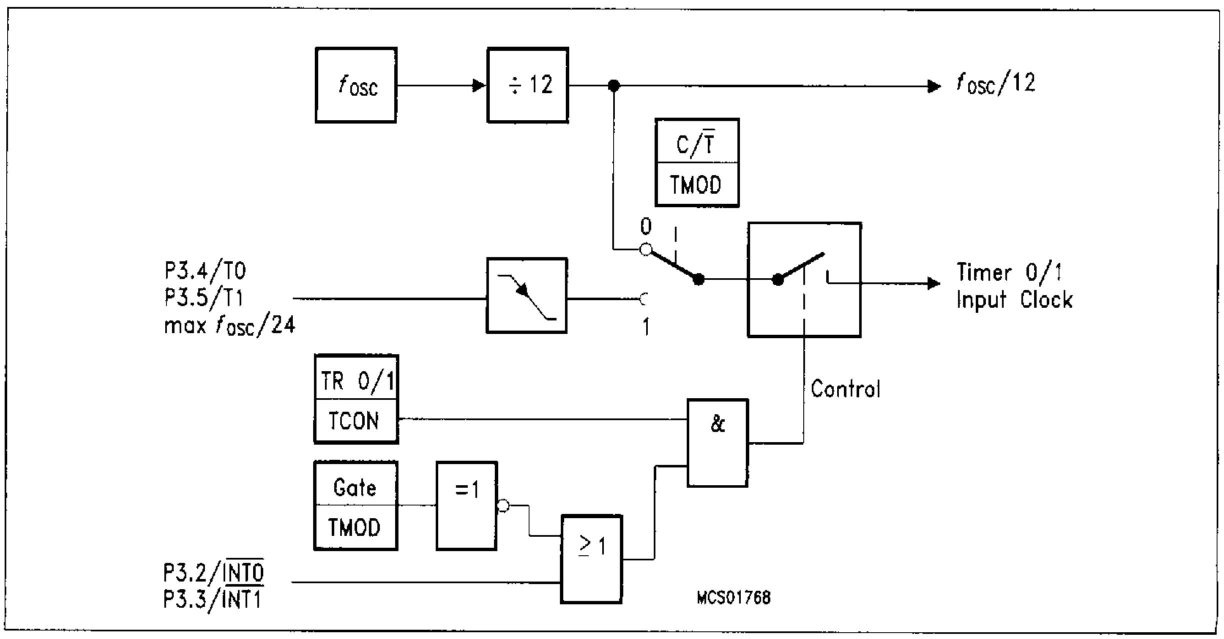

Figure 2
Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with up/down count feature. It can operate either as timer or as an event counter which is selected by bit $C/\overline{T2}$ (T2CON.1). It has three operating modes as shown in **table 5**.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	$CP/\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$f_{OSC}/12$	max $f_{OSC}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting)	$f_{OSC}/12$	max $f_{OSC}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2)	$f_{OSC}/2$	max $f_{OSC}/24$
	1	X	1	X	1	↓	extra external interrupt ("Timer 2")		
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

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Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. **Figure 3** illustrates the block diagram of Baudrate generation for the serial interface.

Table 6
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate or Baudrate Generator	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate or Baudrate Generator	9-bit UART Like mode 2 except the variable baud rate

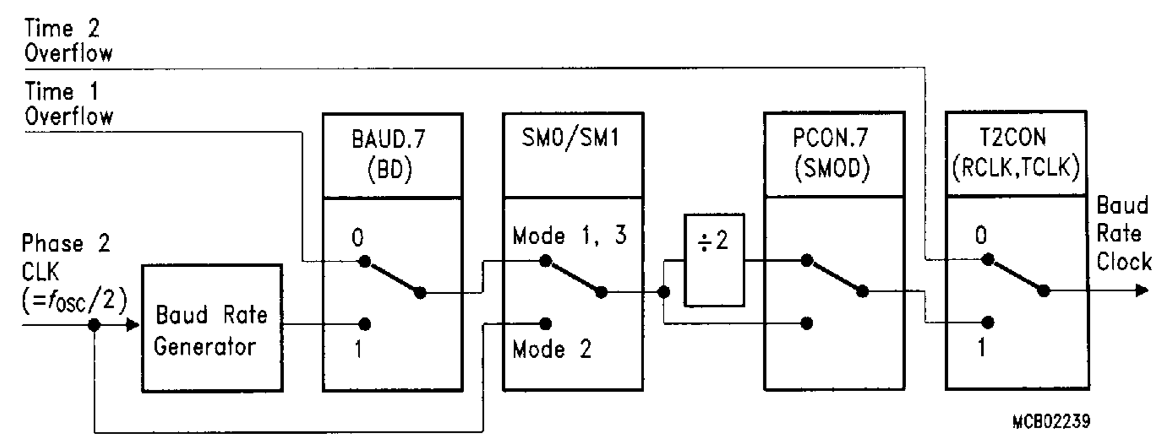

Figure 3
Block Diagram of Baud Rate Generation for Serial Interface

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The possible baudrate can be calculated using the formulas given in **table 7**.

Table 7
Baudrates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC})/64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times \text{timer 1 overflow rate})/32$ $(2^{SMOD} \times f_{OSC})/(32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	$f_{OSC}/(32 \times (65536\text{-(RC2H, RC2L)}))$
Baudrate Generator	1,3	$(2^{SMOD} \times f_{OSC})/(64 \times (2^{10}\text{-SREL}))$

The internal baudrate generator consists of a free running 10-bit timer with $f_{OSC}/2$ input frequency. The internal baudrate generator is selected by setting bit BD in SFR BAUD.

Additional On-Chip RAM - XRAM

The SAB-C502 contains another 256byte of On-Chip RAM additional to the 256bytes internal RAM. This RAM is called XRAM ('eXtended RAM') in this document.

The additional ON-Chip RAM is logically located in the external data memory range. The highbyte of the XRAM address range startaddress is programmable by SFR XCON (94_H). The reset value of XCON is $0F8_H$ (that is, XRAM address range $F800H_H$ … $F8FF_H$).

The contents of the XRAM is not affected by a reset. After power up the contents is undefined, while it remains unchanged during and after reset as long as the power supply is not turned off. The XRAM is controlled by SFR SYSCON as shown in **table 8**.

Table 8
Control of the XRAM

SFR SYSCON		Description
XMAP1	XMAP0	
0	1	Resetvalue. Access to XRAM is disabled. When cleared it can be set again only by a reset
0	0	XRAM enabled
1	0	XRAM enabled. The signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM

Because of the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM. A general overview gives **table 9**.

Table 9
Accessing the XRAM

Instruction using	Instruction	Remarks
DPTR	MOVX A @DPTR MOVX @ DPTR,A	Normally the use of these instructions would use a physically external memory. However, in the SAB-C502 the XRAM is accessed if it is enabled.
R0/R1 (page mode)	MOVX A, @Ri MOVX@Ri,A	Normally Port 2 serves as page register. However, the distinction, whether Port 2 is as general purpose I/O or as "page address" is made by the external design. Hence a special SFR XPAGE is implemented the serve the same function for the XRAM as Port 2 for external data memory.

Note: When writing the page address (in page mode) at Port2 the value is also written in XPAGE. However when writing XPAGE the value at PORT2 is not changed!

The behaviour of Port0/Port2 and $\overline{RD/WR}$ during MOVX accesses is shown in **table 10**.

Table 10
Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ during MOVX Accesses

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			XMAP1, XMAP0		
		00	10	X1	00	10	X1
MOVX @DPTR	DPTR outside XRAM address range (DPH ≠ XCON)	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	DPTR within XRAM address range (DPH = XCON)	a) P0/P2 → Bus ($\overline{WR}$-Data only) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2 → Bus ($\overline{WR}$-Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2 → Bus ($\overline{WR}$-Data only) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2 → Bus b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
MOVX @Ri	XPAGE outside XRAM addr. page range (XPAGE ≠ XCON)	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used
	XPAGE within XRAM addr. page range (XPAGE = XCON)	a) P0 → Bus ($\overline{WR}$-Data only) P2 → I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0 → Bus ($\overline{WR}$-Data only) P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used	a) P0/P2 → I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0 → Bus ($\overline{WR}$-Data only) P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0 → Bus P2 → I/O b) $\overline{RD}/\overline{WR}$ active c) ext. memory is used

modes compatible to the standard 8051-family

Eight Datapointers for Faster External Bus Access

The SAB-C502 contains a set of eight 16-bit-Datapointer (DPTR) from which the actual DPTR can be selected.

This means that the user's program may keep up to eight 16-bit addresses resident in these registers, but only one register at the time is selected to be the datapointer. Thus the DPTR in turn is accessed (or selected) via indirect addressing. This indirect addressing is done through a special function register (SFR) called DPSEL (data pointer select register, Bits 0 to 2). All instructions of the SAB-C502 which handle the DPTR therefore affect only one of the eight pointers which is addressed by DPSEL at that very moment.

A 3-bit field in SFR DPSEL points to the currently used DPTRx:

DPSEL			selected DPTR
.2	.1	.0	
0	0	0	DPTR 0
0	0	1	DPTR 1
0	1	0	DPTR 2
0	1	1	DPTR 3
1	0	0	DPTR 4
1	0	1	DPTR 5
1	1	0	DPTR 6
1	1	1	DPTR 7

Interrupt System

The SAB-C502 provides 6 interrupt sources with two priority levels. **Figure 4** gives a general overview of the interrupt sources and illustrates the request and control flags.

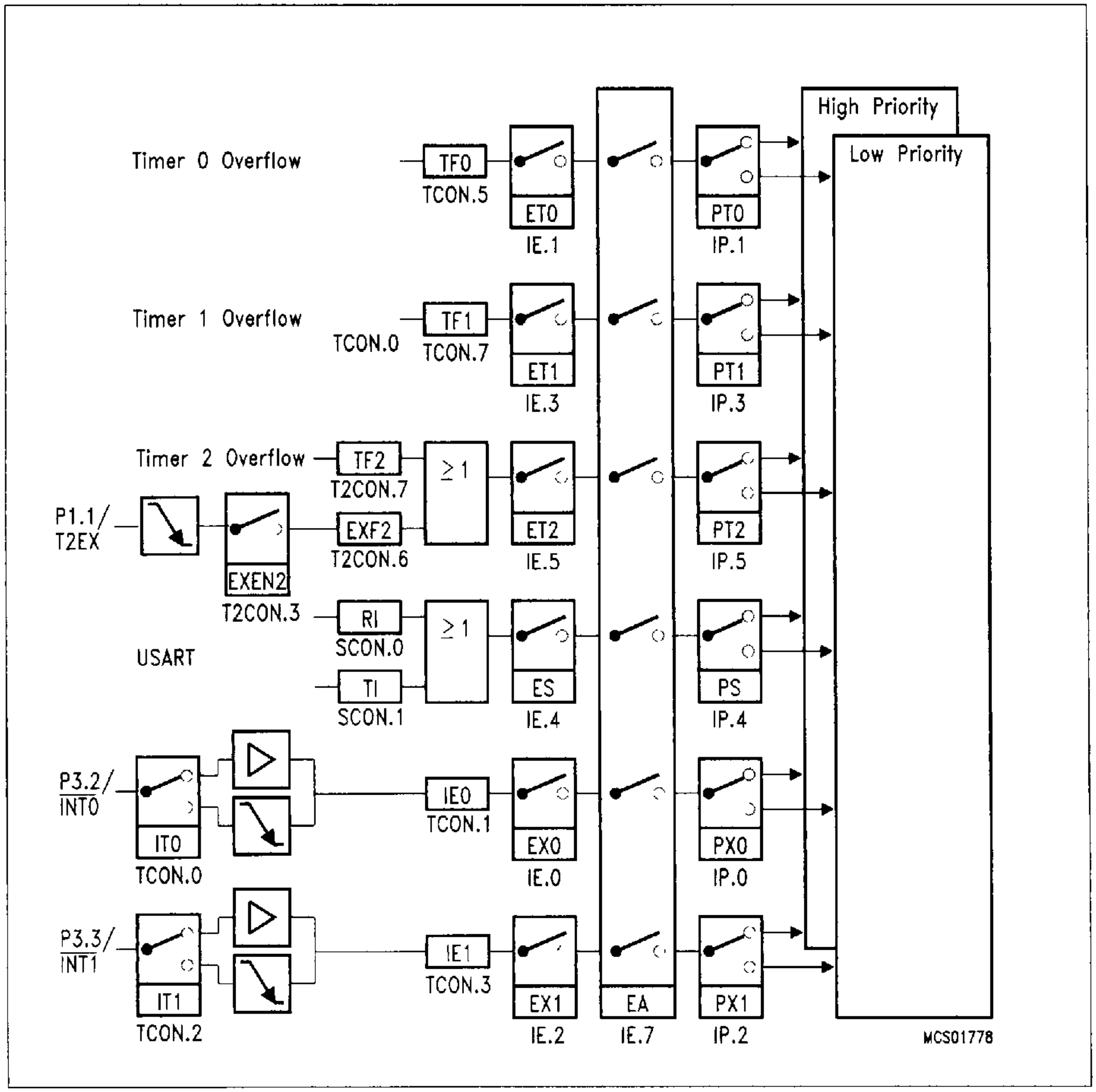

Figure 4
Interrupt Request Sources

Table 11
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	$002B_H$

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 12**.

Table 12
Interrupt Priority-within-Level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Serial Channel,	RI or TI	
Timer 2 Interrupt,	TF2 or EXF2	Low

Fail Safe Mechanisms

The SAB-C502 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure.

1) Watchdog Timer (15 bit, WDT)

2) Oscillator Watchdog (OWD)

1) Watchdog Timer (WDT)

The Watchdog Timer in the SAB-C502 is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler. The latter is enabled by setting bit WDTREL.7.

Figure 5 shows the block diagram of the programmable Watchdog Timer.

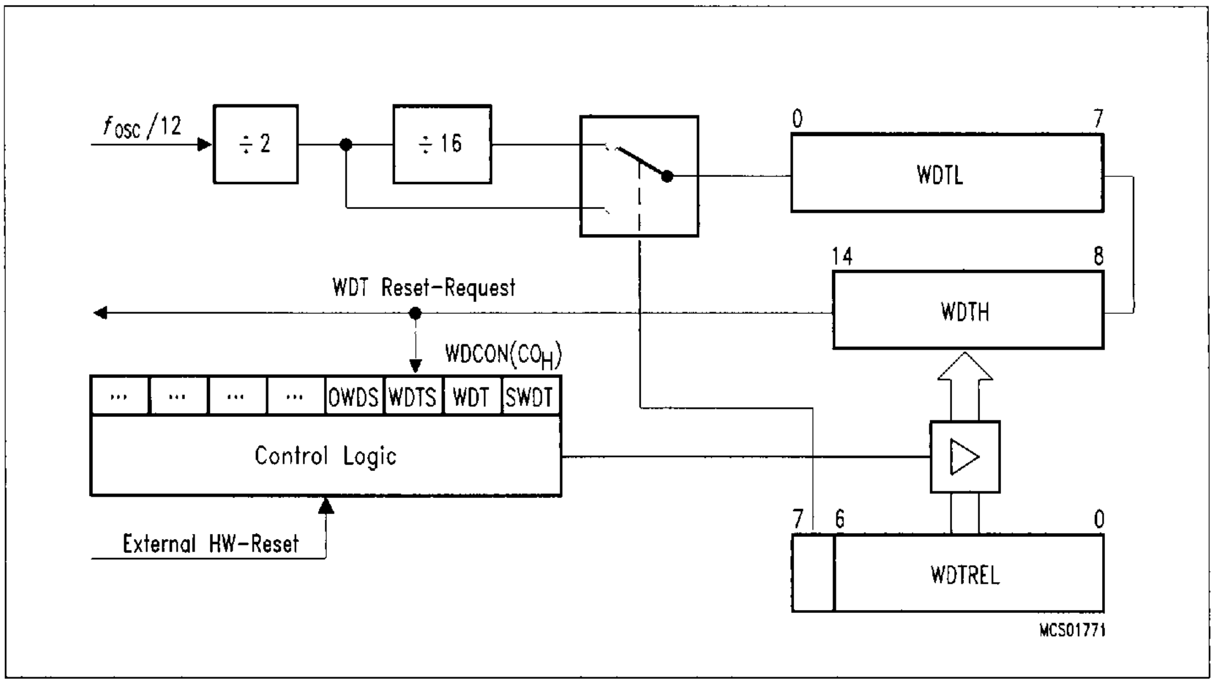

Figure 5
Block Diagram of the Programmable Watchdog Timer

– Starting and refreshing the WDT

Table 13 gives an overview how to start and refresh the WDT. The mentioned bits are located in SFR WDCON.

Table 13
Starting and Refreshing the WDT

Function	Example		Remarks
Starting WD	SETB	SWDT	Cannot be stopped during active mode of the device. WDT is halted during idle mode, power down mode or the oscillator watchdog reset is active.
Refreshing WD	SETB SETB	WDT SWDT	Double instruction sequence (setting bit WDT and SWDT consecutively) to increase system security.

– Watchdog reset and watchdog status flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state $7FFC_H$. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS (SFR WDCON) is set. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

2) Oscillator Watchdog (OWD)

The OWD consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

Figure 6 shows the block diagram of the oscillator watchdog unit while **table 14** shows the effect when the OWD becomes active/inactive.

Note: The OWD is always enabled!

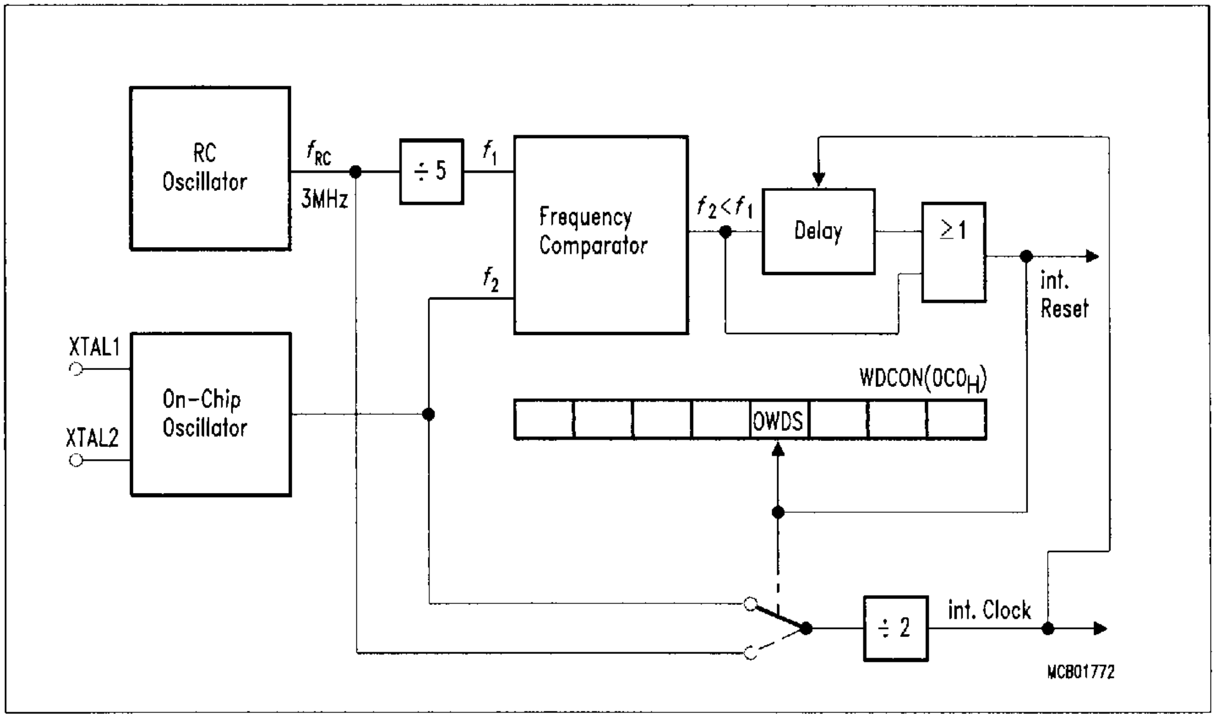

Figure 6
Functional Block Diagram of the Oscillator Watchdog

Table 14
Effects of the OWD

Conditions	Effect
$f_{OSC} < f_{RC}/5$	Switch input of internal clock system to RC oscillator output Activating internal reset at the same time (reset sequence is clocked by RC-oscillator). Exception from effects of a Hardware Reset: Watchdog Timer Status Flag, WDTS is not reset Oscillator Watchdog Status Flag, OWDS is set
$f_{OSC} > f_{RC}/5$	Input of internal clock system is $f_{OSC}/2$. When failure condition ($f_{OSC} < f_{RC}/5$) disappears the part executes a final reset phase of typ. 1 ms in order to allow the external oscillator to stabilize.

Fast Internal Reset after Power-On

The SAB-C502 can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Normally members of the 8051 family enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up timed of the oscillator is relatively long (typ. 1 ms). During this time period the pins have an undefined state which could have severe effects e.g. to actuators connected to port pins.

In the SAB-C502 the oscillator watchdog unit avoids this situation. After power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 µs). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is valid the watchdog uses the RC oscillator output as a clock source for the chip rather than the on-chip oscillator's 16 output. This allows correct resetting of the part and brings also all ports to the defined state.

Delay between power-on and correct reset state:

Typ: 18 µs

Max: 34 µs

Power Saving Modes

Two power down modes are available, the Idle Mode and the Power Down Mode.

The bits PDE, PDS and IDLE, IDLS select the Power Down mode or the idle mode, respectively. If the Power Down mode and the idle mode are set at the same time, Power Down takes precedence. **Table 15** gives a general overview of the power saving modes.

Table 15
Entering and Leaving the Power Saving Modes

Mode	Entering Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active Double instruction sequence
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillators are stopped. Contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR's contents.) Double instruction sequence

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) .... – 40 °C to + 85 °C
Storage temperature (T_{ST}) .... – 65 °C to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) .... – 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) .... – 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition .... – 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .... | 100 mA |

Power dissipation .... TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 to + 70 °C for the SAB-C502
T_A = – 40 to + 85 °C for the SAF-C502

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except $\overline{EA}$, RESET, XTAL1)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to RESET, $\overline{EA}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA[1)]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA[1)]
Output high voltage (ports 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA[2)], I_{OH} = – 80 µA[2)]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$, P1)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 °C
Power supply current:					
Active mode, 12 MHz[7)]	I_{CC}	–	23.3	mA	V_{CC} = 5 V,[4)]
Idle mode, 12 MHz[7)]	I_{CC}	–	7.4	mA	V_{CC} = 5 V,[5)]
Active mode, 20 MHz[7)]	I_{CC}	–	33.9	mA	V_{CC} = 5 V,[4)]
Idle mode, 20 MHz[7)]	I_{CC}	–	10.6	mA	V_{CC} = 5 V,[5)]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 … 5.5 V,[3)]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{\text{EA}}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ – 0.5 V; XTAL2 = N.C.;
$\overline{\text{EA}}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS}$ + 0.5 V, $V_{IH} = V_{CC}$ – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{\text{EA}}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

7) $I_{CC\,max}$ at other frequencies is given by:
active mode: $I_{CC\,max} = 1.32 \times f_{OSC} + 7.48$
idle mode: $I_{CC\,max} = 0.40 \times f_{OSC} + 2.62$
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

AC Characteristics for SAB-C502-L / C502-2R

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to + 70 °C for the SAB-C502
T_A = – 40 °C to + 85 °C for the SAF-C502

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}$ – 40	–	ns
Address setup to ALE	t_{AVLL}	43	–	t_{CLCL} – 40	–	ns
Address hold after ALE	t_{LLAX}	30	–	t_{CLCL} – 53	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL}$ – 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL}$ – 35	–	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL}$ – 100	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ} *)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{PSEN}$	t_{PXAV} *)	75	–	t_{CLCL} – 8	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL}$ – 115	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C502-L/C502-2R to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

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AC Characteristics for SAB-C502-L / C502-2R

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	30	–	$t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for SAB-C502-L20 / C502-2R20

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V

T_A = 0 °C to + 70 °C for the SAB-C502
T_A = – 40 °C to + 85 °C for the SAF-C502

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	20	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	20	–	$t_{CLCL} - 30$	–	ns
ALE low to valid instr in	t_{LLIV}	–	100	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	25	–	$t_{CLCL} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	115	–	$3t_{CLCL} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	75	–	$3t_{CLCL} - 75$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	40	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	47	–	$t_{CLCL} - 3$	–	ns
Address to valid instr in	t_{AVIV}	–	190	–	$5t_{CLCL} - 60$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB-C502-L20/C502-2R20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C502-L20 / C502-2R20

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	200	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	200	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	20	–	$t_{CLCL} - 30$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	155	–	$5t_{CLCL} - 95$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	76	–	$2t_{CLCL} - 24$	ns
ALE to valid data in	t_{LLDV}	–	250	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	285	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	100	200	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	20	80	$t_{CLCL} - 30$	$t_{CLCL} + 30$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 45$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	200	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	–	$t_{CLCL} - 40$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

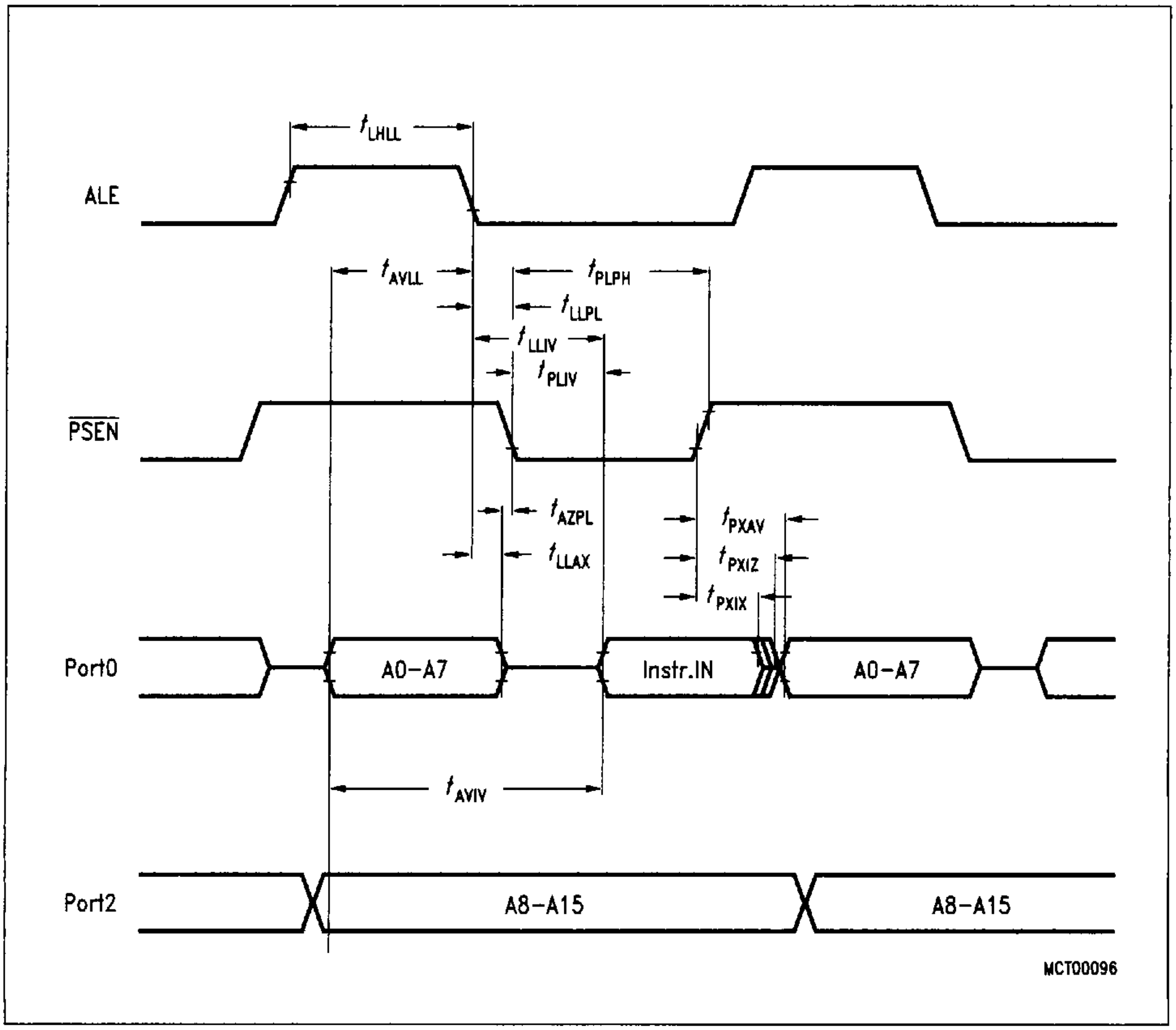


Figure 7
Program Memory Read Cycle

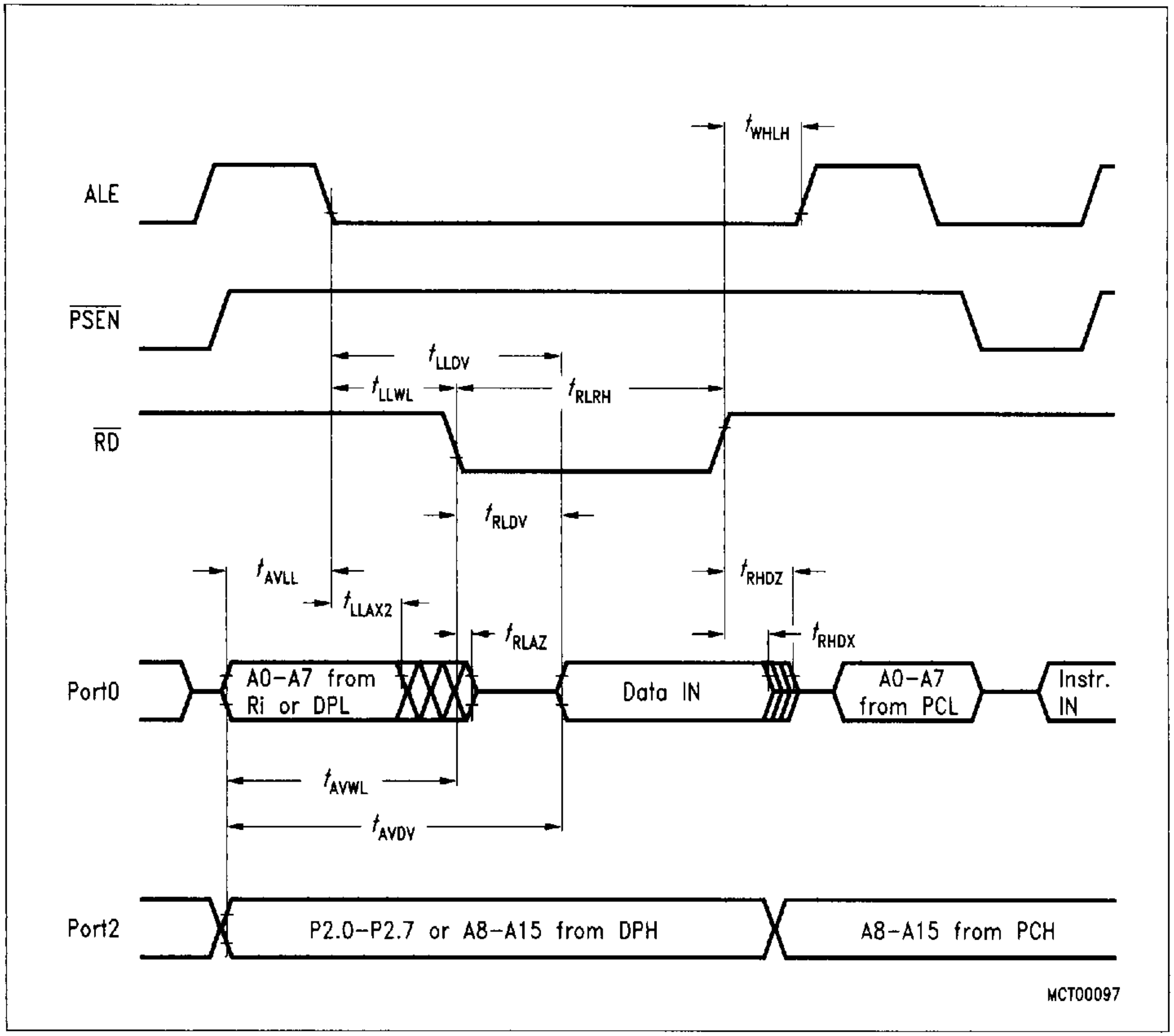


Figure 8
Data Memory Read Cycle

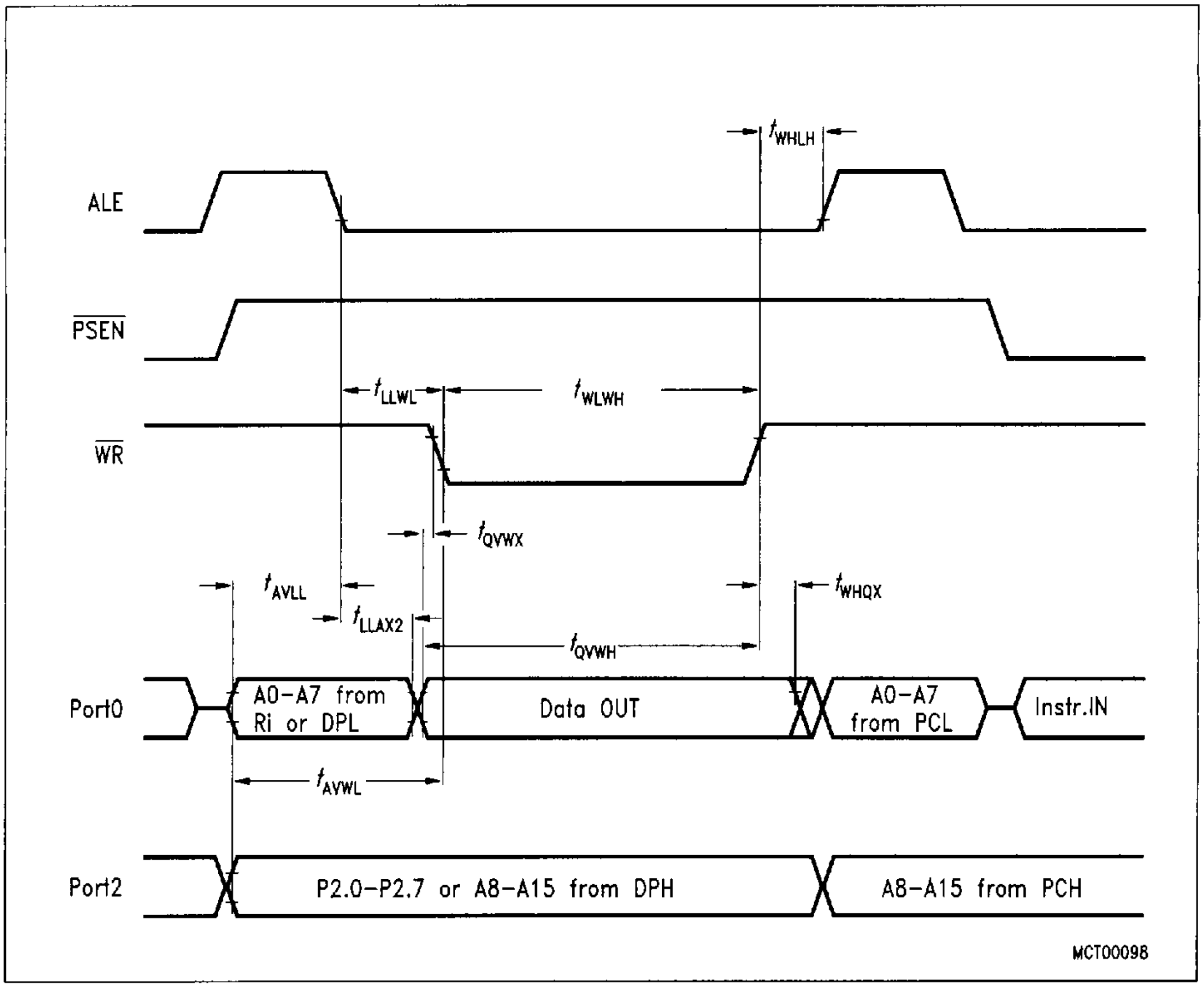


Figure 9
Data Memory Write Cycle

ROM Verification Characteristics for SAB-C502-2R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

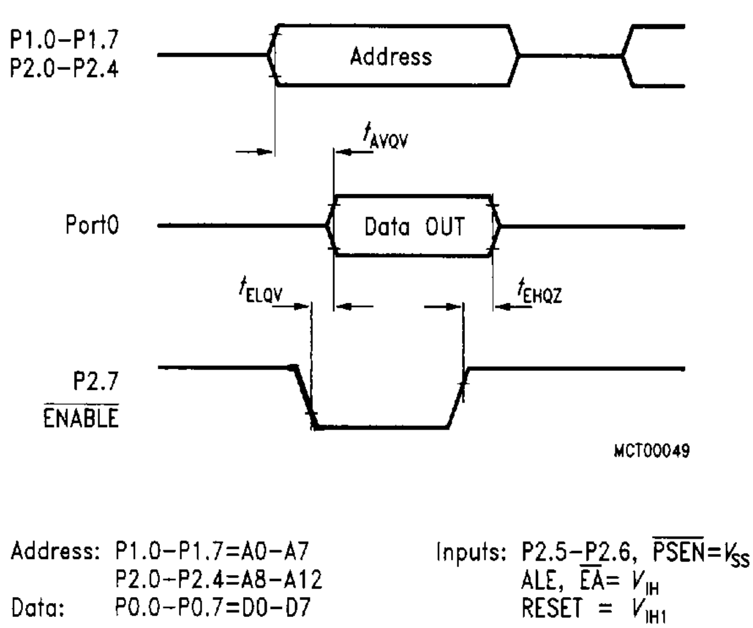
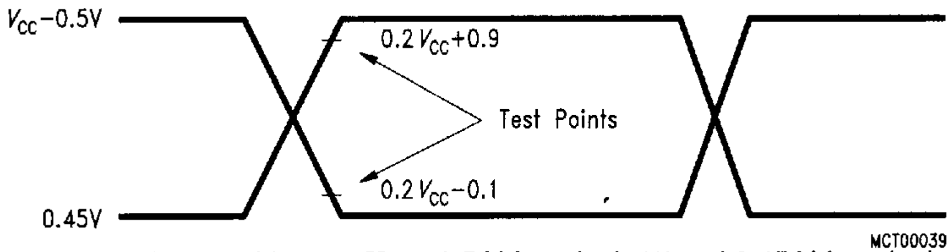
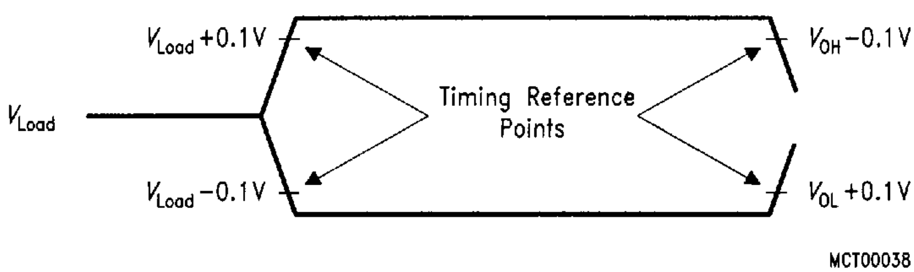


Figure 10
ROM Verification Mode 1



AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 11
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs.
I_{OL} / I_{OH} ≥ ± 20 mA.

Figure 12
AC Testing: Float Waveforms

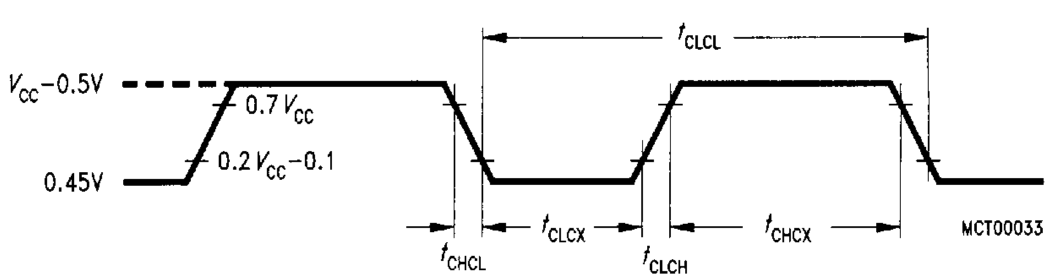


Figure 13
External Clock Cycle

8235605 0061313 140

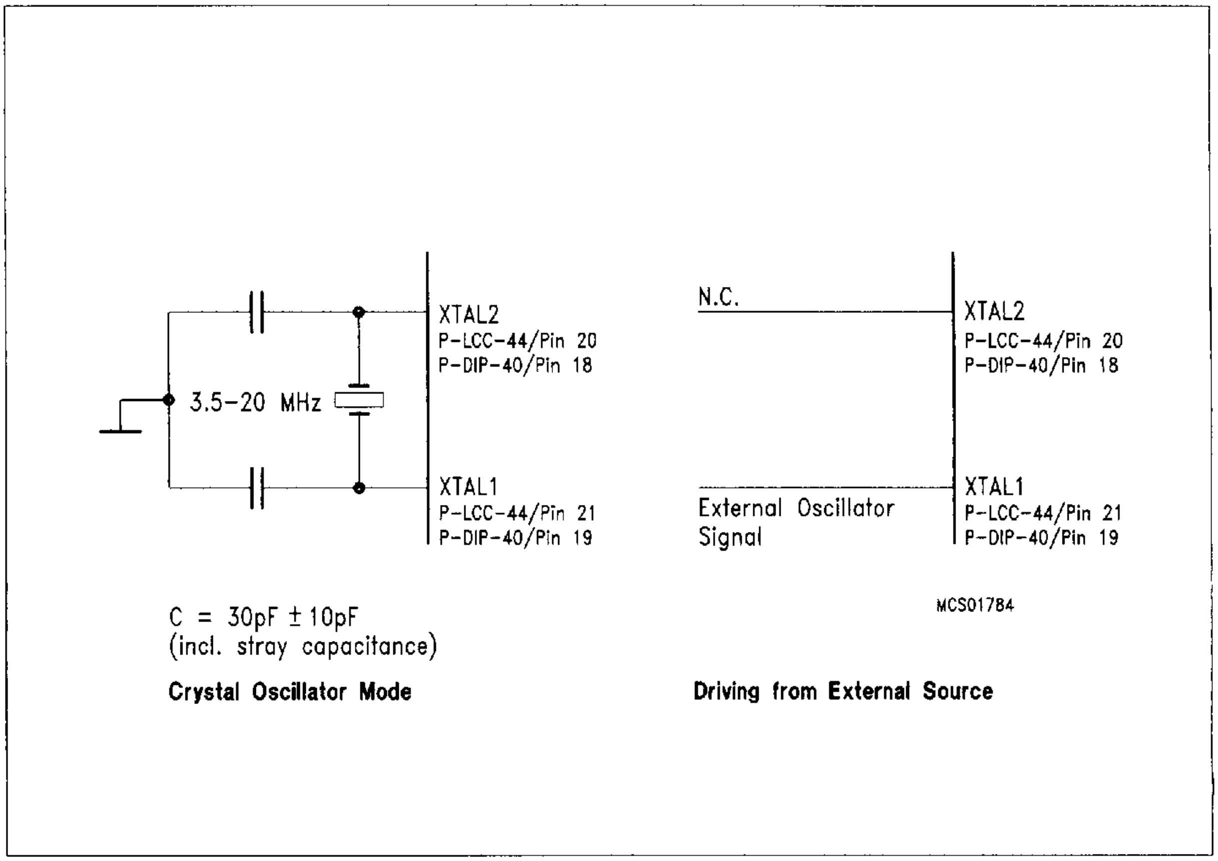


Figure 14
Recommended Oscillator Circuits