High-Speed, Low-Glitch D/CMOS Analog Switches

FEATURES

- Fast Switching— t_{ON}: 12 ns
- Low Charge Injection: ±2 pC
- Wide Bandwidth: 500 MHz
- 5-V CMOS Logic Compatible
- Low $r_{DS(on)}$: 18 Ω
- Low Quiescent Power : 1.2 nW
- Single Supply Operation

BENEFITS

- Improved Data Throughput
- Minimal Switching Transients
- Improved System Performance
- Easily Interfaced
- Low Insertion Loss
- Minimal Power Consumption

APPLICATIONS

- Fast Sample-and-Holds
- Synchronous Demodulators
- Pixel-Rate Video Switching
- Disk/Tape Drives
- DAC Deglitching
- Switched Capacitor Filters
- GaAs FET Drivers
- Satellite Receivers

DESCRIPTION

The DG611/612/613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

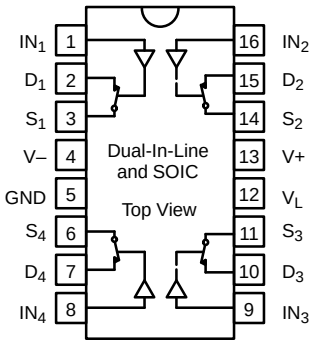
Each switch conducts equally well in both directions when on and blocks up to 16 V_{p-p} when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611/612/613 are built on the Vishay Siliconix proprietary D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

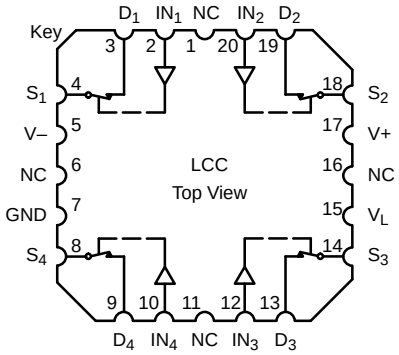
For additional information see Applications Note AN207 (FaxBack number 70605).

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG611



DG611



Four SPST Switches per Package

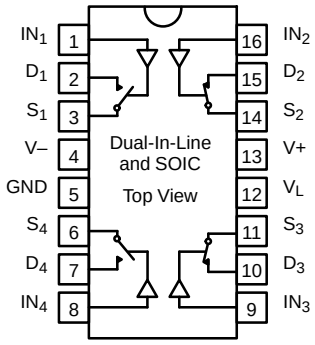
TRUTH TABLE

Logic	DG611	DG612
0	ON	OFF
1	OFF	ON

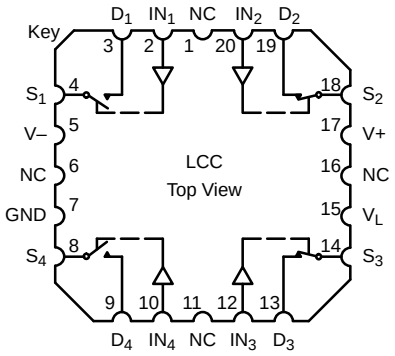
Logic “0” ≤ 1 V
Logic “1” ≥ 4 V

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG613



DG613



Four SPST Switches per Package

TRUTH TABLE

Logic	SW_1, SW_4	SW_2, SW_3
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 1 V
Logic "1" ≥ 4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
DG611/612		
–40 to 85°C	16-Pin Plastic DIP	DG611DJ
		DG612DJ
	16-Pin Narrow SOIC	DG611DY
		DG612DY
–55 to 125°C	16-Pin CerDIP	DG611AK/883, 5962-9325501MEA
		DG612AK/883, 5962-9325502MEA
	LCC-20	DG611AZ/883, 5962-9325501M2A
		DG612AZ/883, 5962-9325502M2A
DG613		
–40 to 85°C	16-Pin Plastic DIP	DG613DJ
	16-Pin Narrow SOIC	DG613DY
–55 to 125°C	16-Pin CerDIP	DG613AK/883, 5962-9325503MEA
	LCC-20	DG613AZ/883, 5962-9325503M2A

ABSOLUTE MAXIMUM RATINGS

V+ to V– . . . . . –0.3 V to 21 V
V+ to GND . . . . . –0.3 V to 21 V
V– to GND . . . . . –19 V to 0.3 V
V_L to GND . . . . . –1 V to (V+) + 1 V
or 20 mA, whichever occurs first
V_{IN}[a] . . . . . (V–) –1 V to (V+) + 1 V
or 20 mA, whichever occurs first
V_S, V_D[a] . . . . . (V–) –0.3 V to (V–) + 16 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) . . . . . ±30 mA
Current, S or D (Pulsed at 1 μs, 10% Duty Cycle) . . . . . ±100 mA

Storage Temperature: CerDIP . . . . . –65 to 150°C
Plastic . . . . . –65 to 125°C
Power Dissipation (Package)b
16-Pin Plastic DIP[c] . . . . . 470 mW
16-Pin Narrow SOIC[d] . . . . . 600 mW
16-Pin CerDIP[e] . . . . . 900 mW
20-Pin LCC[e] . . . . . 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

RECOMMENDED OPERATING RANGE

V+ . . . . . 5 V to 21 V
V– . . . . . –10 V to 0 V
V_L . . . . . 4 V to V+
V_{IN} . . . . . 0 V to V_L
V_{ANALOG} . . . . . V– to (V+) – 5 V

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –3 V V_L = 5 V, V_{IN} = 4 V, 1 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}	V– = –5 V, V+ = 12 V	Full		–5	7	–5	7	V
Switch On-Resistance	$r_{DS(on)}$	I_S = –1 mA, V_D = 0 V	Room Full	18		45 60		45 60	Ω
Resistance Match Bet Ch.	$\Delta r_{DS(on)}$		Room	2					
Source Off Leakage	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Hot	±0.001	–0.25 –20	0.25 20	–0.25 –20	0.25 20	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V	Room Hot	±0.001	–0.25 –20	0.25 20	–0.25 –20	0.25 20	
Switch On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Hot	±0.001	–0.4 –40	0.4 40	–0.4 –40	0.4 40	
Digital Control									
Input Voltage High	V_{IH}		Full		4		4		V
Input Voltage Low	V_{IL}		Full			1		1	
Input Current	I_{IN}		Room Hot	0.005	–1 –20	1 20	–1 –20	1 20	µA
Input Capacitance	C_{IN}		Room	5					pF
Dynamic Characteristics									
Off State Input Capacitance	$C_{S(off)}$	V_S = 0 V	Room	3					pF
Off State Output Capacitance	$C_{D(off)}$	V_D = 0 V	Room	2					
On State Input Capacitance	$C_{S(on)}$	V_S = V_D = 0 V	Room	10					
Bandwidth	BW	R_L = 50 Ω	Room	500					MHz
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 3 pF, V_S = ±2 V See Test Circuit, Figure 2	Room	12		25		25	ns
Turn-Off Time[e]	t_{OFF}		Room	8		20		20	
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 75 pF V_S = ±2 V See Test Circuit, Figure 2	Room Full	19		35 50		35 50	
Turn-Off Time	t_{OFF}		Room Full	16		25 35		25 35	
Charge Injection[e]	Q	C_L = 1 nF, V_S= 0 V	Room	4					pC
Ch. Injection Change[e, g]	ΔQ	C_L = 1 nF, $\lvert V_S \rvert \leq$ 3 V	Room	3		4		4	
Off Isolation[e]	OIRR	R_{IN} = 50 Ω, R_L = 50 Ω f = 5 MHz	Room	74					dB
Crosstalk[e]	X_{TALK}	R_{IN} = 10 Ω, R_L = 50 Ω, f = 5 MHz	Room	87					
Power Supplies									
Positive Supply Curent	I+	V_{IN} = 0 V or 5 V	Room Full	0.005		1 5		1 5	µA
Negative Supply Current	I–		Room Full	–0.005	–1 –5		–1 –5		
Logic Supply Current	I_L		Room Full	0.005		1 5		1 5	
Ground Current	I_{GND}		Room Full	–0.005	–1 –5		–1 –5		

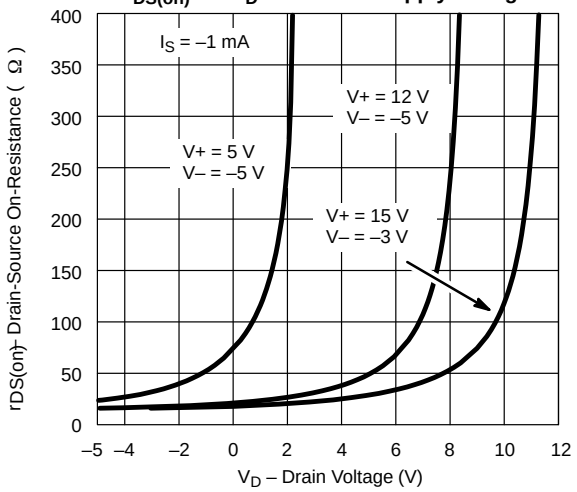
SPECIFICATIONS[a] FOR UNIPOLAR SUPPLIES

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –3 V V_L = 5 V, V_{IN} = 4 V, 1 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	7	0	7	V
Switch On-Resistance	$r_{DS(on)}$	I_S = –1 mA, V_D = 1 V	Room	25		60		60	Ω
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 3 pF, V_S = 2 V See Test Circuit, Figure 2	Room	15		30		30	ns
Turn-Off Time[e]	t_{OFF}		Room	10		25		25	

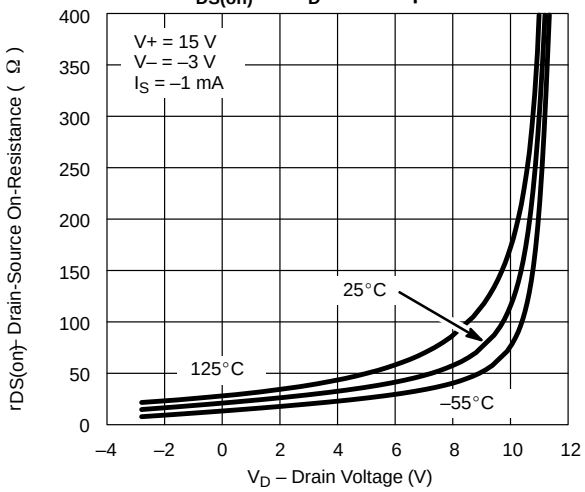
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta Q = |Q \text{ at } V_S = 3 \text{ V} - Q \text{ at } V_S = -3 \text{ V}|$.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

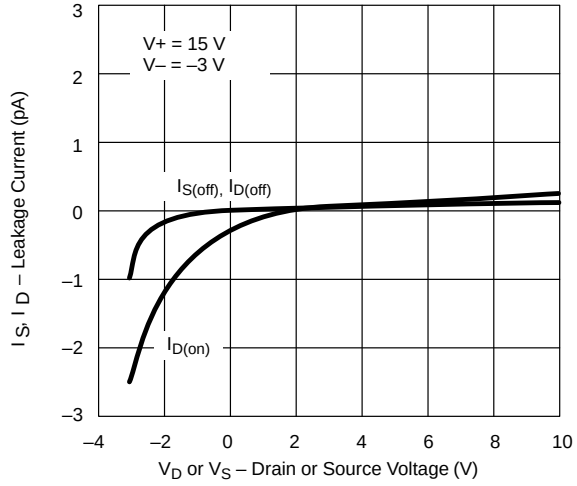
$r_{DS(on)}$ vs. V_D and Power Supply Voltages



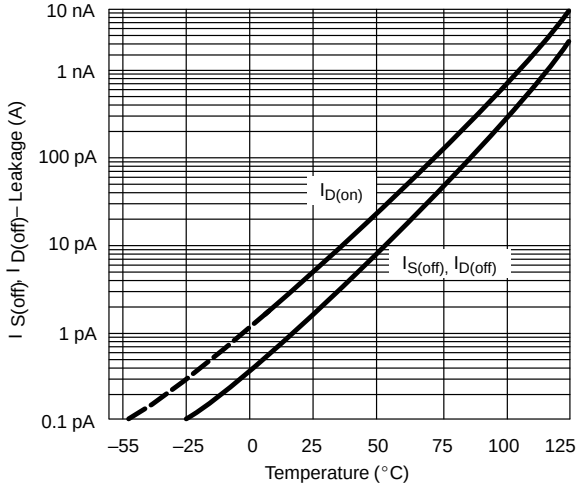
$r_{DS(on)}$ vs. V_D and Temperature



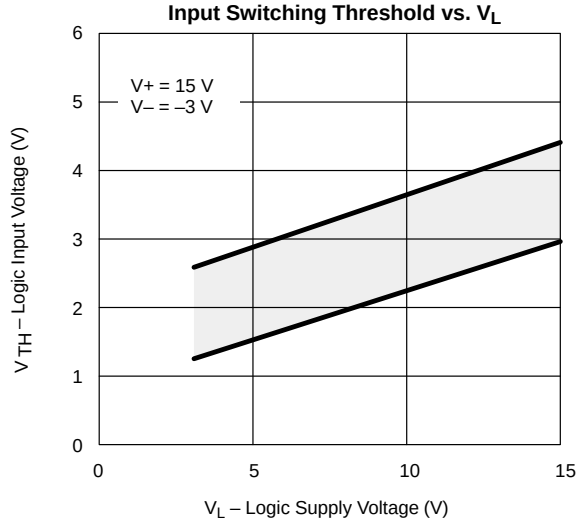
Leakage Current vs. Analog Voltage



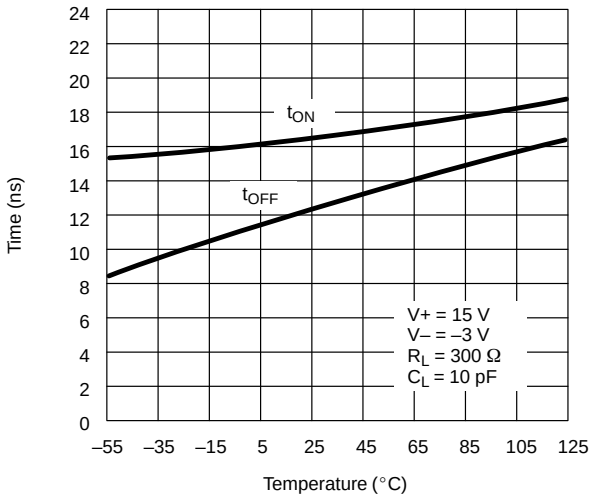
Leakage Currents vs. Temperature



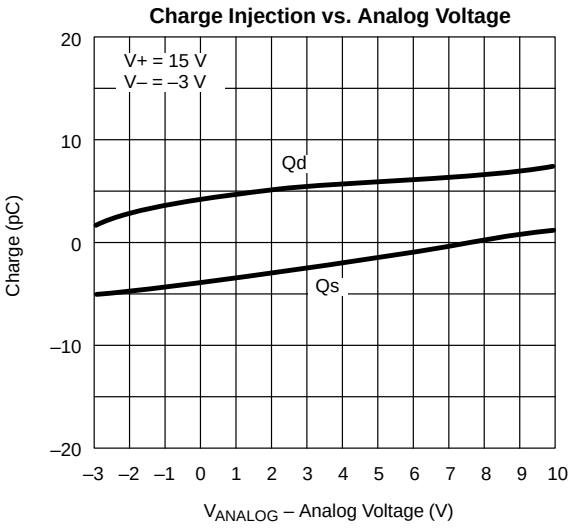
Input Switching Threshold vs. V_L

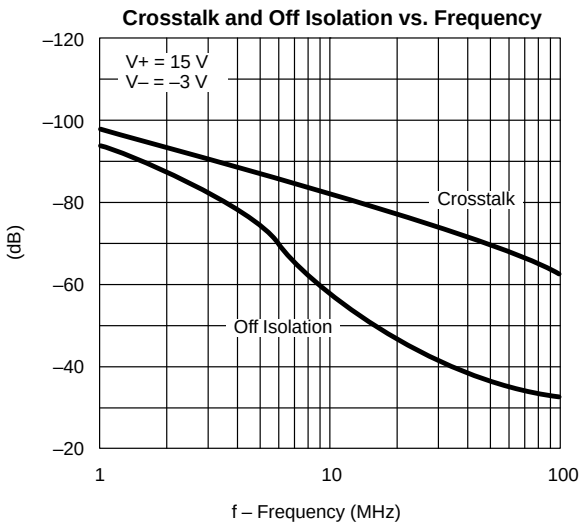


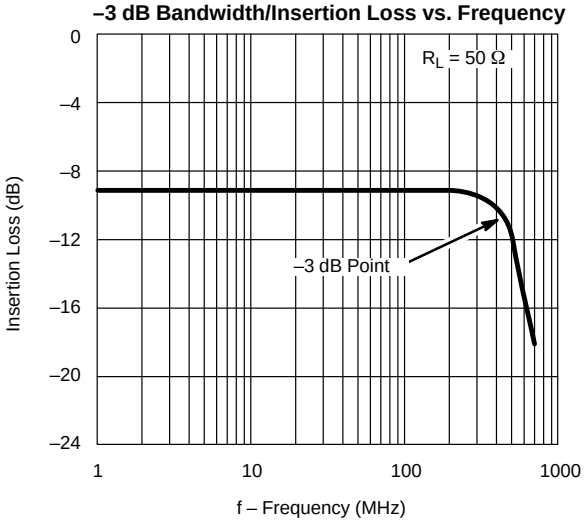
Switching Times vs. Temperature

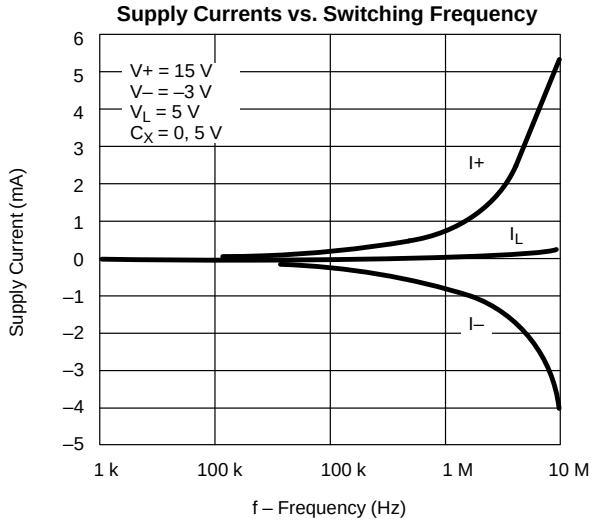


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)









SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

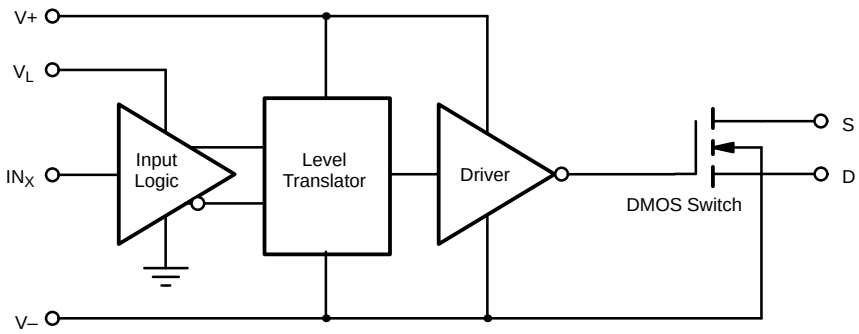


FIGURE 1.

TEST CIRCUITS

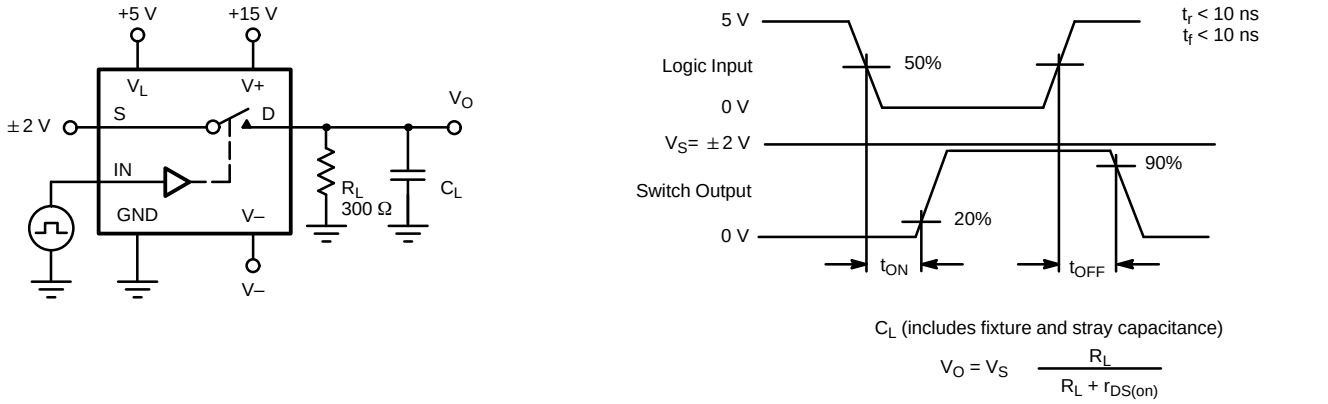


FIGURE 2. Switching Time

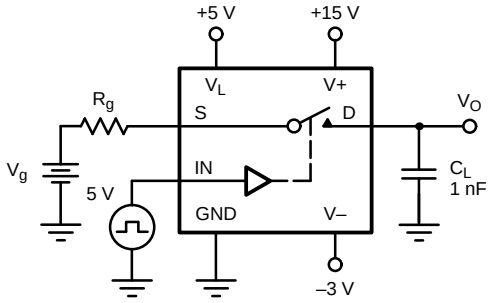


FIGURE 3. Charge Injection

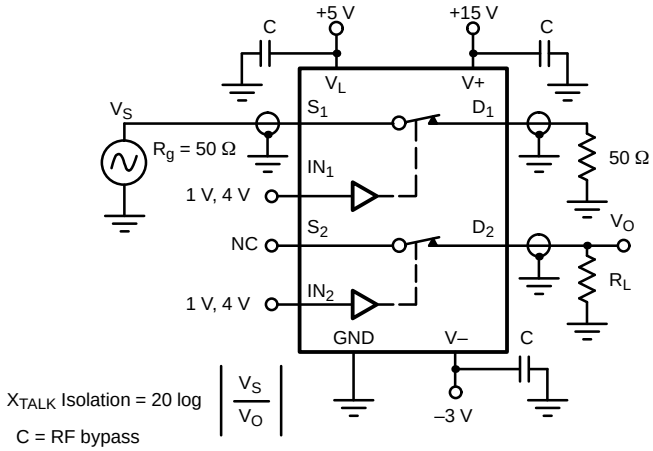


FIGURE 4. Crosstalk

APPLICATIONS

High-Speed Sample-and-Hold

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The CLC111, a fast input buffer, helps to shorten acquisition and settling times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (See Figure 5.)

Pixel-Rate Switch

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video sources must be sync locked. The glitch-less analog switch eliminates halos. (See Figure 6.)

GaAs FET Drivers

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S_1, whereas to turn it off, –8 V are applied via S_2. This high-speed, low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.

APPLICATIONS

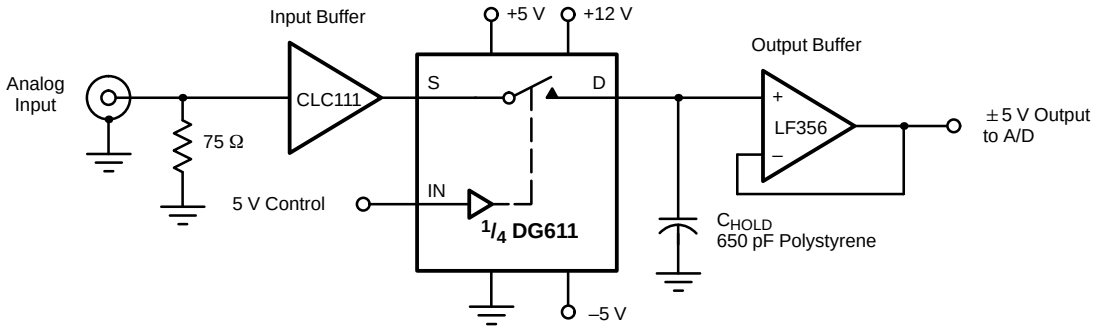


FIGURE 5. High-Speed Sample-and-Hold

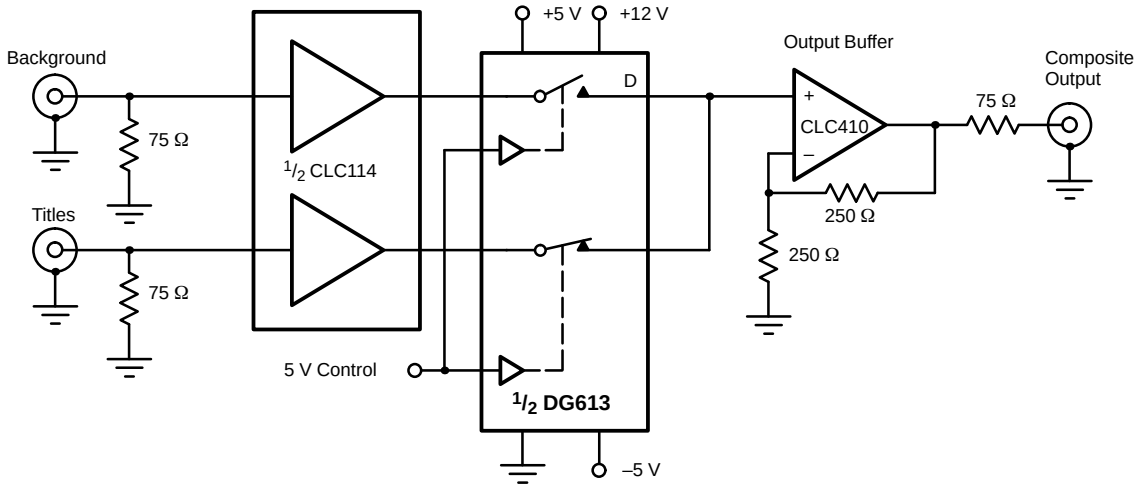


FIGURE 6. A Pixel-Rate Switch Creates Title Overlays

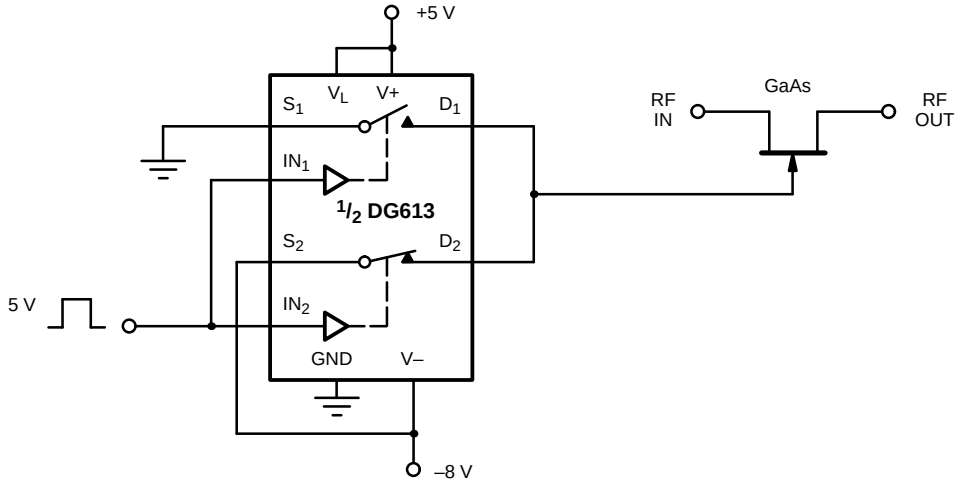


FIGURE 7. A High-Speed GaAs FET Driver that Saves Power