

# NLAS44599

## Low Voltage Single Supply Dual DPDT Analog Switch

The NLAS44599 is an advanced dual-independent CMOS double pole-double throw (DPDT) analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This DPDT controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The device has been designed so the ON resistance ( $R_{ON}$ ) is much lower and more linear over input voltage than  $R_{ON}$  of typical CMOS analog switches.

The channel select input is compatible with standard CMOS outputs.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The NLAS44599 can also be used as a quad 2-to-1 multiplexer-demultiplexer analog switch with two Select pins that each controls two multiplexer-demultiplexers.

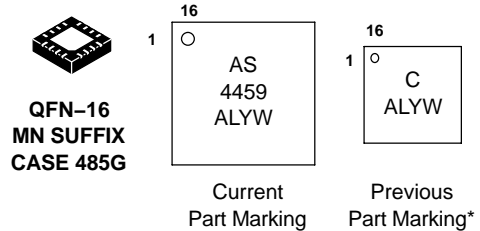
- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation:  $I_{CC} = 2 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch-up Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
- Chip Complexity: 158 FETs



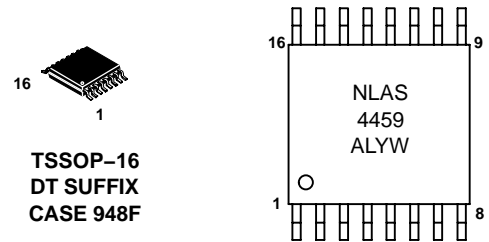
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS



\*Previous releases of this device may be marked as shown in this diagram.

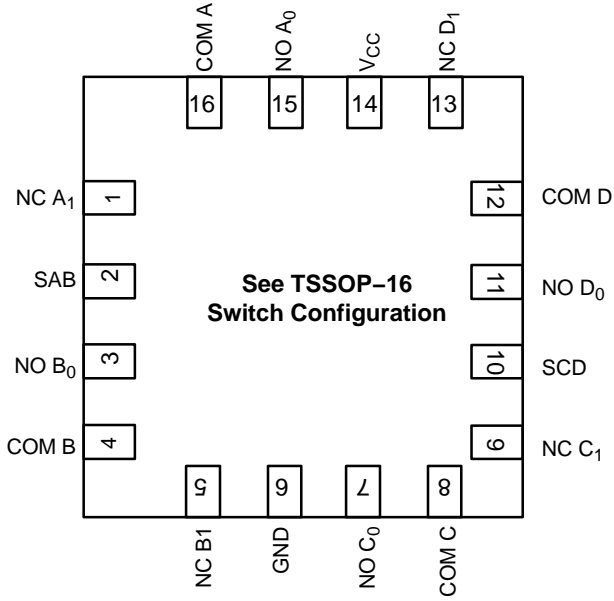


A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

QFN-16 PACKAGE



FUNCTION TABLE

Select AB or CD	On Channel
L	NC to COM
H	NO to COM

TSSOP-16 PACKAGE

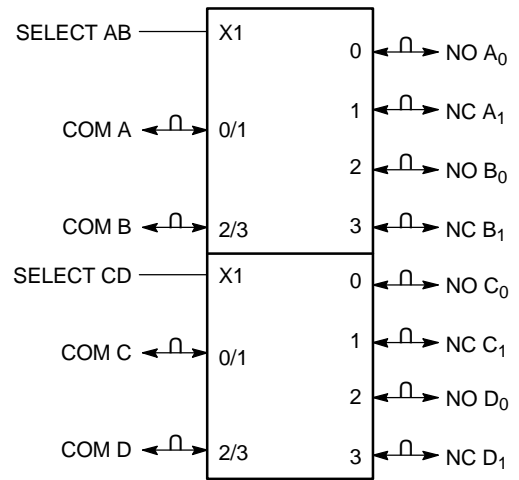
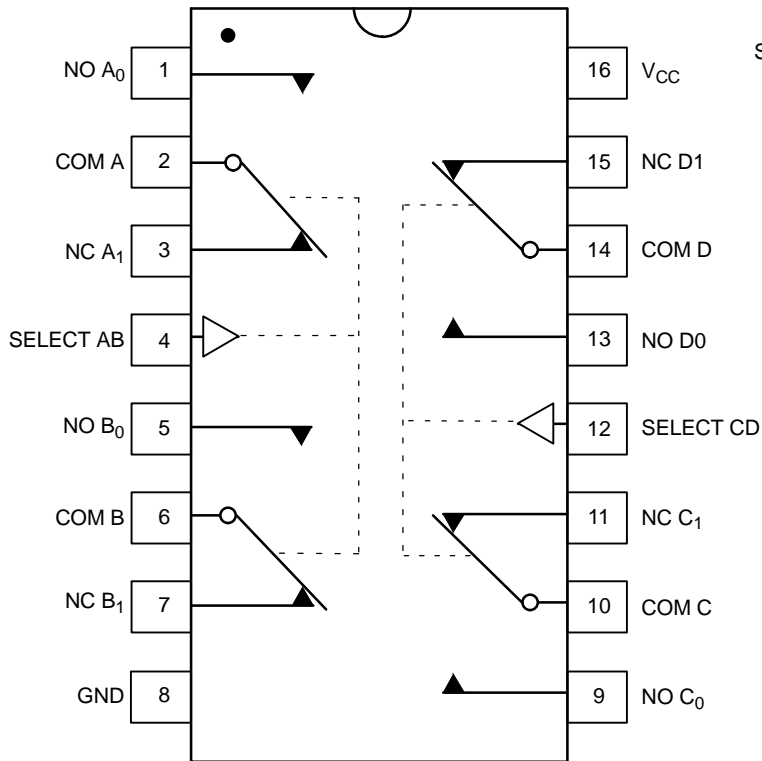


Figure 2. IEC Logic Symbol

Figure 1. Logic Diagram

**MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Positive DC Supply Voltage	-0.5 to +7.0	V	
V <sub>IS</sub>	Analog Input Voltage (V <sub>NO</sub> or V <sub>COM</sub> )	-0.5 ≤ V <sub>IS</sub> ≤ V <sub>CC</sub> + 0.5		
V <sub>IN</sub>	Digital Select Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0	V	
I <sub>IK</sub>	DC Current, Into or Out of Any Pin	±50	mA	
P <sub>D</sub>	Power Dissipation in Still Air	QFN-16 TSSOP-16	800 450	mW
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C	
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C	
MSL	Moisture Sensitivity	Level 1		
F <sub>R</sub>	Flammability Rating	Oxygen Index: 30% – 35%	UL 94-V0 (0.125 in)	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	2000 200 1000	V
I <sub>Latch-Up</sub>	Latch-Up Performance	Above V <sub>CC</sub> and Below GND at 125°C (Note 4)	±300	mA
θ <sub>JA</sub>	Thermal Resistance	QFN-16 TSSOP-16	80 164	°C/W

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	Digital Select Input Voltage	GND	5.5	V
V <sub>IS</sub>	Analog Input Voltage (NC, NO, COM)	GND	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Time, SELECT	V <sub>CC</sub> = 3.3 V ± 0.3 V V <sub>CC</sub> = 5.0 V ± 0.5 V	0 100 20	ns/V

**DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES**

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

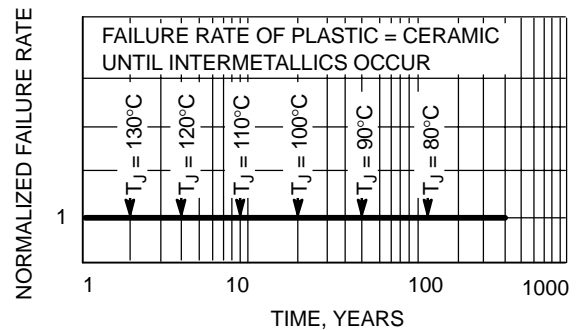


Figure 3. Failure Rate vs. Time Junction Temperature

# NLAS44599

## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub>	Guaranteed Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage, Select Inputs		2.0	1.5	1.5	1.5	V
			2.5	1.9	1.9	1.9	
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, Select Inputs		2.0	0.5	0.5	0.5	V
			2.5	0.6	0.6	0.6	
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I <sub>IN</sub>	Maximum Input Leakage Current, Select Inputs	V <sub>IN</sub> = 5.5 V or GND	5.5	±0.2	±2.0	±2.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0	±10	±10	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	Select and V <sub>IS</sub> = V <sub>CC</sub> or GND	5.5	4.0	4.0	8.0	μA

## DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V <sub>CC</sub>	Guaranteed Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
R <sub>ON</sub>	Maximum “ON” Resistance (Figures 17 – 23)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = GND to V <sub>CC</sub>  I <sub>IN</sub>   ≤ 10.0 mA	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
R <sub>FLAT (ON)</sub>	ON Resistance Flatness (Figures 17 – 23)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>IN</sub>   ≤ 10.0 mA V <sub>IS</sub> = 1 V, 2 V, 3.5 V	4.5	4	4	5	Ω
I <sub>NC(OFF)</sub> I <sub>NO(OFF)</sub>	NO or NC Off Leakage Current (Figure 9)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> or V <sub>NC</sub> = 1.0 V <sub>COM</sub> 4.5 V	5.5	1	10	100	nA
I <sub>COM(ON)</sub>	COM ON Leakage Current (Figure 9)	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>NO</sub> 1.0 V or 4.5 V with V <sub>NC</sub> floating or V <sub>NO</sub> 1.0 V or 4.5 V with V <sub>NO</sub> floating V <sub>COM</sub> = 1.0 V or 4.5 V	5.5	1	10	100	nA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3.0$  ns)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	V <sub>IS</sub> (V)	Guaranteed Maximum Limit						Unit	
					-55°C to 25°C			< 85°C		< 125°C		
					Min	Typ*	Max	Min	Max	Min		Max
t <sub>ON</sub>	Turn-On Time (Figures 12 and 13)	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 5 and 6)	2.5	2.0	5	23	35	5	38	5	41	ns
			3.0	2.0	5	16	24	5	27	5	30	
			4.5	3.0	2	11	16	2	19	2	22	
			5.5	3.0	2	9	14	2	17	2	20	
t <sub>OFF</sub>	Turn-Off Time (Figures 12 and 13)	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figures 5 and 6)	2.5	2.0	1	7	12	1	15	1	18	ns
			3.0	2.0	1	5	10	1	13	1	16	
			4.5	3.0	1	4	6	1	9	1	12	
			5.5	3.0	1	3	5	1	8	1	11	
t <sub>BBM</sub>	Minimum Break-Before-Make Time	V <sub>IS</sub> = 3.0 V (Figure 4) R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		

Symbol	Parameter	Typical @ 25, V <sub>CC</sub> = 5.0 V				Unit
		Min	Typ*	Max	Max	
C <sub>IN</sub>	Maximum Input Capacitance, Select Input		8			pF
C <sub>NO</sub> or C <sub>NC</sub>	Analog I/O (switch off)		10			
C <sub>COM</sub>	Common I/O (switch off)		10			
C <sub>(ON)</sub>	Feedthrough (switch on)		20			

\*Typical Characteristics are at 25°C.

**ADDITIONAL APPLICATION CHARACTERISTICS** (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V <sub>CC</sub> V	Typical	Unit
				25°C	
BW	Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 11)	V <sub>IN</sub> = 0 dBm V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	3.0	145	MHz
			4.5	170	
			5.5	175	
V <sub>ONL</sub>	Maximum Feedthrough On Loss	V <sub>IN</sub> = 0 dBm @ 100 kHz to 50 MHz V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	3.0	-3	dB
			4.5	-3	
			5.5	-3	
V <sub>ISO</sub>	Off-Channel Isolation (Figure 10)	f = 100 kHz; V <sub>IS</sub> = 1 V RMS V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	3.0	-93	dB
			4.5	-93	
			5.5	-93	
Q	Charge Injection Select Input to Common I/O (Figure 15)	V <sub>IN</sub> = V <sub>CC</sub> to GND, F <sub>IS</sub> = 20 kHz t <sub>r</sub> = t <sub>f</sub> = 3 ns R <sub>IS</sub> = 0 Ω, C <sub>L</sub> = 1000 pF Q = C <sub>L</sub> * ΔV <sub>OUT</sub> (Figure 8)	3.0	1.5	pC
			5.5	3.0	
THD	Total Harmonic Distortion THD + Noise (Figure 14)	F <sub>IS</sub> = 20 Hz to 100 kHz, R <sub>L</sub> = R <sub>gen</sub> = 600 Ω, C <sub>L</sub> = 50 pF V <sub>IS</sub> = 5.0 V <sub>PP</sub> sine wave	5.5	0.1	%
VCT	Channel-to-Channel Crosstalk	f = 100 kHz; V <sub>IS</sub> = 1 V RMS V <sub>IN</sub> centered between V <sub>CC</sub> and GND (Figure 7)	5.5	-90	dB
			3.0	-90	

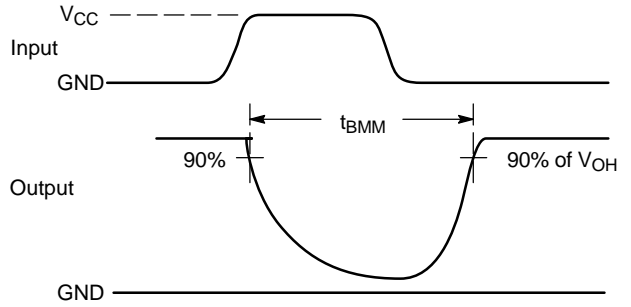
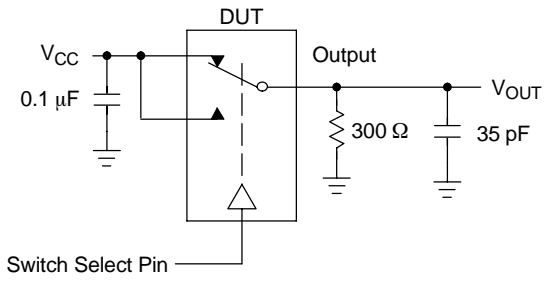


Figure 4.  $t_{BMM}$  (Time Break-Before-Make)

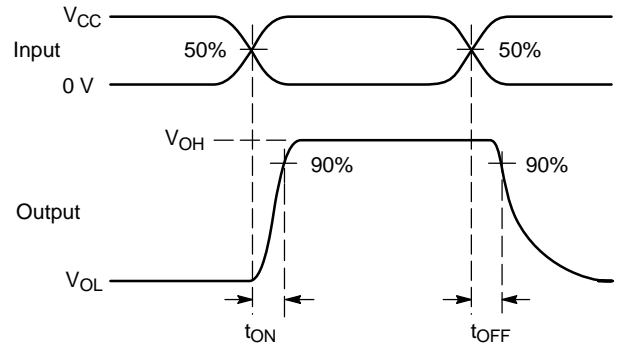
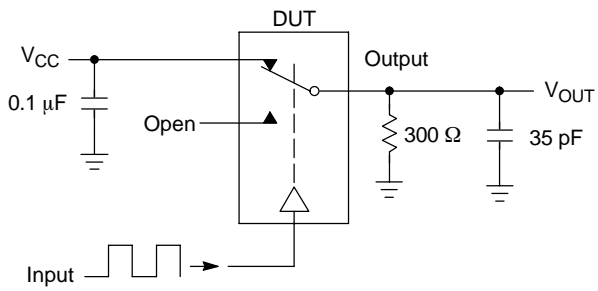


Figure 5.  $t_{ON}/t_{OFF}$

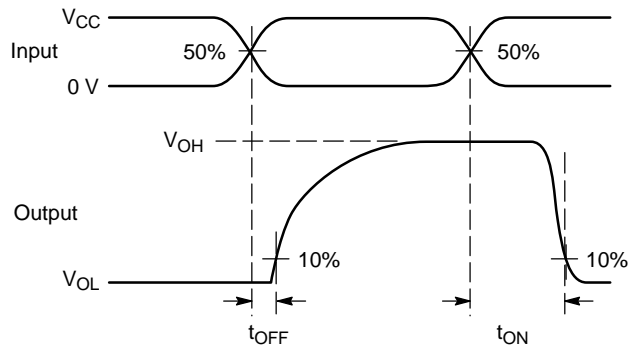
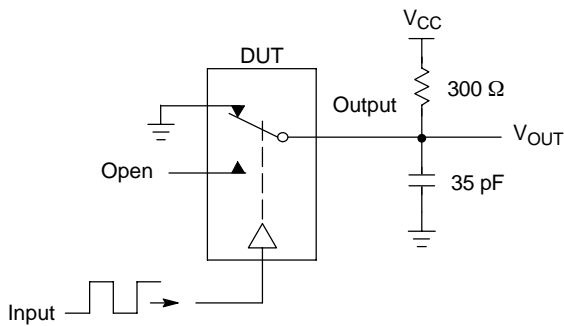
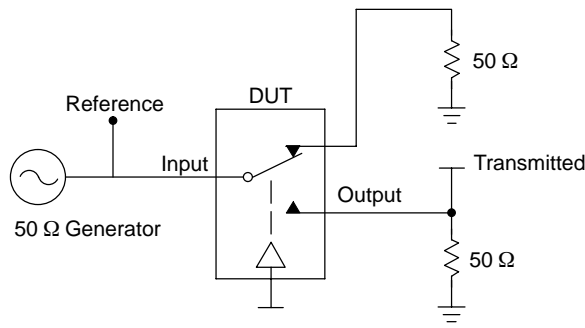


Figure 6.  $t_{ON}/t_{OFF}$



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

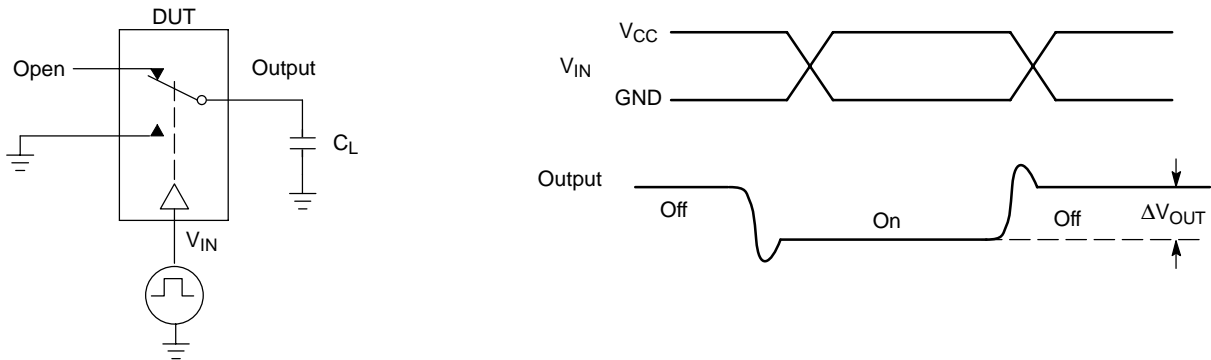
$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

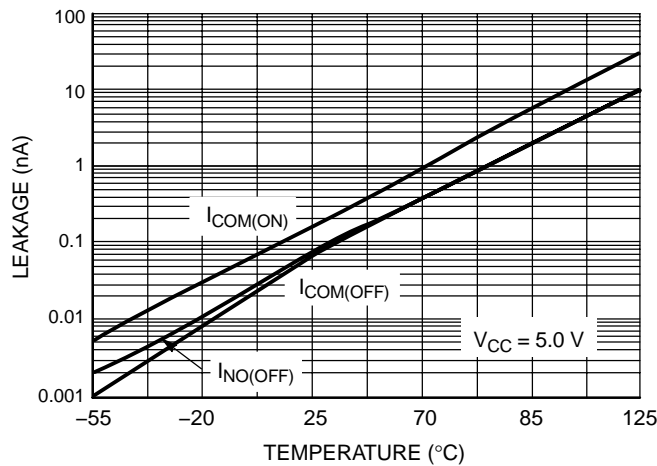
Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

$V_{CT}$  = Use  $V_{ISO}$  setup and test to all other switch analog input/outputs terminated with 50  $\Omega$

**Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**



**Figure 8. Charge Injection: (Q)**



**Figure 9. Switch Leakage vs. Temperature**

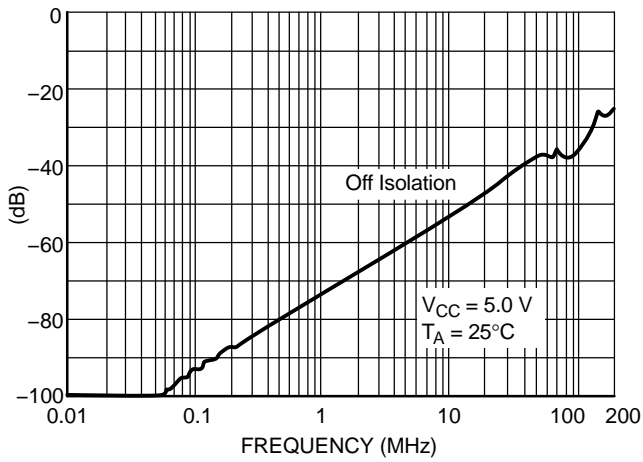


Figure 10. Off-Channel Isolation

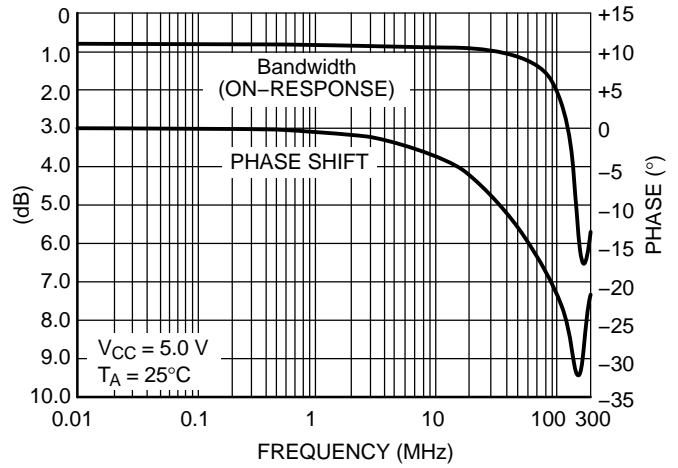


Figure 11. Typical Bandwidth and Phase Shift

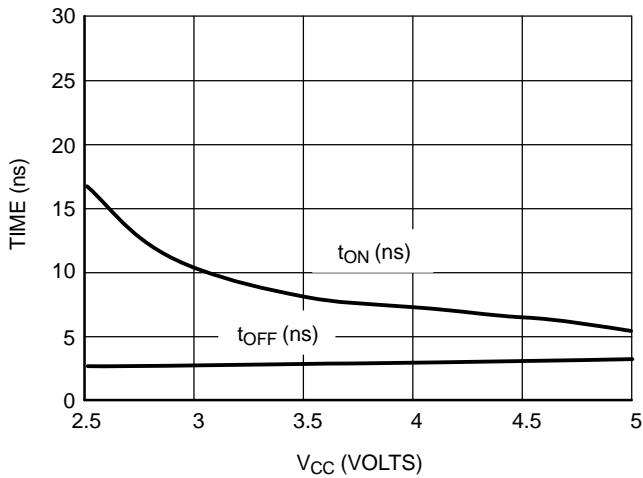


Figure 12. t<sub>ON</sub> and t<sub>OFF</sub> vs. V<sub>CC</sub> at 25°C

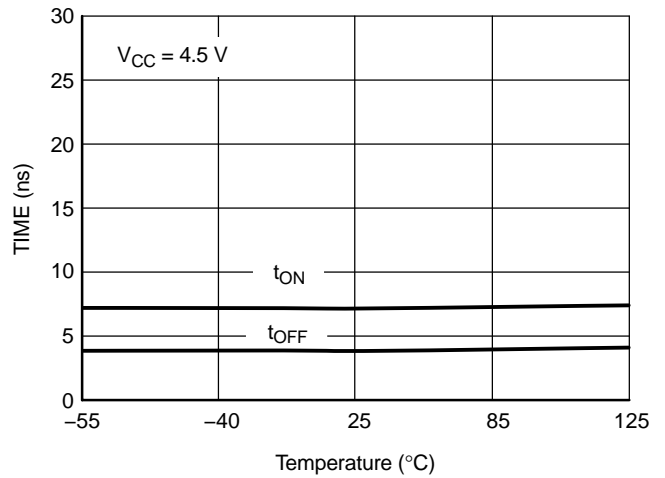


Figure 13. t<sub>ON</sub> and t<sub>OFF</sub> vs. Temp

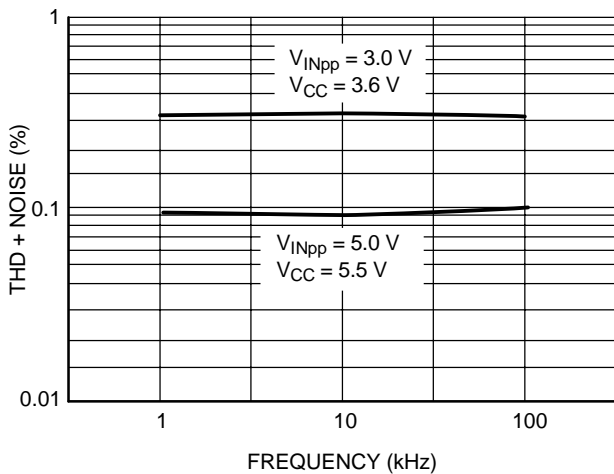


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

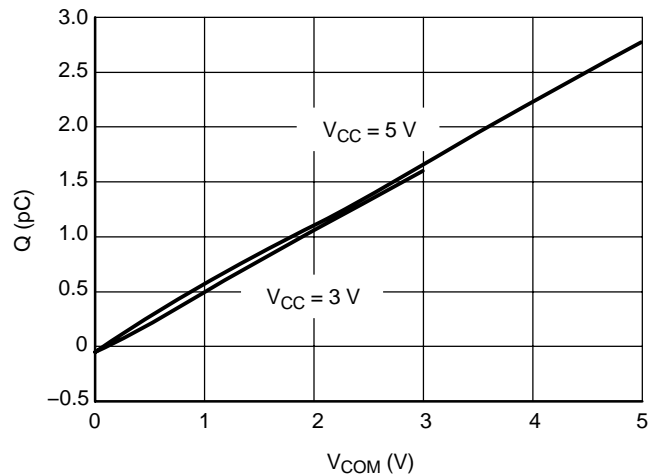


Figure 15. Charge Injection vs. COM Voltage



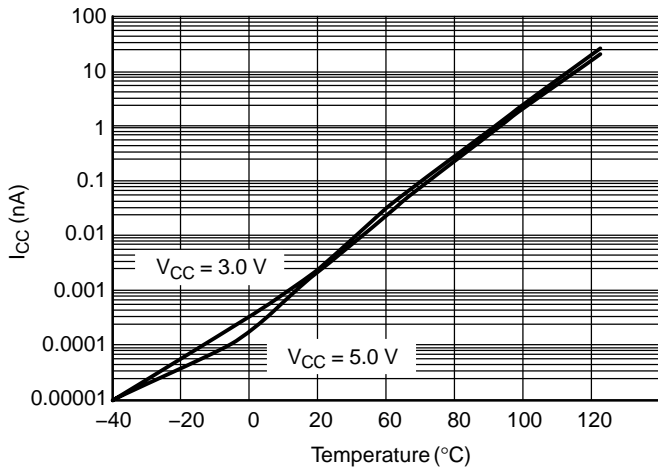


Figure 16.  $I_{CC}$  vs. Temp,  $V_{CC} = 3\text{ V}$  &  $5\text{ V}$

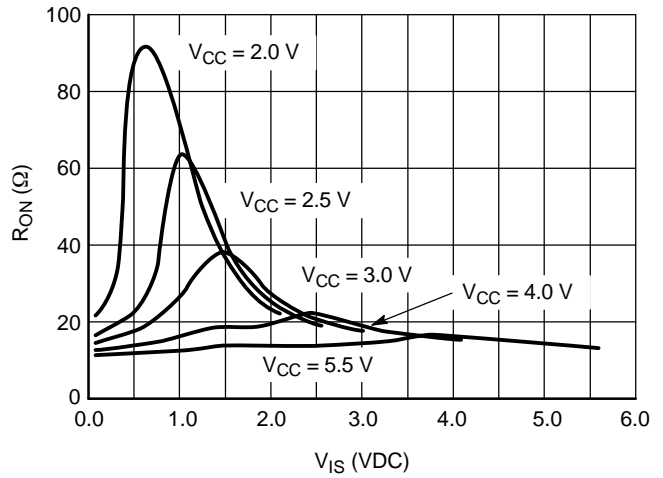


Figure 17.  $R_{ON}$  vs.  $V_{CC}$ , Temp =  $25^\circ\text{C}$

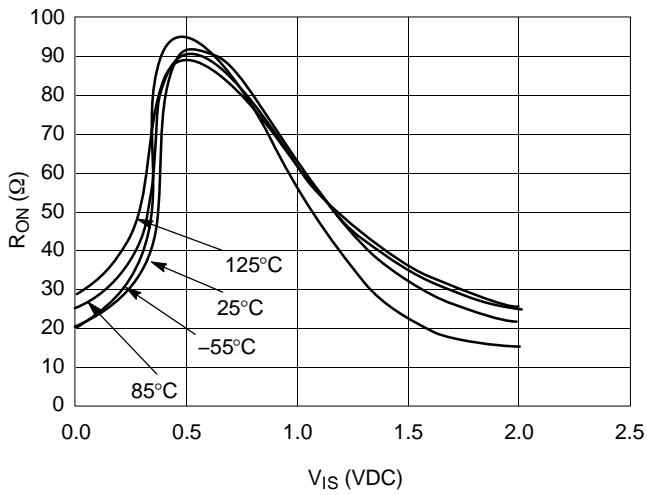


Figure 18.  $R_{ON}$  vs Temp,  $V_{CC} = 2.0\text{ V}$

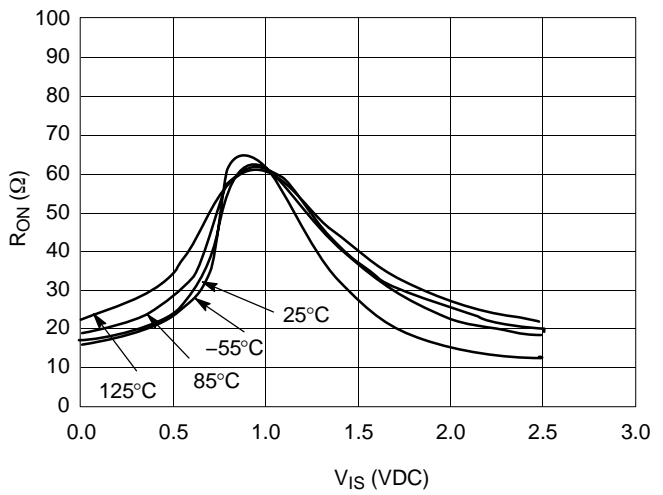


Figure 19.  $R_{ON}$  vs. Temp,  $V_{CC} = 2.5\text{ V}$

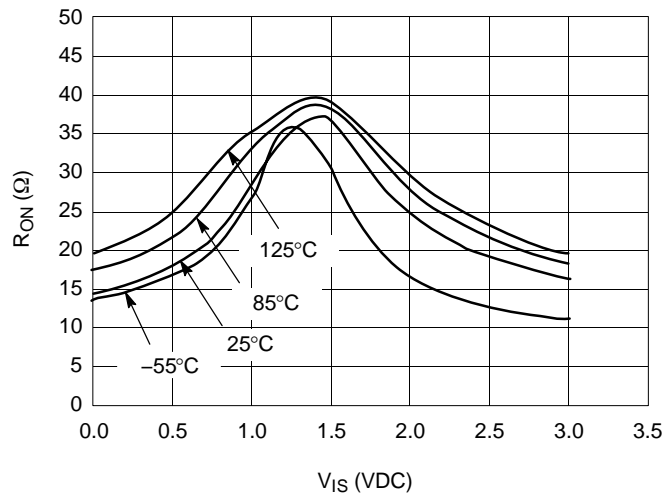


Figure 20.  $R_{ON}$  vs. Temp,  $V_{CC} = 3.0\text{ V}$

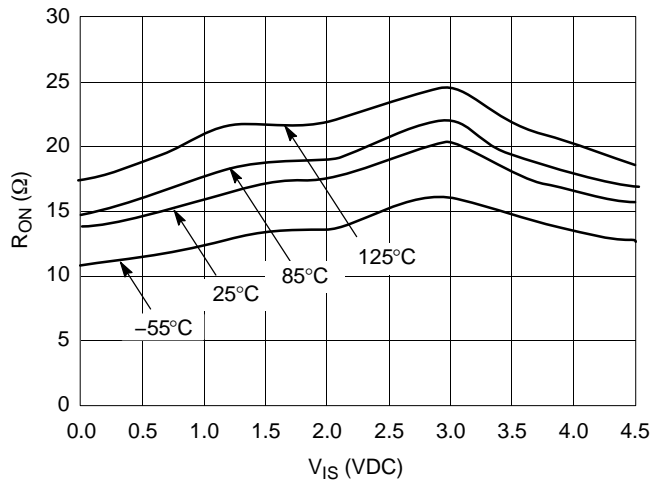


Figure 21.  $R_{ON}$  vs. Temp,  $V_{CC} = 4.5\text{ V}$

# NLAS44599

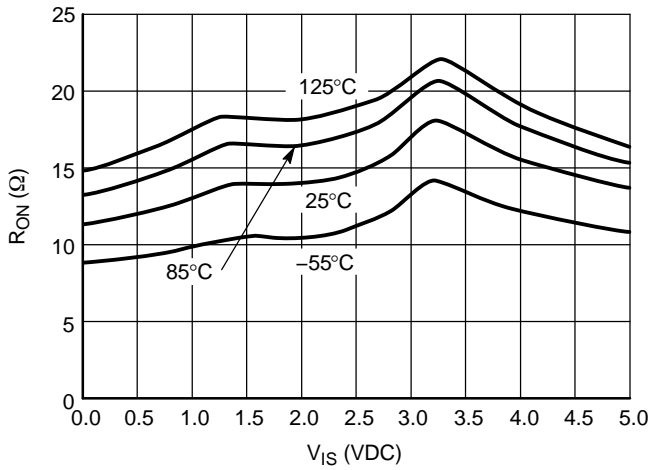


Figure 22.  $R_{ON}$  vs. Temp,  $V_{CC} = 5.0$  V

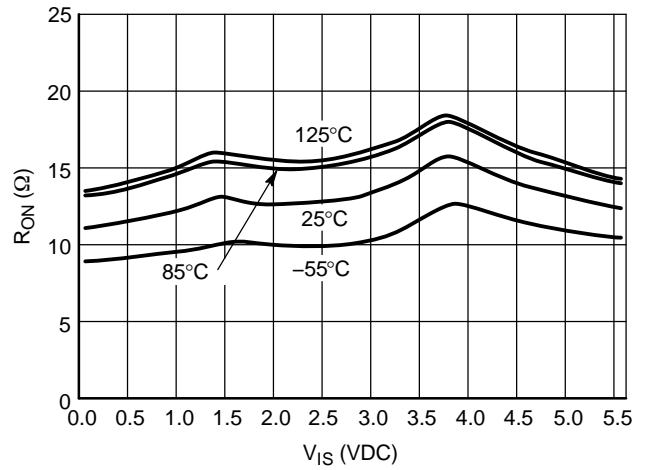


Figure 23.  $R_{ON}$  vs. Temp,  $V_{CC} = 5.5$  V

## DEVICE ORDERING INFORMATION

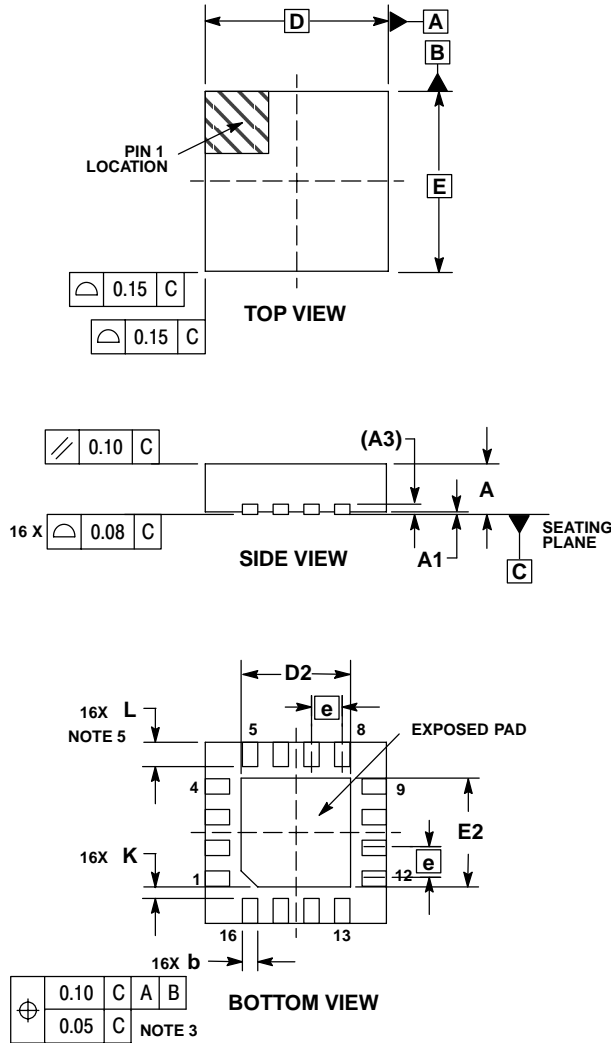
Device Order Number	Device Nomenclature					Package Type	Tape & Reel Size†
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAS44599MNR2	NL	AS	44599	MN	R2	QFN	13-inch/2500 Unit
NLAS44599DTR2	NL	AS	44599	DT	R2	TSSOP	13-inch/2500 Unit
NLAS44599MN	NL	AS	44599	MN		QFN	124 Unit Rail
NLAS44599DT	NL	AS	44599	DT		TSSOP	96 Unit Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NLAS44599

## PACKAGE DIMENSIONS

QFN-16  
MN SUFFIX  
CASE 485G-01  
ISSUE B

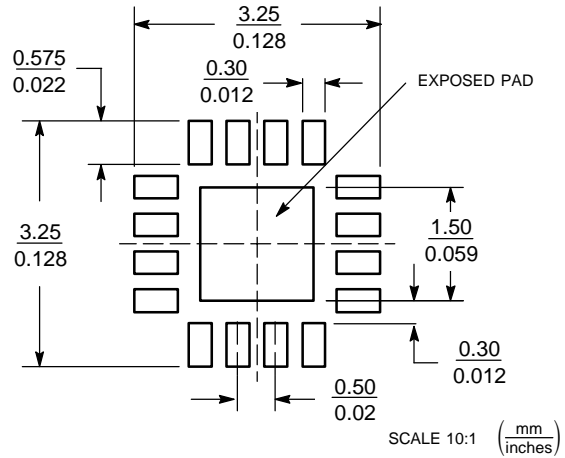


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L<sub>max</sub> CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	----
L	0.30	0.50

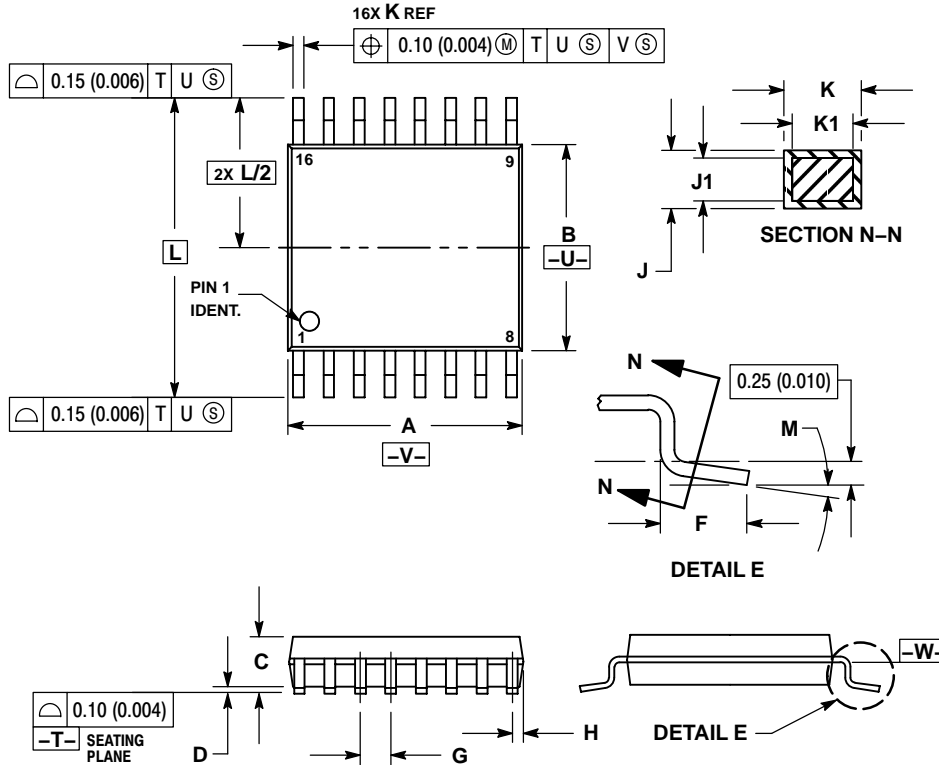
### SOLDERING FOOTPRINT



# NLAS44599

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

NLAS44599/D