

TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH245FU, TC7WH245FK

(UNDER DEVELOPMENT)

DUAL BUS TRANSCEIVER

The TC7WH245 is an advanced high speed CMOS DUAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

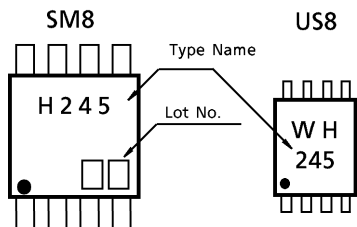
FEATURES

- High Speed $t_{pd} = 4.0ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Balanced Propagation Delays $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC} (opr) = 2 \sim 5.5V$
- Low Noise $V_{OLP} = 0.8V$ (Max.)

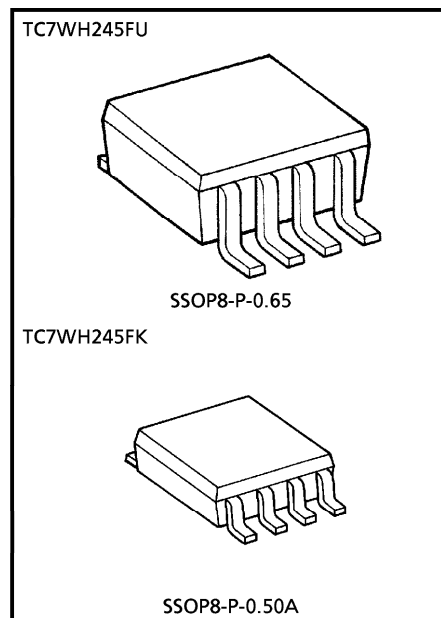
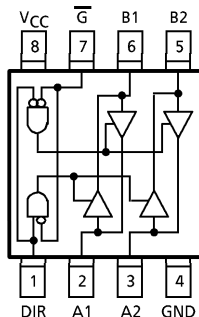
APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.
- 3) A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

MARKING



PIN ASSIGNMENT (TOP VIEW)



Weight
 SSOP8-P-0.65 : 0.02g (Typ.)
 SSOP8-P-0.50A : 0.01g (Typ.)

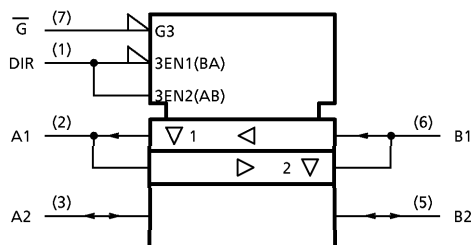
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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} + 0.5	V
Input Diode Current	I _{IJK}	-20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	300 (SM8)	mW
		200 (US8)	
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature (10 s)	T _L	260	°C

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
\bar{G}	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	x	High impedance		Z

x : Don't care
Z : High impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V _{CC} = 3.3 ± 0.3V)	ns / V
		0~20 (V _{CC} = 5 ± 0.5V)	

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- The information contained herein is subject to change without notice.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT		
					MIN.	TYP.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V		
				3.0~5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7	—			
Low-Level Input Voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V		
				3.0~5.5	—	—	V _{CC} × 0.3	—	V _{CC} × 0.3			
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}		I _{OH} = -50 μA		2.0	1.9	2.0	—	1.9	—	V
						3.0	2.9	3.0	—	2.9	—	
						4.5	4.4	4.5	—	4.4	—	
				I _{OH} = -4mA		3.0	2.58	—	—	2.48	—	
I _{OH} = -8mA		4.5	3.94			—	—	3.80	—			
		Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}		I _{OL} = 50 μA		2.0	—	0.0	0.1	—
3.0	—							0.0	0.1	—	0.1	
4.5	—							0.0	0.1	—	0.1	
I _{OL} = 4mA						3.0	—	—	0.36	—	0.44	
		I _{OL} = 8mA		4.5	—	—	0.36	—	0.44			
3-State Output Off-State Current	I _{OZ}			V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	2.0	—	20.0	μA		

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			VCC (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time	tpLH	RL = 1kΩ	3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	ns
				50	—	8.3	11.9	1.0	13.5	
	5.0 ± 0.5		15	—	4.0	5.5	1.0	6.5		
			50	—	5.5	7.5	1.0	8.5		
3-State Output Enable Time	tpZL	RL = 1kΩ	3.3 ± 0.3	15	—	8.5	13.2	1.0	15.5	ns
				50	—	11.0	16.7	1.0	19.0	
	5.0 ± 0.5		15	—	5.8	8.5	1.0	10.0		
			50	—	7.3	10.6	1.0	12.0		
3-State Output Disable Time	tpLZ	RL = 1kΩ	3.3 ± 0.3	50	—	11.5	15.8	1.0	18.0	ns
			5.0 ± 0.5	50	—	7.0	9.7	1.0	11.0	
Output to Output Skew	tosLH	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	CIN	DIR, \bar{G}	—	—	4	10	—	10	pF	
Bus Input Capacitance	CI/O	An, Bn	—	—	8	—	—	—	pF	
Power Dissipation Capacitance	CPD	(Note 2)	—	—	21	—	—	—	pF	

(Note 1) : Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

(Note 2) : CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

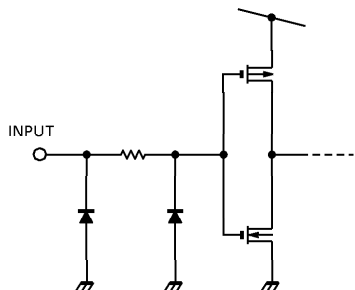
Average operating current can be obtained by the equation :

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Ta = 25°C, Input $t_r = t_f = 3ns$)

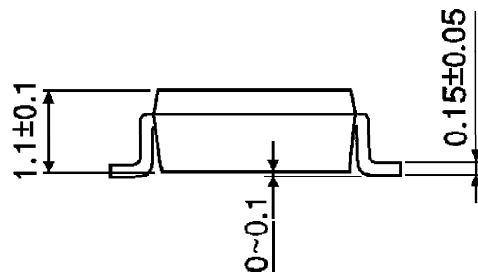
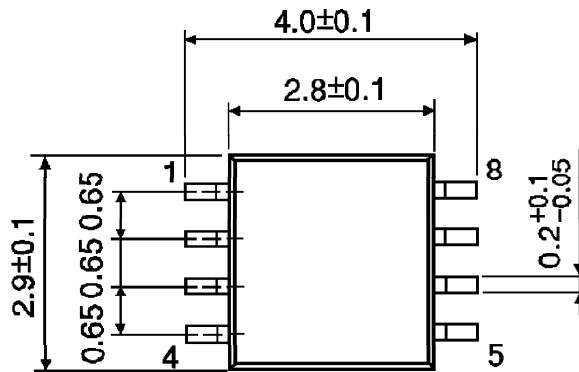
CHARACTERISTIC	SYMBOL	TEST CONDITION	VCC (V)	TYP.	IMIT	UNIT
			5.0			
Quiet Output Maximum Dynamic VOL	VOLP	CL = 50pF	5.0	0.5	0.8	V
Quiet Output Minimum Dynamic VOL	VOLV	CL = 50pF	5.0	-0.5	-0.8	V
Minimum High Level Dynamic Input Voltage	VIHD	CL = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	VILD	CL = 50pF	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SSOP8-P-0.65

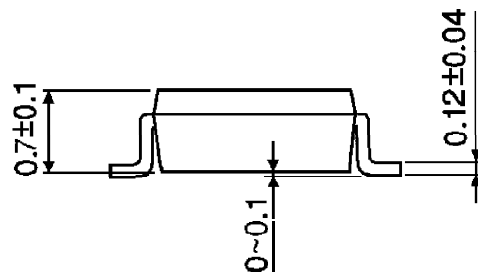
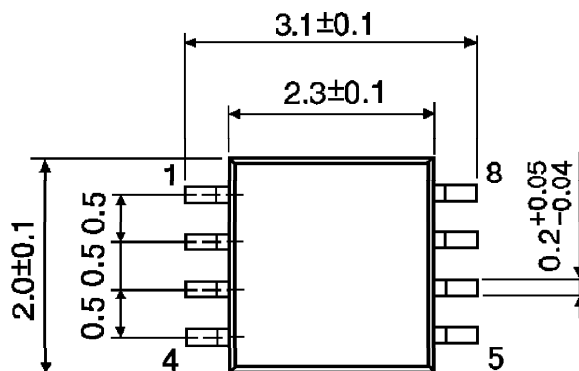
Unit : mm



Weight : 0.02g (Typ.)

OUTLINE DRAWING
SSOP8-P-0.50A

Unit : mm



Weight : 0.01g (Typ.)