Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE In-circuit Emulation, Debug Communication Channel Support
- 128 Kbytes of Internal High-speed Flash, Organized in 512 Pages of 256 Bytes
  - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
  - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
  - Page Programming Time: 4 ms, Including Page Auto-erase, Full Erase Time: 10 ms
  - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
  - Fast Flash Programming Interface for High Volume Production
- 32 Kbytes of Internal High-speed SRAM, Single-cycle Access at Maximum Speed
- Memory Controller (MC)
  - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
  - Based on Power-on Reset and Low-power Factory-calibrated Brown-out Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)
  - Software Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
  - Three Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- One Parallel Input/Output Controller (PIOA)
  - Thirty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Eleven Peripheral Data Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects

AT91 ARM® Thumb®-based Microcontrollers

AT91SAM7S128

Summary Preliminary

6116AS–ATARM–20-Oct-04

Note: This is a summary document. A complete document is not available at this time. For more information, please contact your local Atmel sales office.

- **One Three-channel 16-bit Timer/Counter (TC)**
  - **Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel**
  - **Double PWM Generation, Capture/Waveform Mode, Up/Down Capability**
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **One Two-wire Interface (TWI)**
  - **Master Mode Support Only, All Two-wire Atmel EEPROMs Supported**
- **One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os**
- **IEEE 1149.1 JTAG Boundary Scan on All Digital Pins**
- **5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each**
- **Power Supplies**
  - **Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components**
  - **3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply**
  - **1.8V VDDCORE Core Power Supply with Brown-out Detector**
- **Fully Static Operation: Up to 55 MHz at 1.65V and 85°C Worst Case Conditions**
- **Available in a 64-lead LQFP Package**

Description

Atmel's AT91SAM7S128 is a member of a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a 128 Kbyte high-speed Flash and a 32 Kbyte SRAM, a large set of peripherals, including a USB 2.0 device, and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The AT91SAM7S128 system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brown-out detector and a watchdog running off an integrated RC oscillator.

The AT91SAM7S128 is a general-purpose microcontroller. Its integrated USB Device port makes it an ideal device for peripheral applications requiring connectivity to a PC or cellular phone. Its aggressive price point and high level of integration pushes its scope of use far into the cost-sensitive, high-volume consumer market.

Block Diagram

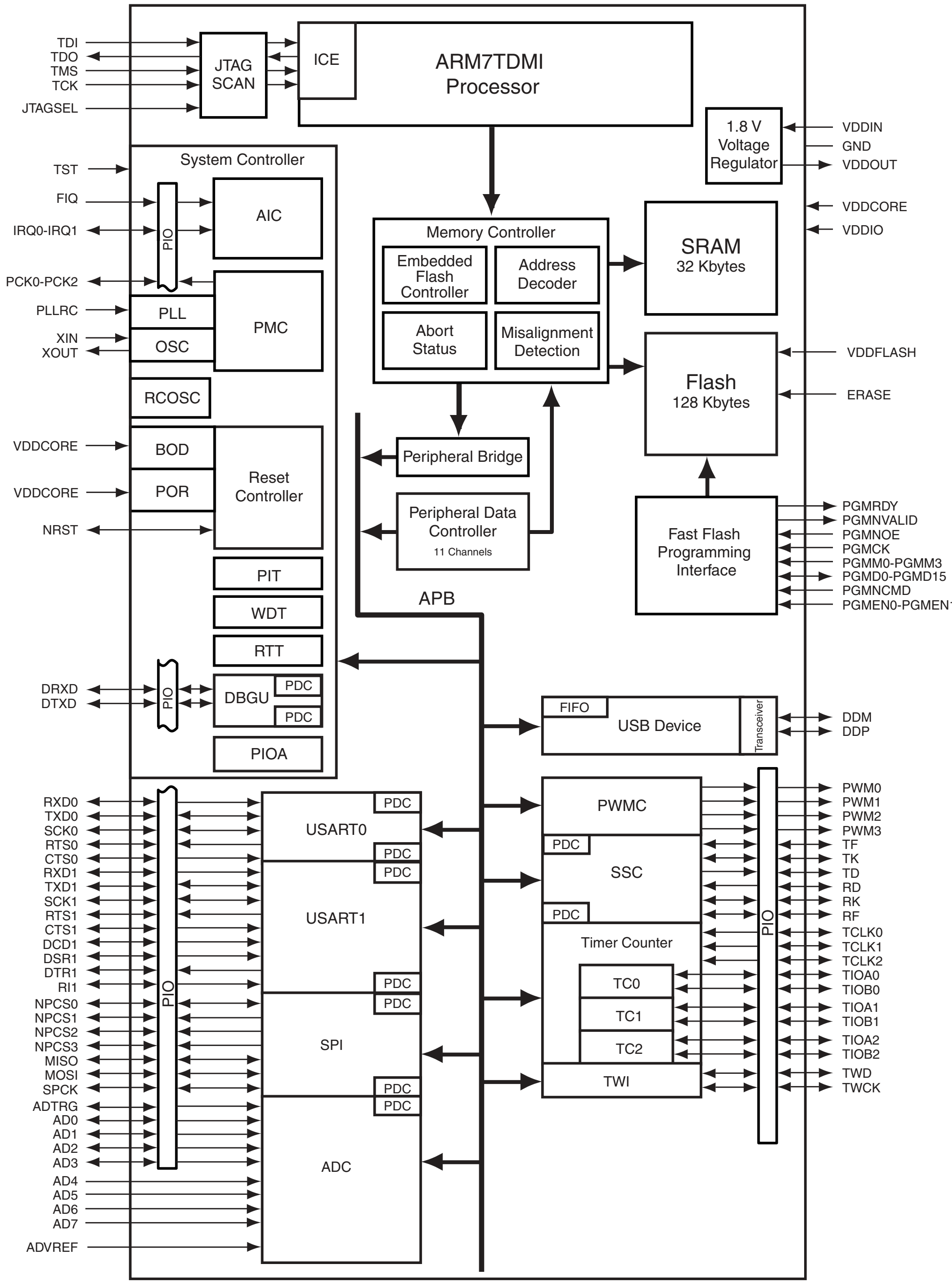


Figure 1. AT91SAM7S128 Block Diagram

Signal Description

Table 1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIN	Voltage Regulator Power Supply Input	Power		3.0V to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V nominal
VDDFLASH	Flash Power Supply	Power		3.0V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor
Flash Memory				
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-Up resistor
TST	Test Mode Select	Input		Pull-down resistor
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		

Table 1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
PIO				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USART				
SCK0 - SCK1	Serial Clock	I/O		
TXD0 - TXD1	Transmit Data	I/O		
RXD0 - RXD1	Receive Data	Input		
RTS0 - RTS1	Request To Send	Output		
CTS0 - CTS1	Clear To Send	Input		
DCD1	Data Carrier Detect	Input		
DTR1	Data Terminal Ready	Output		
DSR1	Data Set Ready	Input		
RI1	Ring Indicator	Input		
Synchronous Serial Controller				
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK2	External Clock Inputs	Input		
TIOA0 - TIOA2	I/O Line A	I/O		
TIOB0 - TIOB2	I/O Line B	I/O		
PWM Controller				
PWM0 - PWM3	PWM Channels	Output		
SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	

Table 1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
Analog-to-Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
Fast Flash Programming Interface				
PGMEN0-PGMEN1	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	

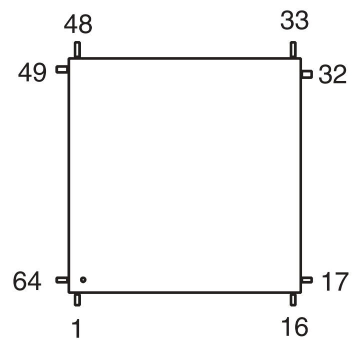
Package and Pinout

The AT91SAM7S128 is available in a 64-lead LQFP package.

64-lead LQFP Mechanical Overview

Figure 2 shows the orientation of the 64-lead LQFP package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 2. 64-lead LQFP Package Pinout (Top View)



Pinout

Table 2. AT91SAM7S128 Pinout in 64-lead LQFP Package

1	ADVREF	17	GND	33	TDI	49	TDO
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS
4	AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK
6	AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE
8	VDDOUT	24	VDDCORE	40	TST	56	DDM
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9	27	PA12/PGMD0	43	PA3	59	VDDFLASH
12	VDDCORE	28	PA11/PGMM3	44	PA2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT
14	PA22/PGMD10	30	PA9/PGMM1	46	GND	62	XIN/PGMCK
15	PA23/PGMD11	31	PA8/PGMM0	47	PA1/PGMEN1	63	PLLRC
16	PA20/PGMD8/AD3	32	PA7/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Power Considerations

Power Supplies

The AT91SAM7S128 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator; voltage ranges from 3.0V to 3.6V, 3.3V nominal. If the voltage regulator is not used, VDDIN should be connected to GND.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines and the USB transceivers; dual voltage range is supported. Ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDFLASH pin. It powers a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

Power Consumption

The AT91SAM7S128 has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brown-out detector is deactivated. Activating the brown-out detector adds 20 µA static current.

The dynamic power consumption on VDDCORE is less than 50 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

Voltage Regulator

The AT91SAM7S128 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 20 µA static current and draws 1 mA of output current.

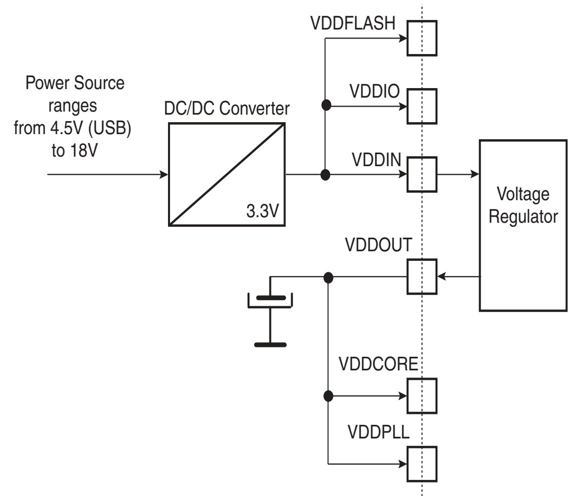
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor must be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 µF (or 3.3 µF) X7R capacitor must be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

Typical Powering Schematics

The AT91SAM7S128 supports a 3.3V single supply mode. The internal regulator is connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 3 shows the power schematics to be used for USB bus-powered systems.

Figure 3. 3.3V System Single Power Supply Schematic



I/O Lines Considerations

JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS and TCK are 5-V tolerant, TDI is not. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The pin JTAGSEL is used to select the JTAG boundary scan when asserted at a high level. The pin JTAGSEL integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

Test Pin

The pin TST is used for manufacturing test or fast programming mode of the AT91SAM7S128 when asserted high. The pin TST integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the pin TST and the pins PA0 and PA1 should be tied high.

Driving the pin TST at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

Reset Pin

The pin NRST is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the pin NRST as system user reset, and the use of the signal NRST to reset all the components of the system.

The pin NRST integrates a permanent pull-up resistor to VDDIO.

ERASE Pin

The pin ERASE is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

PIO Controller A Lines

All the I/O lines PA0 to PA31 are 5V-tolerant and all integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled can lead to unpredictable results. Care should be taken, in particular at reset, as all the I/O lines default to input with pull-up resistor enabled at reset.

I/O Line Drive Levels

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 150 mA.

Processor and Architecture

ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

Debug and Test Features

- Integrated embedded in-circuit emulator
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

Memory Controller

- Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral Data Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states
  - Prefetch buffer, bufferizing and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

Peripheral Data Controller

- Handles data transfer between peripherals and memories
- Eleven channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Synchronous Controller
  - Two for the Serial Peripheral Interface
  - One for the Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements

Memory

- 128 Kbytes of Flash Memory
  - 512 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in worst case conditions
  - Page programming time: 4 ms, including page auto-erase
  - Page programming without auto-erase: 2 ms
  - Full chip erase time: 10 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, each protecting 8 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
  - Single-cycle access at full speed

Memory Mapping

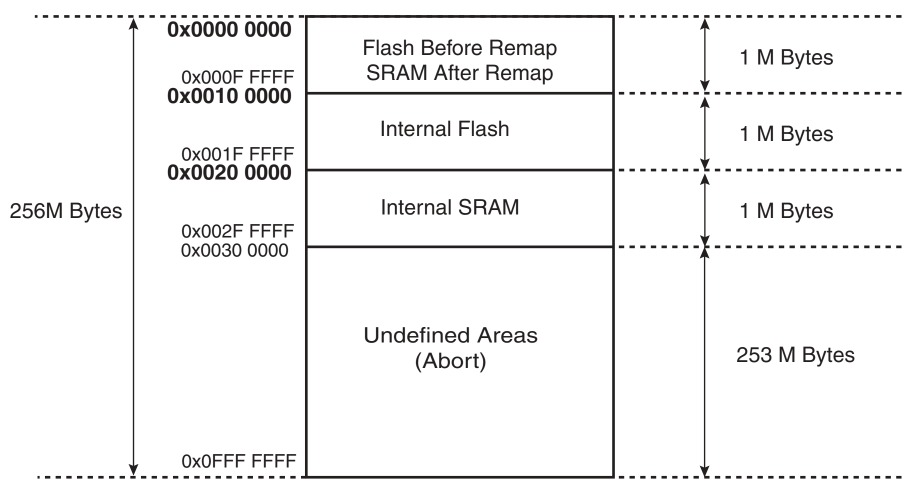
Internal SRAM

The AT91SAM7S128 embeds a high-speed 32-Kbyte SRAM bank. After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

Internal Flash

The AT91SAM7S128 features one bank of 128 Kbytes of Flash. At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Figure 4. Internal Memory Mapping



Embedded Flash

Flash Overview

The Flash of the AT91SAM7S128 is organized in 512 pages of 256 bytes. It reads as 32,768 32-bit words.

The Flash contains a 256-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

Embedded Flash Controller

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

Lock Regions

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-regions erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Security Bit Feature

The AT91SAM7S128 features a security bit, based on a specific NVM-Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command "Set Security Bit" of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands "Clear General-purpose NVM Bit" and "Set General-purpose NVM Bit" of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

Calibration Bits

Eight NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

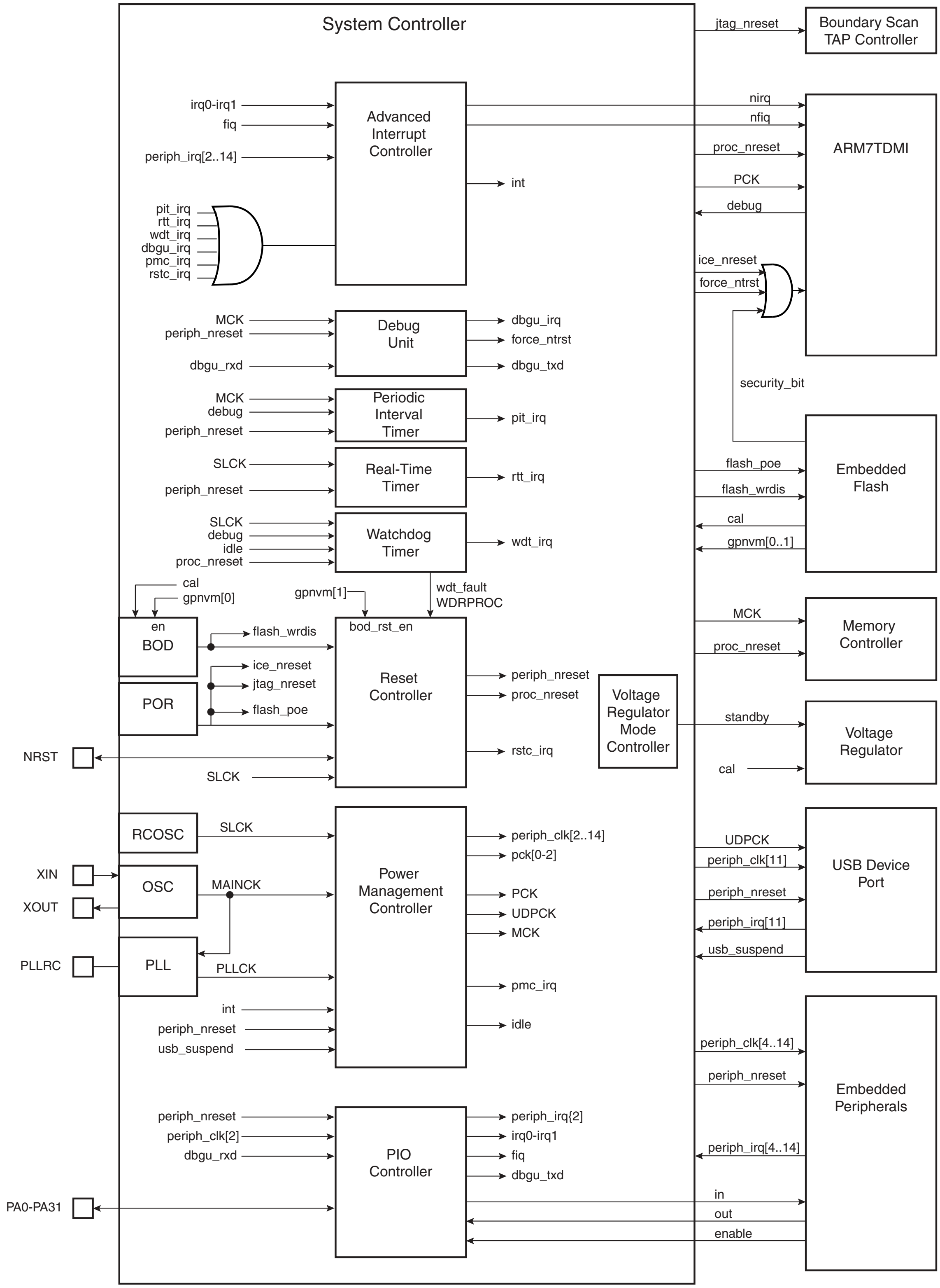
The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high.

System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

Figure 5. System Controller Block Diagram



System Controller Mapping

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 6 shows the mapping of the System Controller. Note that the Memory Controller configuration user interface is also mapped within this address space.

Figure 6. System Controller Mapping

Address	Peripheral	Peripheral Name	Size
0xFFFF F000 – 0xFFFF F1FF	AIC	Advanced Interrupt Controller	512 Bytes/128 registers
0xFFFF F200 – 0xFFFF F3FF	DBGU	Debug Unit	512 Bytes/128 registers
0xFFFF F400 – 0xFFFF F5FF	PIOA	PIO Controller A	512 Bytes/128 registers
0xFFFF F600 – 0xFFFF FBFF	Reserved		
0xFFFF FC00 – 0xFFFF FCFF	PMC	Power Management Controller	256 Bytes/64 registers
0xFFFF FD00 – 0xFFFF FD0F	RSTC	Reset Controller	16 Bytes/4 registers
	Reserved		
0xFFFF FD20 – 0xFFFF FC2F	RTT	Real-time Timer	16 Bytes/4 registers
0xFFFF FD30 – 0xFFFF FC3F	PIT	Periodic Interval Timer	16 Bytes/4 registers
0xFFFF FD40 – 0xFFFF FD4F	WDT	Watchdog Timer	16 Bytes/4 registers
	Reserved		
0xFFFF FD60 – 0xFFFF FC6F	VREG	Voltage Regulator Mode Controller	4 Bytes/1 register
0xFFFF FD70 – 0xFFFF FEFF	Reserved		
0xFFFF FF00 – 0xFFFF FFFF	MC	Memory Controller	256 Bytes/64 registers

Reset Controller

The Reset Controller is based on a power-on reset cell and one brownout detector. It gives the status of the last reset, indicating whether it is a power-up reset, a software reset, a user reset, a watchdog reset or a brownout reset. In addition, it controls the internal resets and the NRST pin output. It allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

Brownout Detector and Power-on Reset

The AT91SAM7S128 embeds a brownout detection circuit and a power-on reset cell. Both are supplied with and monitor VDDCORE. Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE level during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE.

Only VDDCORE is monitored, as a voltage drop on VDDFLASH or any other power supply of the device cannot affect the Flash.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot-, defined as Vbot - hyst/2), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (Vbot+, defined as Vbot + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of ± 2% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 20 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1µA. The deactivation is configured through the GPNVM bit 0 of the Flash.

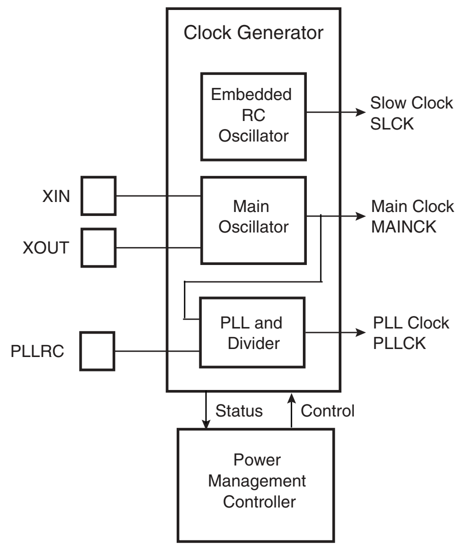
Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 KHz and 42 KHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 200 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 7. Clock Generator Block Diagram



Power Management Controller

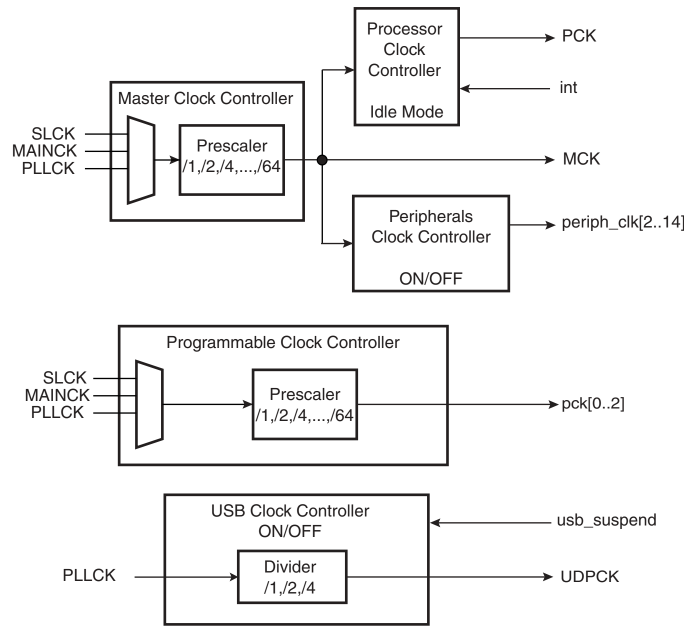
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 8. Power Management Controller Block Diagram



Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt of the processor
  - Handles priority of the interrupt sources
  - Higher priority interrupts can be served during service of lower priority interrupt

- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support
  - One set of Chip ID Registers
  - One Interface providing ICE Access Prevention
- Two-pin UART
  - Implemented features are compatible with the USART
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x270c0740 (VERSION 0)

Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SLCK accuracy compensation

PIO Controller

- One PIO Controller, controlling 32 I/O lines
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain

- Programmable pull-up on each I/O line
- Pin data status register, supplies visibility of the level on the pin at any time

- Synchronous output, provides Set and Clear of several I/O lines in a single write

Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

Peripherals

Peripheral Mapping

Each peripheral is allocated 16 Kbytes of address space.

Figure 9. User Peripheral Mapping

Start Address	End Address	Peripheral	Peripheral Name	Size
0xF000 0000	0xFFF9 FFFF	Reserved		
0xFFFA 0000	0xFFFA 3FFF	TC0, TC1, TC2	Timer/Counter 0, 1 and 2	16 Kbytes
0xFFFA 4000	0xFFFA FFFF	Reserved		
0xFFFB 0000	0xFFFB 3FFF	UDP	USB Device Port	16 Kbytes
0xFFFB 4000	0xFFFB 7FFF	Reserved		
0xFFFB 8000	0xFFFB BFFF	TWI	Two-Wire Interface	16 Kbytes
0xFFFB C000	0xFFFB FFFF	Reserved		
0xFFFC 0000	0xFFFC 3FFF	USART0	Universal Synchronous Asynchronous Receiver Transmitter 0	16 Kbytes
0xFFFC 4000	0xFFFC 7FFF	USART1	Universal Synchronous Asynchronous Receiver Transmitter 1	16 Kbytes
0xFFFC 8000	0xFFFC BFFF	Reserved		
0xFFFC C000	0xFFFC FFFF	PWMC	PWM Controller	16 Kbytes
0xFFFD 0000	0xFFFD 3FFF	Reserved		
0xFFFD 4000	0xFFFD 7FFF	SSC	Serial Synchronous Controller	16 Kbytes
0xFFFD 8000	0xFFFD BFFF	ADC	Analog-to-Digital Converter	16 Kbytes
0xFFFD C000	0xFFFD FFFF	Reserved		
0xFFFE 0000	0xFFFE 3FFF	SPI	Serial Peripheral Interface	16 Kbytes
0xFFFE 4000	0xFFFE FFFF	Reserved		

Peripheral Multiplexing on PIO Lines

The AT91SAM7S128 features one PIO controller, PIOA, that multiplexes the I/O lines of the peripheral set.

PIO Controller A controls 32 lines. Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

Table 3 on page 25 defines how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only may be duplicated in the table.

All pins reset in their Parallel I/O lines function are configured in input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

PIO Controller A Multiplexing

Table 3. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Function**	**Comments**
PA0	PWM0	TIOA0	High-Drive		
PA1	PWM1	TIOB0	High-Drive		
PA2	PWM2	SCK0	High-Drive		
PA3	TWD	NPCS3	High-Drive		
PA4	TWCK	TCLK0			
PA5	RXD0	NPCS3			
PA6	TXD0	PCK0			
PA7	RTS0	PWM3			
PA8	CTS0	ADTRG			
PA9	DRXD	NPCS1			
PA10	DTXD	NPCS2			
PA11	NPCS0	PWM0			
PA12	MISO	PWM1			
PA13	MOSI	PWM2			
PA14	SPCK	PWM3			
PA15	TF	TIOA1			
PA16	TK	TIOB1			
PA17	TD	PCK1	AD0		
PA18	RD	PCK2	AD1		
PA19	RK	FIQ	AD2		
PA20	RF	IRQ0	AD3		
PA21	RXD1	PCK1			
PA22	TXD1	NPCS3			
PA23	SCK1	PWM0			
PA24	RTS1	PWM1			
PA25	CTS1	PWM2			
PA26	DCD1	TIOA2			
PA27	DTR1	TIOB2			
PA28	DSR1	TCLK1			
PA29	RI1	TCLK2			
PA30	IRQ1	NPCS2			
PA31	NPCS1	PCK2			

Peripheral Identifiers

The AT91SAM7S128 embeds a wide range of peripherals. Table 4 defines the Peripheral Identifiers of the AT91SAM7S128. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 4. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSIRQ(1)	System Interrupt	
2	PIOA	Parallel I/O Controller A	
3	Reserved		
4	ADC(1)	Analog-to Digital Converter	
5	SPI	Serial Peripheral Interface	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15 - 29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSIRQ and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped aftere ach conversion.

Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers

- Selectable mode fault detection
- Maximum frequency at up to Master Clock

Two-wire Interface

- Master Mode only
- Compatibility with standard two-wire serial memories
- One, two or three bytes for slave address
- Sequential read/write operations

USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

Timer Counter

- Three 16-bit Timer Counter Channels
  - Three output compare or two input capture
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement

– Pulse generation
– Delay timing
– Pulse Width Modulation
– Up/down capabilities
- Each channel is user-configurable and contains:
  – Three external clock inputs
  – Five internal clock inputs, as defined in Table 5

Table 5. Timer Counter Clocks Assignment

TC Clock Input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  – Two multi-purpose input/output signals
  – Two global registers that act on all three TC channels

PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  – One Modulo n counter providing eleven clocks
  – Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  – Independent enable/disable commands
  – Independent clock selection
  – Independent period and duty cycle, with double bufferization
  – Programmable selection of the output waveform polarity
  – Programmable center or left aligned output waveform

USB Device Port

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 328-byte dual-port RAM for endpoints
- Four endpoints
  – Endpoint 0: 8 bytes
  – Endpoint 1 and 2: 64 bytes ping-pong
  – Endpoint 3: 64 bytes
  – Ping-pong Mode (two memory banks) for bulk endpoints
- Suspend/resume logic

Analog-to-digital Converter

- 8-channel ADC
- 10-bit 100 Ksamples/sec. Successive Approximation Register ADC
- -2/+2 LSB Integral Non Linearity, -1/+2 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs

- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

Ordering Information

Table 6. Ordering Information

Ordering Code	Package	Temperature Operating Range
AT91SAM7S128-AI	LQFP 64	Industrial (-40°C to 85°C)

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