## ADG821/ADG822/ADG823

## FEATURES

$0.8 \Omega$ Max On Resistance @ $125^{\circ} \mathrm{C}$
$0.28 \Omega$ Max On Resistance Flatness @ $125^{\circ} \mathrm{C}$
1.8 V to 5.5 V Single Supply

200 mA Current Carrying Capability
Automotive Temperature Range: $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Rail-to-Rail Operation
8-Lead MSOP Package
33 ns Switching Times
Typical Power Consumption ( $<0.01 \mu \mathrm{~W}$ )
TTL/CMOS Compatible Inputs
Pin Compatible with ADG721/722/723

## APPLICATIONS

Power Routing
Battery-Powered Systems
Communication Systems
Data Acquisition Systems
Audio and Video Signal Routing
Cellular Phones
Modems
PCMCIA Cards
Hard Drives
Relay Replacement

## GENERAL DESCRIPTION

The ADG821, ADG822, and ADG823 are monolithic CMOS SPST (single pole, single throw) switches. These switches are designed on an advanced submicron process that provides low power dissipation, yet gives high switching speed, low on resistance, and low leakage currents.

The ADG821, ADG822, and ADG823 are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments.

Each switch of the ADG821/ADG822/ADG823 conducts equally well in both directions when on. The ADG821, ADG822, and ADG823 contain two independent SPST switches. The ADG821 and ADG822 differ only in that both switches are normally open and normally closed, respectively. In the ADG823, Switch 1 is normally open and Switch 2 is normally closed. The ADG823 exhibits break-before-make switching action.

The ADG821, ADG822, and ADG823 are available in an 8-lead MSOP package.

REV. 0

## FUNCTIONAL BLOCK DIAGRAM




SWITCHES SHOWN FOR A LOGIC " 0 " INPUT

## PRODUCT HIGHLIGHTS

1. Very Low On Resistance ( $0.5 \Omega$ typ)
2. On Resistance Flatness ( $\mathrm{R}_{\mathrm{FLAT}(\mathrm{ON})}$ ) (0.15 $\Omega$ typ)
3. Automotive Temperature Range $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
4. 200 mA Current Carrying Capability
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. 8-Lead MSOP Package

## ADG821/ADG822/ADG823-SPEG|FIGATIONS $\begin{gathered}1\left(\mathrm{v}_{\mathrm{DD}}=5 \mathrm{~V} \pm 10 \%, \text { GND }=0 \mathrm{~V} . \text { All specifications }\right. \\ \left.-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}, \text { unless otherwise noted. }\right)\end{gathered}$

| Parameter | $25^{\circ} \mathrm{C}$ | $\begin{aligned} & -40^{\circ} \mathrm{C} \text { to } \\ & +85^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & -40^{\circ} \mathrm{C} \text { to } \\ & +125^{\circ} \mathrm{C}^{2} \end{aligned}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH <br> Analog Signal Range On Resistance ( $\mathrm{R}_{\mathrm{ON}}$ ) <br> On Resistance Match Between Channels ( $\Delta \mathrm{R}_{\mathrm{ON}}$ ) <br> On Resistance Flatness ( $\mathrm{R}_{\mathrm{FLAT}(\mathrm{ON})}$ ) | $\begin{aligned} & 0.5 \\ & 0.6 \\ & \\ & 0.16 \\ & 0.2 \\ & 0.15 \\ & 0.23 \end{aligned}$ | $\begin{aligned} & 0.7 \\ & 0.25 \\ & 0.26 \end{aligned}$ | $\begin{aligned} & 0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}} \\ & 0.8 \\ & 0.28 \\ & 0.3 \end{aligned}$ | V <br> $\Omega$ typ <br> $\Omega$ max <br> $\Omega$ typ <br> $\Omega$ max <br> $\Omega$ typ <br> $\Omega$ max | $\mathrm{V}_{\mathrm{S}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}}, \mathrm{I}_{\mathrm{S}}=100 \mathrm{~mA} ;$ <br> Test Circuit 1 $\begin{aligned} & \mathrm{V}_{\mathrm{S}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}}, \mathrm{I}_{\mathrm{S}}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{S}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}}, \mathrm{I}_{\mathrm{S}}=100 \mathrm{~mA} \end{aligned}$ |
| LEAKAGE CURRENTS <br> Source OFF Leakage IS (OFF) <br> Drain OFF Leakage $\mathrm{I}_{\mathrm{D}}(\mathrm{OFF})$ <br> Channel ON Leakage $\mathrm{I}_{\mathrm{D}}, \mathrm{I}_{\mathrm{S}}(\mathrm{ON})$ | $\begin{aligned} & \pm 0.01 \\ & \pm 0.25 \\ & \pm 0.01 \\ & \pm 0.25 \\ & \pm 0.01 \\ & \pm 0.25 \end{aligned}$ | $\begin{aligned} & \pm 3 \\ & \pm 3 \\ & \pm 3 \end{aligned}$ | $\begin{aligned} & \pm 25 \\ & \pm 25 \\ & \pm 25 \end{aligned}$ | nA typ <br> nA max <br> nA typ <br> nA max <br> nA typ <br> nA max | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{S}}=4.5 \mathrm{~V} / 1 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=1 \mathrm{~V} / 4.5 \mathrm{~V} ; \end{aligned}$ <br> Test Circuit 2 $\mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V} / 1 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=1 \mathrm{~V} / 4.5 \mathrm{~V} \text {; }$ <br> Test Circuit 2 $\mathrm{V}_{\mathrm{S}}=\mathrm{V}_{\mathrm{D}}=1 \mathrm{~V} \text {, or } \mathrm{V}_{\mathrm{S}}=\mathrm{V}_{\mathrm{D}}=4.5 \mathrm{~V} \text {; }$ <br> Test Circuit 3 |
| DIGITAL INPUTS <br> Input High Voltage, $\mathrm{V}_{\text {INH }}$ Input Low Voltage, $\mathrm{V}_{\text {INL }}$ Input Current $\mathrm{I}_{\text {INL }}$ or $\mathrm{I}_{\text {INH }}$ <br> $\mathrm{C}_{\mathrm{IN}}$, Digital Input Capacitance | $\begin{aligned} & 0.005 \\ & 4 \end{aligned}$ |  | $\begin{gathered} 2.0 \\ 0.8 \\ \\ \pm 0.1 \end{gathered}$ | V min <br> V max <br> $\mu \mathrm{A}$ typ <br> $\mu \mathrm{A}$ max <br> pF typ | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {INL }}$ or $\mathrm{V}_{\text {INH }}$ |
| DYNAMIC CHARACTERISTICS ${ }^{3}$ <br> $\mathrm{t}_{\mathrm{ON}}$ <br> $\mathrm{t}_{\mathrm{OFF}}$ <br> Break-Before-Make Time Delay, $\mathrm{t}_{\text {BBM }}$ (ADG823 Only) <br> Charge Injection <br> Off Isolation <br> Channel-to-Channel Crosstalk <br> Bandwidth -3 dB <br> $\mathrm{C}_{\mathrm{S}}$ (OFF) <br> $\mathrm{C}_{\mathrm{D}}$ (OFF) <br> $\mathrm{C}_{\mathrm{D}}, \mathrm{C}_{\mathrm{S}}(\mathrm{ON})$ | 33 <br> 45 <br> 11 <br> 16 <br> 32 <br> 15 <br> $-52$ <br> $-82$ <br> 24 <br> 85 <br> 98 <br> 230 | $\begin{aligned} & 48 \\ & 19 \end{aligned}$ | 52 21 | ns typ <br> ns max <br> ns typ <br> ns max <br> ns typ <br> ns min <br> pC typ <br> dB typ <br> dB typ <br> MHz typ <br> pF typ <br> pF typ <br> pF typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{S}}=3 \mathrm{~V} ; \text { Test Circuit } 4 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{S}}=3 \mathrm{~V} ; \text { Test Circuit } 4 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{S} 1}=\mathrm{V}_{\mathrm{S} 2}=3 \mathrm{~V} ; \text { Test Circuit } 5 \\ & \mathrm{~V}_{\mathrm{S}}=2.5 \mathrm{~V} ; \mathrm{R}_{\mathrm{S}}=0 \Omega, \mathrm{C}_{\mathrm{L}}=1 \mathrm{nF} ; \\ & \text { Test Circuit } 6 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & \mathrm{f}=1 \mathrm{MHz} ; \text { Test Circuit } 7^{\mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}} \\ & \mathrm{f}=1 \mathrm{MHzz} \text { Test Circuit } 9 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} ; \\ & \mathrm{Test} \mathrm{Circuit} 8 \\ & \mathrm{f}=1 \mathrm{MHz} \\ & \mathrm{f}=1 \mathrm{MHz} \\ & \mathrm{f}=1 \mathrm{MHz} \end{aligned}$ |
| POWER REQUIREMENTS $\mathrm{I}_{\mathrm{DD}}$ | 0.001 | 1.0 | 2.0 | $\mu \mathrm{A}$ typ <br> $\mu \mathrm{A} \max$ | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=5.5 \mathrm{~V} \\ & \text { Digital Inputs }=0 \mathrm{~V} \text { or } 5.5 \mathrm{~V} \end{aligned}$ |

## NOTES

${ }^{1}$ Temperature range: Automotive range: $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
${ }^{2} \mathrm{On}$ resistance parameters tested with $\mathrm{I}_{\mathrm{S}}=10 \mathrm{~mA}$.
${ }^{3}$ Guaranteed by design, not subject to production test.
Specifications subject to change without notice.
$\left(\mathrm{V}_{D D}=2.7 \mathrm{~V} \text { to 3.6 } \mathrm{V}, \mathrm{GND}=0 \mathrm{~V} \text {. All specifications }-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \text {, unless otherwise noted. }\right)^{1}$

| Parameter | $25^{\circ} \mathrm{C}$ | $\begin{aligned} & -40^{\circ} \mathrm{C} \text { to } \\ & +85^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & -40^{\circ} \mathrm{C} \text { to } \\ & +125^{\circ} \mathrm{C}^{2} \end{aligned}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH <br> Analog Signal Range On Resistance ( $\mathrm{R}_{\mathrm{ON}}$ ) <br> On Resistance Match Between Channels ( $\Delta \mathrm{R}_{\mathrm{ON}}$ ) <br> On Resistance Flatness ( $\mathrm{R}_{\text {FLAT(ON) }}$ ) | $\begin{aligned} & 0.7 \\ & 1.4 \\ & 0.16 \\ & 0.2 \\ & 0.3 \end{aligned}$ | 1.5 0.25 | $\begin{aligned} & 0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}} \\ & 1.6 \\ & 0.28 \\ & 0.33 \end{aligned}$ | V <br> $\Omega$ typ <br> $\Omega$ max <br> $\Omega$ typ <br> $\Omega$ max <br> $\Omega$ typ | $\mathrm{V}_{\mathrm{S}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}}, \mathrm{I}_{\mathrm{S}}=100 \mathrm{~mA} ;$ <br> Test Circuit 1 $\begin{aligned} & \mathrm{V}_{\mathrm{S}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}}, \mathrm{I}_{\mathrm{S}}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{S}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{DD}}, \mathrm{I}_{\mathrm{S}}=100 \mathrm{~mA} \end{aligned}$ |
| LEAKAGE CURRENTS <br> Source OFF Leakage IS (OFF) <br> Drain OFF Leakage $\mathrm{I}_{\mathrm{D}}$ (OFF) <br> Channel ON Leakage $\mathrm{I}_{\mathrm{D}}, \mathrm{I}_{\mathrm{S}}(\mathrm{ON})$ | $\begin{aligned} & \pm 0.01 \\ & \pm 0.25 \\ & \pm 0.01 \\ & \pm 0.25 \\ & \pm 0.01 \\ & \pm 0.25 \end{aligned}$ | $\begin{aligned} & \pm 3 \\ & \pm 3 \\ & \pm 3 \end{aligned}$ | $\begin{aligned} & \pm 15 \\ & \pm 25 \\ & \pm 25 \end{aligned}$ | nA typ <br> nA max <br> nA typ <br> nA max <br> nA typ <br> nA max | $\begin{aligned} & \mathrm{V} \mathrm{VD}=3.6 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{S}}=3.3 \mathrm{~V} / 1 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=1 \mathrm{~V} / 3.3 \mathrm{~V} ; \end{aligned}$ <br> Test Circuit 2 $\mathrm{V}_{\mathrm{S}}=3.3 \mathrm{~V} / 1 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=1 \mathrm{~V} / 3.3 \mathrm{~V} \text {; }$ <br> Test Circuit 2 $\mathrm{V}_{\mathrm{S}}=\mathrm{V}_{\mathrm{D}}=1 \mathrm{~V} \text {, or } 3.3 \mathrm{~V} \text {; }$ <br> Test Circuit 3 |
| DIGITAL INPUTS <br> Input High Voltage, $\mathrm{V}_{\text {INH }}$ Input Low Voltage, $\mathrm{V}_{\text {INL }}$ Input Current $\mathrm{I}_{\text {INL }}$ or $\mathrm{I}_{\text {INH }}$ <br> $\mathrm{C}_{\mathrm{IN}}$, Digital Input Capacitance | $\begin{aligned} & 0.005 \\ & 4 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 0.8 \\ & \\ & \pm 0.1 \end{aligned}$ | V min <br> V max <br> $\mu \mathrm{A}$ typ <br> $\mu \mathrm{A}$ max <br> pF typ | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {INL }}$ or $\mathrm{V}_{\text {INH }}$ |
| ```DYNAMIC CHARACTERISTICS \({ }^{3}\) \(\mathrm{t}_{\mathrm{ON}}\) \(\mathrm{t}_{\mathrm{OFF}}\) Break-Before-Make Time Delay, tBвм (ADG823 Only) Charge Injection Off Isolation Channel-to-Channel Crosstalk Bandwidth - 3 dB \(\mathrm{C}_{\mathrm{S}}\) (OFF) \(\mathrm{C}_{\mathrm{D}}\) (OFF) \(\mathrm{C}_{\mathrm{D}}, \mathrm{C}_{\mathrm{S}}(\mathrm{ON})\)``` | $\begin{aligned} & 48 \\ & 67 \\ & 12 \\ & 18 \\ & 40 \\ & \pm 2 \\ & -52 \\ & -82 \\ & -82 \\ & 24 \\ & \\ & 85 \\ & 98 \\ & 230 \end{aligned}$ | 74 20 | 78 23 | ns typ <br> ns max <br> ns typ <br> ns max <br> ns typ <br> ns min <br> pC typ <br> dB typ <br> dB typ <br> MHz typ <br> pF typ <br> pF typ <br> pF typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{S}}=1.5 \mathrm{~V} ; \mathrm{Test}^{2} \text { Circuit } 4 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{S}}=1.5 \mathrm{~V} ; \text { Test Circuit } 4 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{S} 1}=\mathrm{V}_{\mathrm{S} 2}=1.5 \mathrm{~V} ; \text { Test Circuit } 5 \\ & \mathrm{~V}_{\mathrm{S}}=1.5 \mathrm{~V} ; \mathrm{R}_{\mathrm{S}}=0 \Omega, \mathrm{C}_{\mathrm{L}}=1 \mathrm{nF} ; \\ & \text { Test Circuit } 6 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & \mathrm{f}=1 \mathrm{MHz} ; \mathrm{Test} \mathrm{Circuit} 7 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \\ & \mathrm{f}=1 \mathrm{MHz} ; \text { Test Circuit } 9 \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} ; \\ & \text { Test Circuit } 8 \\ & \mathrm{f}=1 \mathrm{MHz} \\ & \mathrm{f}=1 \mathrm{MHz} \\ & \mathrm{f}=1 \mathrm{MHz} \\ & \hline \end{aligned}$ |
| POWER REQUIREMENTS $\mathrm{I}_{\mathrm{DD}}$ | 0.001 | 1.0 | 2.0 | $\mu \mathrm{A}$ typ <br> $\mu \mathrm{A}$ max | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=3.6 \mathrm{~V} \\ & \text { Digital Inputs }=0 \mathrm{~V} \text { or } 3.6 \mathrm{~V} \end{aligned}$ |

NOTES
${ }^{1}$ Temperature range: Automotive range: $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
${ }^{2} \mathrm{On}$ resistance parameters tested with $\mathrm{I}_{\mathrm{S}}=10 \mathrm{~mA}$.
${ }^{3}$ Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

## ADG821/ADG822/ADG823

## ABSOLUTE MAXIMUM RATINGS ${ }^{1}$

( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)
$\mathrm{V}_{\mathrm{DD}}$ to GND . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3 V to +7 V
Analog Inputs ${ }^{2} \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots .0 .3 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{DD}}+0.3 \mathrm{~V}$ or 30 mA , Whichever Occurs First
 30 mA , Whichever Occurs First
Peak Current, S or D (Pulsed at $1 \mathrm{~ms}, 10 \%$ Duty Cycle max)
Continuous Current, S or D . . . . . . . . . . . . . . . . . . . 200 mA
Operating Temperature Range
Automotive . . . . . . . . . . . . . . . . . . . . . . . . $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage Temperature Range . . . . . . . . . . . . $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Junction Temperature ( $\mathrm{T}_{\mathrm{i}}$ max) . . . . . . . . . . . . . . . . . . . . $150^{\circ} \mathrm{C}$
Package Power Dissipation $\ldots \ldots . . . . . . .\left(T_{j} \max -T_{A}\right) / \theta_{\mathrm{JA}}$
8-Lead MSOP Package
$\theta_{\mathrm{JA}}$ Thermal Impedance . . . . . . . . . . . . . . . . . . . . . . $206^{\circ} \mathrm{C} / \mathrm{W}$
$\theta_{\mathrm{JC}}$ Thermal Impedance . . . . . . . . . . . . . . . . . . . . . $44^{\circ} \mathrm{C} / \mathrm{W}$
Lead Temperature, Soldering (10 sec) . . . . . . . . . . . . . $300^{\circ} \mathrm{C}$
IR Reflow, Peak Temperature (<20 sec) . . . . . . . . . . . . $235^{\circ} \mathrm{C}$

## NOTES

${ }^{1}$ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
${ }^{2}$ Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table for the ADG821/ADG822

| ADG821 INx | ADG822 INx | Switch $\mathbf{x}$ Condition |
| :--- | :--- | :--- |
| 0 | 1 | OFF |
| 1 | 0 | ON |

Table II. Truth Table for the ADG823

| IN1 | IN2 | Switch S1 | Switch S2 |
| :--- | :--- | :--- | :--- |
| 0 | 0 | OFF | ON |
| 0 | 1 | OFF | OFF |
| 1 | 0 | ON | ON |
| 1 | 1 | ON | OFF |

ORDERING GUIDE

| Model Option | Temperature Range | Brand $^{*}$ | Package Description | Package |
| :--- | :--- | :--- | :--- | :--- |
| ADG821BRM | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | SQB | MSOP (microSmall Outline IC) | RM-8 |
| ADG822BRM | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | SRB | MSOP (microSmall Outline IC) | RM-8 |
| ADG823BRM | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | SSB | MSOP (microSmall Outline IC) | RM-8 |

*Branding on MSOP packages is limited to three characters due to space constraints.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG821/ADG822/ADG823 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


# PIN CONFIGURATION <br> 8-Lead MSOP 

(RM-8)


## TERMINOLOGY

| $\mathrm{V}_{\mathrm{DD}}$ | Most Positive Power Supply Potential |
| :---: | :---: |
| GND | Ground (0 V) Reference |
| $\mathrm{I}_{\mathrm{DD}}$ | Positive Supply Current |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| IN | Logic Control Input |
| $\mathrm{R}_{\text {ON }}$ | Ohmic Resistance between D and S |
| $\Delta \mathrm{R}_{\mathrm{ON}}$ | On Resistance Match between any Two Channels (i.e., $\mathrm{R}_{\mathrm{ON}} \mathrm{max}-\mathrm{R}_{\mathrm{ON}} \mathrm{min}$ ) |
| $\mathrm{R}_{\text {FLAT(ON) }}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| $\mathrm{I}_{\mathrm{S}}(\mathrm{OFF})$ | Source Leakage Current with the Switch OFF |
| $\mathrm{I}_{\mathrm{D}}$ (OFF) | Drain Leakage Current with the Switch OFF |
| $\mathrm{I}_{\mathrm{D}}, \mathrm{I}_{\mathrm{S}}(\mathrm{ON})$ | Channel Leakage Current with the Switch ON |
| $\mathrm{V}_{\mathrm{D}}\left(\mathrm{V}_{\mathrm{S}}\right)$ | Analog Voltage on Terminals D and S |
| $\mathrm{V}_{\text {INL }}$ | Maximum Input Voltage for Logic "0" |
| $\mathrm{V}_{\text {INH }}$ | Minimum Input Voltage for Logic "1" |
| $\mathrm{I}_{\text {INL }}\left(\mathrm{I}_{\text {INH }}\right)$ | Input Current of the Digital Input |
| $\mathrm{C}_{\mathrm{S}}$ (OFF) | OFF Switch Source Capacitance |
| $\mathrm{C}_{\mathrm{D}}$ (OFF) | OFF Switch Drain Capacitance |
| $\mathrm{C}_{\mathrm{D}}, \mathrm{C}_{\mathrm{S}}(\mathrm{ON})$ | ON Switch Capacitance |
| $\mathrm{t}_{\mathrm{ON}}$ | Delay between Applying the Digital Control Input and the Output Switching ON |
| $\mathrm{t}_{\text {OFF }}$ | Delay between Applying the Digital Control Input and the Output Switching OFF |
| $\mathrm{t}_{\text {BBM }}$ | OFF time or ON time measured between the $90 \%$ points of both switches, when switching from one address state to another. |
| Charge Injection | It is a measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| Crosstalk | It is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Off Isolation | A Measure of Unwanted Signal Coupling through an OFF Switch |
| Bandwidth | The Frequency at which the Output Is Attenuated by -3 dBs |
| On Response | The Frequency Response of the ON Switch |
| Insertion Loss | The Loss due to the On Resistance of the Switch |

## ADG821/ADG822/ADG823-Typical Performance Characteristics



TPC 1. On Resistance vs. $V_{D}\left(V_{S}\right)$


TPC 4. On Resistance vs. $V_{D}\left(V_{S}\right)$ for Different Temperatures


TPC 7. $t_{\text {ON }} / t_{\text {OFF }}$ vs. Temperature


TPC 2. On Resistance vs. $V_{D}\left(V_{S}\right)$


TPC 5. Leakage Currents vs. Temperature


TPC 8. Off Isolation vs. Frequency


TPC 3. On Resistance vs. $V_{D}\left(V_{S}\right)$ for Different Temperatures


TPC 6. Charge Injection vs. Source Voltage


TPC 9. On Response vs. Frequency


TPC 10. Crosstalk vs. Frequency


TPC 11. Logic Threshold Voltage vs. Suppply Voltage


TPC 12. THD

## ADG821/ADG822/ADG823

## Test Circuits



Test Circuit 1. On Resistance


Test Circuit 2. Off Leakage


Test Circuit 3. On Leakage


Test Circuit 4. Switching Times


Test Circuit 5. Break-Before-Make Time Delay, $t_{B B M}$ (ADG823 only)


Test Circuit 6. Charge Injection


Test Circuit 7. Off Isolation


Channel-to-channel crosstalk $=20$ LoG $\frac{\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\mathrm{S}}}$
Test Circuit 9. Channel-to-Channel Crosstalk


INSERTION LOSS $=20$ LOG $\frac{V_{\text {OUT }} \text { WITH SWITCH }}{V_{\text {OUT }} \text { WITHOUT SWITCH }}$

Test Circuit 8. Bandwidth

## OUTLINE DIMENSIONS

## 8-Lead MSOP Package [MSOP] (RM-8)

Dimensions shown in millimeters


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