PRELIMINARY | Data Sheet | October 1998 | File Number 4509.1

Dual High Speed Laser Driver

The HIP9022 Dual High Speed Laser Driver is designed to operate with a constant current drain from the power supply. This current defines the laser operating power. The current is accurately controlled in the range of 0.5A to 2A to deliver constant optical power from the laser when used with an external Power FET and Power Sense resistor. The operating circuit allows flexibility in choosing driver current levels.

Eight S/H circuits are multiplex bus controlled to provide analog data for the dual laser drivers. The bus is updated during the blanking period of the laser printer scan with a data rate up to 2.5MHz. A “thermo-electric-cooler” control circuit provides temperature control of the laser. Two on-chip ESD diodes protect each laser.

A principle advantage of the Dual High Speed Laser Driver is accomplished by managing the high currents externally with discrete Power FETs and thereby not forcing large switching currents to exist on the same IC substrate with the precision control circuitry.

Features

- Dual High Speed Laser Driver with Data Rates up to 2.5MHz
- 0.5A to 2A Range of Constant Current Source Controlled to 0.1% Full Scale
- Low Signal Transients with Controlled Constant Current Switching
- Laser Optical Power Controlled to Better than 0.5%
- Thermoelectric Cooler (TEC) Circuit to Control Temperature to within $0.25^{o}C$
- Multiplexed Sample/Hold (S/H) Bus Interface
- Serial Diagnostic Bus with Multiplexed Output
- High Current ESD Diodes for Laser Diode Protection

Applications

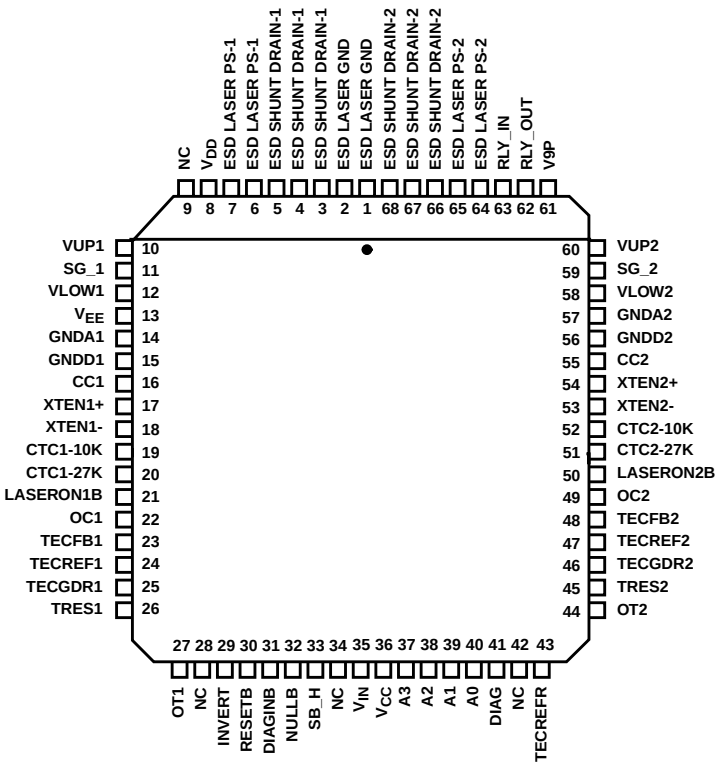
- Dual Laser Printer Driver

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP9022AM	0 to 100	68 Ld PLCC	N68.95

Pinout

HIP9022 (PLCC)
TOP VIEW



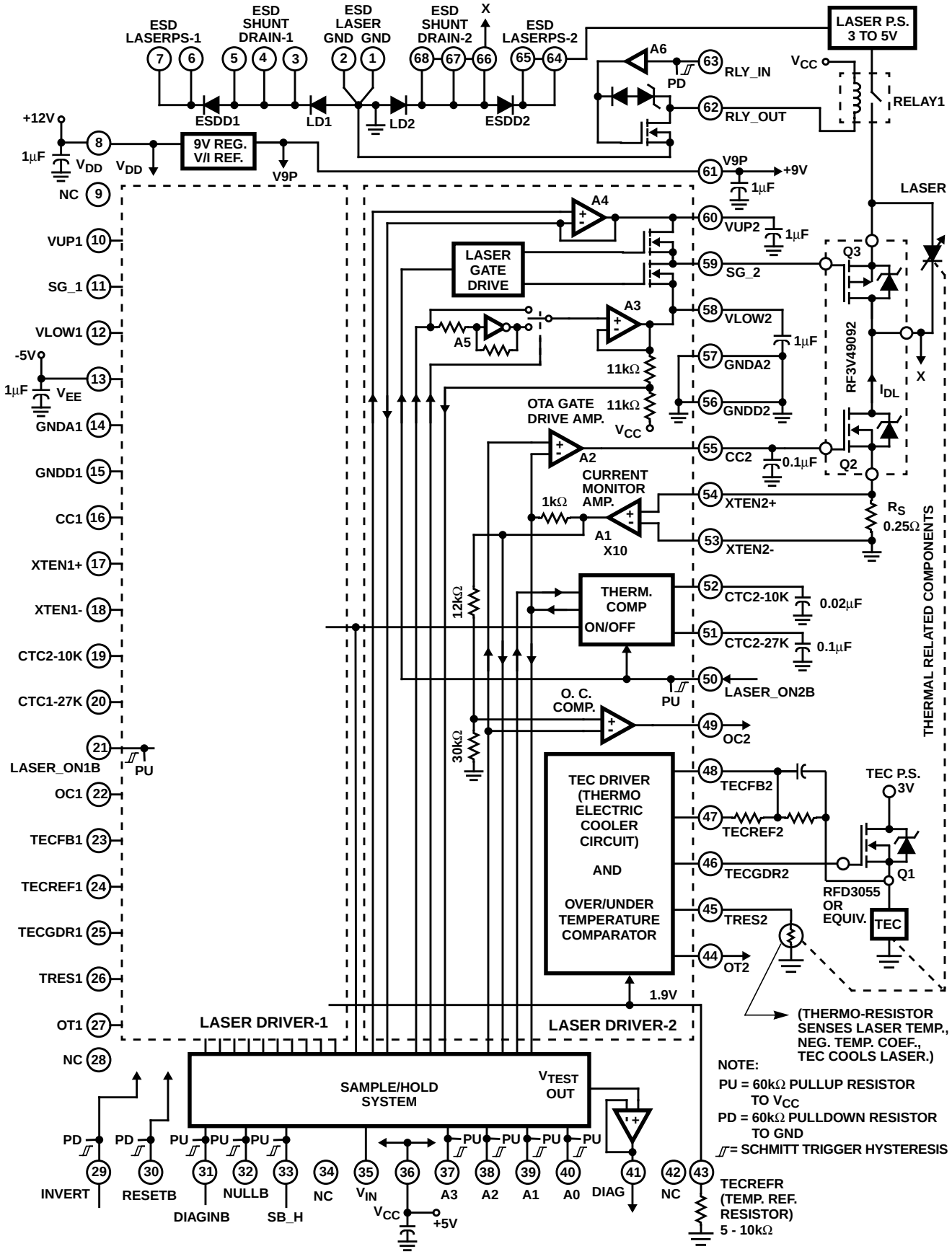


FIGURE 1. HIGH SPEED LASER DRIVER FUNCTIONAL BLOCK DIAGRAM SHOWN IN QUIESCENT P.S. CURRENT TEST MODE

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2	ESD LASER GND	Laser supply and system ground.
3, 4, 5	ESD SHUNT DRAIN-1	Laser diode ESD protection.
6, 7	SD LASER PS-1	Laser power supply ESD protection.
8	V_{DD}	Input for 12V power supply.
9	NC	No connection.
10	VUP1	Filter capacitor for internally generated shunt gate upper voltage level (1µF).
11	SG_1	Drive output to shunt Power FET gate.
12	VLOW1	Filter capacitor for internally generated shunt Power FET gate lower drive voltage level (1µF).
13	V_{EE}	Input for -5V power supply.
14	GNDA1	Analog Ground.
15	GNDD1	Digital Ground.
16	CC1	Gate drive to the current source Power FET.
17	XTEN1+	Times 10 constant current monitor amplifier input from the high side of the sense resistor.
18	XTEN1-	Times 10 constant current monitor amplifier input from the low side of the sense resistor.
19	CTC1-10K	Thermal compensation short time constant where T_{TC} = External C x 10kΩ. (External C typically equal 0.02µF).
20	CTC1-27K	Thermal compensation long time constant where T_{TC} = External C x 27kΩ. (External C typically equal 0.1µF).
21	LASERON1B	Input control turns shunt Power FET gate drive ON/OFF with 5V CMOS logic. Low turns the shunt Power FET OFF and the Laser ON. These pins have an internal pull-up.
22	OC1	Laser over-current indicator flag.
23	TECFB1	Feedback to stabilize the TEC loop.
24	TECREF1	Feedback to stabilize the TEC loop.
25	TECGDR1	Thermo-Electric Cooler Power FET gate drive.
26	TRES1	Thermo-Resistor output to ground connection for TEC control.
27	OT1	Laser out of temperature range indication.
28	NC	No connection.
29	INVERT	High input converts to operation with Pmos Current source and NDmos shunt Power FET external transistors. Low input converts to operation with NDmos Current source and Pmos high side shunt Power FET external transistors. This pin has an internal pull-down.
30	RESETB	When RESETB is held low, three reset actions occur. The LASERONB input is defeated to a Laser Off condition. The SG_1, 2 outputs are switched to VLOW when in the INVERT low mode and to VUP when in the INVERT high mode. The TEC amplifier is turned off to switch the TECGDR1, 2 outputs to Ground. This pin has an internal pull-down.
31	DIAGINB	Low level activates the diagnostic mode. This pin has an internal pull-up.
32	NULLB	Auto-zeros the S/H amplifier selected by address when held low. This pin has an internal pull-up.
33	SB_H	Samples the selected address when held low. The setup time for address is <25ns. This pin has an internal pull-up.
34	NC	No connection.
35	V_{IN}	Analog voltage sampled by selected S/H. The input voltage range is 0 to 5V. There is an internal voltage clamp for voltage outside of this range. There is an internal 2 - 3µs filter for noise rejection.
36	V_{CC}	Input for 5V power supply.
37	A3	Refer to the Table 1 Address Map. The A3 - A0 pins have an internal pull-up.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
38	A2	Refer to the Table 1 Address Map. The A3 - A0 pins have an internal pull-up.
39	A1	Refer to the Table 1 Address Map. The A3 - A0 pins have an internal pull-up.
40	A0	Refer to the Table 1 Address Map. The A3 - A0 pins have an internal pull-up.
41	DIAG	Diagnostic output, A 0V - 5V analog signal output limits internally to a range of -0.3V to 5.3V. The output is the channel addressed by A0 - A3.
42	NC	No connection.
43	TECREFER	External resistor to ground with a resistor value equal to the value of the thermo-resistor at the desired laser temperature. (Typically in the 5kΩ to 10kΩ range)
44	OT2	Laser out of temperature range indication.
45	TRES2	Thermo-Resistor output to ground connection for TEC control.
46	TECGDR2	Thermo-Electric Cooler Power FET gate drive.
47	TECREF2	Feedback to stabilize the TEC loop.
48	TECFB2	Feedback to stabilize the TEC loop.
49	OC2	Laser over-current indicator flag.
50	LASERON2B	Input control turns shunt Power FET gate drive ON/OFF with 5V CMOS logic. Low turns the shunt Power FET OFF and the Laser ON. These pins have an internal pull-up.
51	CTC2-27K	Thermal compensation long time constant where T_{TC} = External C x 27kΩ. (External C typically equal 0.1µF).
52	CTC2-10K	Thermal compensation short time constant where T_{TC} = External C x 10kΩ. (External C typically equal 0.02µF).
53	XTEN2-	Times 10 constant current monitor amplifier input from the low side of the sense resistor.
54	XTEN2+	Times 10 constant current monitor amplifier input from the high side of the sense resistor.
55	CC2	Gate drive to the current source Power FET.
56	GNDD2	Digital Ground.
57	GNDA2	Analog Ground.
58	VLOW2	Filter capacitor for internally generated shunt Power FET gate lower drive voltage level (1µF).
59	SG_2	Drive output to shunt Power FET gate.
60	VUP2	Filter capacitor for internally generated shunt gate upper voltage level (1µF).
61	V9P	Filter capacitor bypass for internally generated 9V power source (1µF).
62	RLY_OUT	Relay output drive from an N-channel FET controls an external relay to switch the Laser power supply or power supply interlock ON/OFF for both Laser Drivers.
63	RLY_IN	Relay input control with 5V CMOS logic. A high switches on the relay. This pin has an internal pulldown.
64, 65	ESD LASER PS-2	Laser power supply ESD protection.
66, 67, 68	ESD SHUNT DRAIN-2	Laser diode ESD protection.

Absolute Maximum Ratings

Maximum Analog Supply Voltage, V_{DD} . . . . . -0.3V to 14V
Logic Supply Voltage, V_{CC} . . . . . -0.3V to 6V
Analog Negative Supply Voltage, V_{EE} . . . . . 0.3V to -5.5
Maximum Laser Protection Diode Current 10A, 200ns

Operating Conditions

V_{DD} Supply Voltage Range, V_{DD} . . . . . 11.4V to 12.6V
V_{CC} Supply Voltage Range, V_{CC} . . . . . 4.5V to 5.5V
V_{EE} Supply Voltage Range, V_{EE} . . . . . -4.5V to -5.5V
Laser Power Supply Range, V_{LAS} . . . . . 3V to 5V
TEC Power Supply Range, V_{TEC} . . . . . 3V to 5V
Laser Operating Current Range, I_{DL} . . . . . 0A to 2A
TEC Operating Current Range, I_{TEC} . . . . . 0A to 2A

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JC} (^{o}C/W)
PLCC Package 40
Maximum Operating Junction Temperature, T_J . . . . . 100^{o}C
Maximum Storage Temperature Range, T_{STG} . . . . -55^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

Die Characteristics

Back Side Potential . . . . . -V_{EE}, Substrate

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_J = 100^{o}C, V_{DD} = 12V, V_{CC} = 5V, V_{EE} = -5V, INVERT Low (Figure 1 Configuration) Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V9P Voltage, No External Load	V9P	1µF Tantalum Capacitor to V9P	-	9	-	V
V9P Thermal Shutdown			150	-	-	^{o}C
V9P Thermal Shutdown Recovery			-	-	125	^{o}C
V9P Current Limiting			65	-	-	mA
V_{DD} Power Supply Current	I_{DD}		-	25	75	mA
V_{CC} Power Supply Current	I_{CC}		-	1.5	25	mA
V_{EE} Power Supply Current	I_{EE}		-75	-23	-	mA
LOGIC/DIGITAL INPUTS (A0-A3, NULLB and SB_H, LASERON1B, LASERON2B with 60kΩ Pullup Resistors; INVERT, RESETB, RLY_IN 60kΩ with Pulldown Resistors)						
Low Level Input Voltage	V_{IL}		0	-	1.5	V
High Level Input Voltage	V_{IH}		3.5	-	V_{CC} + 0.3	V
Minimum Hysteresis	V_{HYS}		0.3	-	-	V
Low Level Input Current (Inputs with Pullups)	I_{IL}		-140	-	-	µA
High Level Input Current (Inputs with Pulldowns)	I_{IH}		-	-	140	µA
CONSTANT CURRENT CONTROLLER						
OTA Gate Drive Amp. (A2) Voltage Output Range	V_G		-4	-	V_{CC}	V
Current Monitor Amp. (A1) Gain	A_{VS}		9.8	10	10.2	-
Current Monitor Amp. Differential Sense Input Range	V_{IN}		0	-	500	mV
Current Monitor Amp. Input Offset	V_{IO}		-5	-	5	mV
Current Monitor Amp. Common Mode Input Range	V_{IC}		0	-	5	V
SHUNT CURRENT SWITCH CONTROLLER (Note 2) V_{UPPER} = 2V, V_{LOWER} = -1V, Gate Load = 5000pF, VUP1, 2; 1µF Filter Capacitor to GND, VLOW1, 2; 1µF Filter Capacitor to GND, Unless Otherwise Specified						
Shunt Gate Output Rise/Fall time	t_R/t_F	10% -90% Rise, 90% -10% Fall	-	-	20	ns
Propagation Delay, LASERONB1, 2 to SG_1, 2	t_D	T_J = 100^{o}C	-	80	110	ns
		T_J = -25^{o} C	-	60	95	ns
Drive Output Voltage	V_{UPPER}		0	-	V_{CC}	V
	V_{LOWER}		-4	-	V_{CC}	V

Electrical Specifications $T_J = 100^oC$, $V_{DD} = 12V$, $V_{CC} = 5V$, $V_{EE} = -5V$, INVERT Low (Figure 1 Configuration) Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Driver Maximum Output Current	I_{DRSW}		-1	-	1	A
Shunt Controller Switching Frequency	f_{SC}		0	-	2.5	MHz
ANALOG SAMPLE/HOLD AMPLIFIERS						
Low Level Input Voltage	V_{IL}		0	-	1.5	V
Low Level Input Current	I_{IL}		-140	-	-	µA
High Level Input Voltage	V_{IH}		3.5	-	V_{CC} + 0.3	V
Minimum Hysteresis	V_{HYS}		0.3	-	-	V
Analog Input Voltage Range	V_{IN}		0	-	V_{CC} - 0.2	V
Minimum Sample/Hold Pulse Width			-	10	-	µs
Droop Rate, Constant Current Addresses #'s 1, 2			-	-	0.006	V/s
Droop Rate, Other Addresses #'s 3 - 8			-	-	0.06	V/s
Maximum Analog Multiplexing Frequency			-	-	30	kHz
DIAGNOSTIC OUTPUT (DIAG Output)						
Voltage Follower Voltage Range	V_O		0	-	V_{CC} - 0.2	V
Voltage Follower Maximum Clamp Voltage	V_{CL}		-	-	V_{CC} + 0.3	V
O. C. (OVER CURRENT) COMPARATOR (OC1, 2 Outputs)						
Threshold (%) O.C. Detection		Programmed Current as Ref.	-	140	-	%
Output Voltage, Low Level	V_{OL}		0	-	1.5	V
Output Current, Low Level	I_{OL}		-	12	-	mA
Output Voltage, High Level	V_{OH}		3.5	-	V_{CC} - 0.5	V
Output Current, High Level	I_{OH}		-	4	-	mA
TEC REF. RESISTOR AND DRIVE OUTPUT						
TECREFR Output Voltage to Reference Resistor	V_{REFR}		1.71	1.9	2.09	V
TECGDR1, 2 Drive Output Voltage	V_{TECG}		0	-	9	V
OVER/UNDER TEMPERATURE COMPARATOR (To OT Output)						
Under Temp. Limit	T_{LOW}		2.07	2.1	2.13	V
Over Temp. Limit	T_{HIGH}		1.67	1.7	1.73	V
Output Voltage, Low Level	V_{OL}		0	-	1.5	V
Output Current, Low Level	I_{OL}		-	12	-	mA
Output Voltage, High Level	V_{OH}		3.5	-	V_{CC} - 0.5	V
Output Current, High Level	I_{OH}		-	4	-	mA
RELAY DRIVER						
Driver Output Current	I_{RLY}		-	-	30	mA
Drain to Source Resistance	$r_{DS(ON)}$		-	20	-	Ω
LASER PROTECTION DIODES See Figure 1						
Maximum Diode Forward Voltage Drop	V_{LDX}, V_{ESDX}	10A Peak Current	-	-	2	V
Maximum Reverse Diode Current	I_{LDX}		-	-	1	µA

NOTE:

2. The drive control sets the high and low voltages to the gate of the Power FET driver (shunt switch). Both the upper and lower levels are set by values held in two of the sample/hold amplifiers. External capacitors at VUP1, 2 and VLOW1, 2 are required for stabilization.

Address, Timing and Waveforms

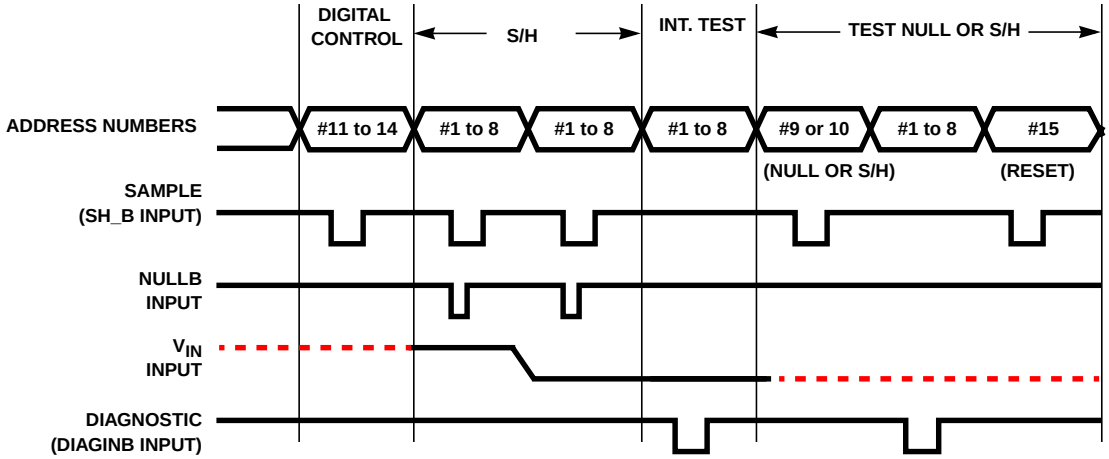


FIGURE 2. ADDRESS WITH SAMPLE, NULL, V_{IN} AND DIAGONAL WAVEFORMS

TABLE 1. HIP9022 ADDRESS MAP

A3	A2	A1	A0	ADDRESS NO.	FUNCTION TYPE	FUNCTION NAME
0	0	0	0	1	ANALOG	$V_{IN(DL)}$ Voltage for Constant Current Level, Laser Driver #1
0	0	0	1	2	ANALOG	$V_{IN(DL)}$ Voltage for Constant Current Level, Laser Driver #2
0	0	1	0	3	ANALOG	V_{LOWER} Level, Laser Driver #1
0	0	1	1	4	ANALOG	V_{LOWER} Level, Laser Driver #2
0	1	0	0	5	ANALOG	V_{UPPER} Level, Laser Driver #1
0	1	0	1	6	ANALOG	V_{UPPER} Level, Laser Driver #2
0	1	1	0	7	ANALOG	$V_{IN(DL)}$ Thermal Compensation Level, Laser Driver #1
0	1	1	1	8	ANALOG	$V_{IN(DL)}$ Thermal Compensation Level, Laser Driver #2
1	0	0	0	9	DIGITAL	Test Mode: S/H Amp, Auto Zero Null Voltage (Note 4)
1	0	0	1	10	DIGITAL	Test Mode: S/H Amp Output Voltage (Note 4)
1	0	1	0	11	DIGITAL	Test Mode: Set VUP and V_{LOW} Amps to Three-State (Note 4)
1	0	1	1	12	DIGITAL	VLOW#1 Set to Positive Output (Default is Negative)
1	1	0	0	13	DIGITAL	VLOW#2 Set to Positive Output (Default is Negative)
1	1	0	1	14	DIGITAL	Thermal Compensation Activated (Default is Deactivated)
1	1	1	0	15	DIGITAL	Reset Digital Address (9-14) to Default State
1	1	1	1	16	DIGITAL	Idle Condition (S/H Pin Defeated) (Note 3)

NOTES:

3. The Idle address is protective in that SB_H input noise cannot disturb the chip if the Idle address is selected; also, the Address inputs are High (selecting Idle state) if the pins are open.
4. Address Numbers 9 - 11 are shaded to indicate test mode conditions and are shown for information only. These addresses are used in original production testing and not required for user applications. However, note that Address No. 15 will force a reset for Address Numbers 9 - 14.
5. Digital Programming: To set the digital addresses, only the proper digital address and a negative pulse >100ns on SB_H is needed. To reset the digital addresses to the default states, Address 15 and a SB_H pulse >100ns is needed. Normally the digital addresses will be set first, and the analog addresses programmed next. The test modes, Address Numbers 9 - 11, will normally only be used during factory testing. An address 15 Reset should normally precede most programming in order to assure that the digital address states begin in their default state. Otherwise, the digital address states will be undefined because there is no power-up-reset.
6. Analog Programming: To program the eight S/H circuits, addresses of 0-5V analog signal on V_{IN} and negative pulses on NullB (10µs) and SB_H (20µs) pins are needed. The NullB pulse is valid only during the SB_H pulse and should occur during the first half of the SB_H pulse. The S/H amplifier is auto-zeroed for zero offset when both NullB and SB_H are low. The input V_{IN} is captured on the S/H storage capacitor during SB_H low.
7. The Diagnostic mode reads map addresses 1 - 8 via the DIAG output when DIAGINB is low.

Circuit Block Descriptions

Laser Drive Circuitry

In Figure 3, the gate of the external current source Power FET, Q2 is driven via the Operational Transconductance Amplifier (OTA), A2 on the IC. The voltage on the current sense resistor, R_S in the source of the Power FET is monitored by a X10 gain of the feedback amplifier, A1. The stability of the current loop is established with an external 0.1µF capacitor to ground at the gate of the Power FET. The sampled voltage range is 0 to 0.5V when the proper value of sense resistor, R_S is chosen (typically 0.25Ω for 2A). The OTA, A2 compares the X10 gain signal to a 0 to 5V reference signal from an on-chip Sample and Hold (First S/H) circuit. The Q2 drain current (Laser Drive current), I_{DL} is:

$$I_{DL} = \frac{V_{IN(DL)}}{(R_S \times 10)} \quad \text{(EQ. 1)}$$

where $V_{IN(DL)}$ is the programmed V_{IN} for the First S/H voltage reference signal.

The S/H reference for the Laser Drive Current current is updated with other multiplexed S/H circuits from a serial bus and an off-chip D/A converter. Laser constant current is fully controllable by the multiplex analog S/H bus, allowing accurate calibration of the laser output and corrections as the laser ages.

In Figure 1, the laser drive current from Q2 is digitally switched to either flow through or is shunted around the laser diode by switching the external Shunt Power FET, Q3 on or off. The gate of the Shunt FET is switched between two voltages (Upper and Lower) which are provide by 2nd and 3rd S/H circuits. These Shunt FET gate drive levels are fully programmable via the multiplexed analog S/H bus. By adjusting these levels to account for the laser power supply, the Shunt FET threshold and channel resistance; minimum Shunt FET gate drive power levels can be established. The Upper and Lower gate voltage driver circuits are two high current OTA amplifiers with two filter capacitors. The upper voltage is programmable in the 0V to V_{CC} range at the input of amplifier A4. The lower voltage is programmable in the range of -4V to V_{CC}. The -4V extension is accomplished by an optional on-chip voltage inverter circuit. The input to amplifier A3 is either direct from the S/H input or inverted by amplifier A5.

The maximum laser on-off switching speeds are dependent on the selection of Shunt FETs. A Harris dual complementary MOSFET, RF3V49092 or RF3S49092 has been designed specifically for this application. With the constant current set at 0.8A, a typical laser switching speed of 20ns has been measured.

Thermal Compensation

A 4th S/H circuit is used to set the amplitude of an optional thermal compensation signal which can be used to modulate the constant laser current source as a two pole filtered effect of the laser on-off data. This feature may be disabled when it is not required. This circuit is designed to compensate for the temperature variations in the laser as the laser is turned on and off. The bypass capacitors at the Thermal Comparator (CTCx-10K, CTCx-27K) represent the respective poles for the filter.

A laser cools after it has been off for a period of time and is more efficient when it is turned-on. Compensation for the increased efficiency is made by slightly reducing the current level of the constant current source FET. The level will be reduced by a programmable amount of 0 to 5% of full scale. The programmable amount is fixed by the level of compensation to S/H addresses 7 and 8 (see Table 1). The percent of modulation (change) in drive current is calculated as follows:

$$\text{Modulation}\,\% = \frac{V_{IN(TC)}}{V_{IN(DL)}} \times 5\% \quad \text{(EQ. 2)}$$

For example, if we control the Laser Drive current with 2V programmed with address 1 and 2 for the First S/H's, given that $V_{IN(DL)}$ = 2V and R_S = 0.25Ω. Then, from EQ. 1, $I_{DL} = V_{IN(DL)}/(R_S \times 10) = 2/(0.25 \times 10) = 0.8A$.

If 2V is programmed to addresses 7 and 8 as Thermal Compensation, $V_{IN(TC)}$ for the 4th S/H's, then, Mod.% = (2/2) x 5% = 5%.

In Figure 3, the correction is applied from the output of the Thermal Compensation circuit (where the current is 2V/20kΩ = 0.1mA) to the input of amplifier A2. The 0.1mA is forced into the 1kΩ resistor (and the low Z output of A1) to increase the voltage at the inverting input of A2 by 0.1V or 5% of the $+V_{IN(DL)}$ input (2V) to A2. The modulation input is limited by the 0 to V_{CC} input range of S/H maximum V_{IN}.

Input Data

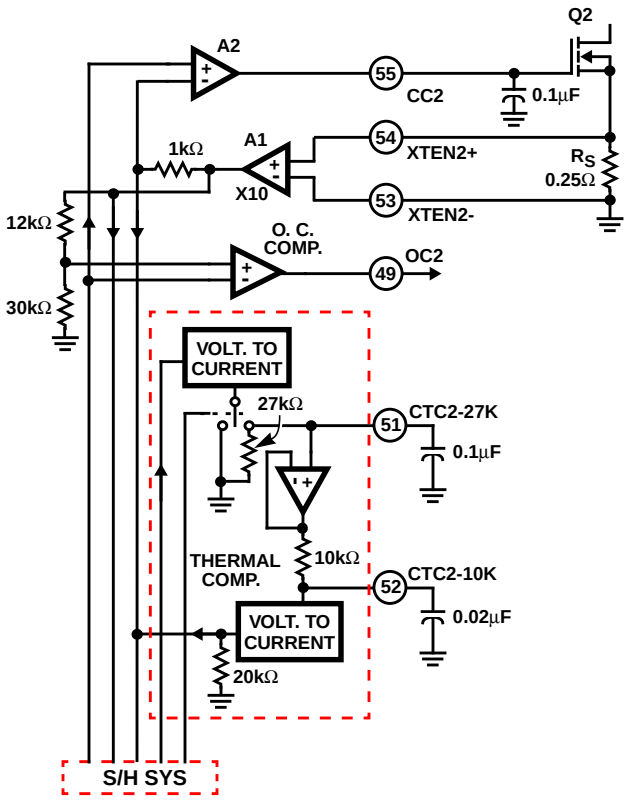


FIGURE 3. LASER CONSTANT CURRENT SOURCE DRIVER WITH OVER CURRENT DETECTION AND THERMAL COMPENSATION

Both analog and digital data is input to control the action of the dual laser driver. Address codes and input data are described in the Table 1 Address Map. Digital data is normally entered first, followed by the analog data via the multiplexed analog bus which updates the S/H stored voltage levels. Four bit digital addresses to pins A3, A2, A1 and A0 are decoded to define the programming functions for data input. It is important to note that Address 15 is a reset for Addresses 9 - 14 and should be performed as the first step in programming because there is no power-on-reset on-chip.

Diagnostic Output Data

For the purpose of monitoring on-chip signals, the multiplexed bus can be used to output signals (at the DIAG pin) via an analog diagnostic amplifier. This mode has the capability to monitor the multiplexed output of four (0-5V) analog signals for each laser channel. Note that the diagnostic information at the VLOW (Amplifier A3) output is 2:1 resistor divided to +5V (V_{CC}) to return this signal to a 0 to 5V range. To minimize noise problems the monitoring function is normally performed during the laser scan for only one signal per scan. In addition, there are 3 test modes which allows the bus to present analog signals for testing the performance of the eight S/H circuits.

Thermo-Electric-Cooler (TEC) Circuitry

Figure 4 shows the Thermal Electric Cooler (TEC) drive circuit with an external reference resistance, a thermo-resistor to sense temperature plus feedback components for stable drive. There is a thermo-resistor reference input on the chip for monitoring the laser's temperature via a 5-10kΩ thermo-resistor which must be mounted near the laser. A reference voltage on the external reference resistor is established by a current from a stable bias source. This current is mirrored to the thermo-resistor (one for each laser driver system). A comparator senses the voltage across the reference resistor versus the voltage across the thermo-resistor and drives the gate of the TEC FET driver. As such, the TEC circuit senses the thermo-resistor input as a measure of the laser temperature and the TEC drive is adjusted to maintain a stable Laser temperature slightly below the ambient temperature. An external Power FET is needed to provide the high TEC driver currents. An out of range temperature output for each laser is also provided.

Laser Protection Diodes

Another feature included on the chip is two high current ESD diodes which, in the printer system, are used to protect the Laser Diodes from ESD damage. Another component of Laser protection in printer systems are relays to disconnect the Lasers when in a non-operating mode. For this purpose, a single relay driver is included.

Over Current Flag Output (OC1, OC2)

Over-current detection is also included on-chip. The circuit of Figure 3 shows the over current detection circuit. For each laser source current driver, the over current monitor compares the S/H input of amplifier A2 to the output of amplifier A1. If the output voltage of A1 exceeds the input of A2 by 40%, then an over current state exists and the OC output will go high.

Invert Option

An INVERT input reconfigures the device such that the constant current source can be high side instead of the normal low side. This provides functionality for driving laser diodes in a common cathode configuration as opposed to the normal common anode configuration. The INVERT must be low (or open with the internal pull down) for the Figure 1 circuit.

Reset Action

The RESETB (active low) controls three things:
(1) The TEC driver is turned off.
(2) The Shunt driver is turned on to turn off the laser.
(3) The Constant current driver is turned off.

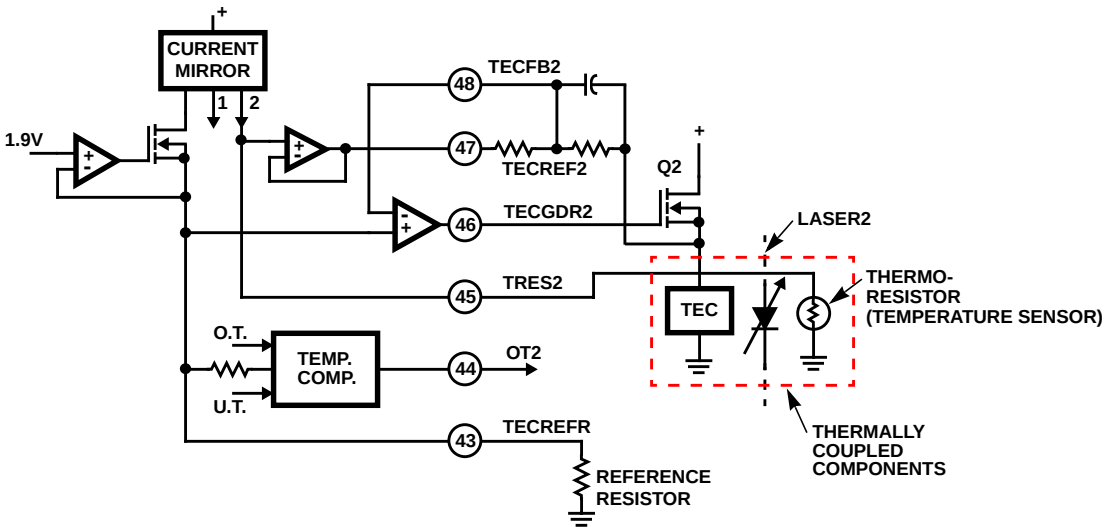
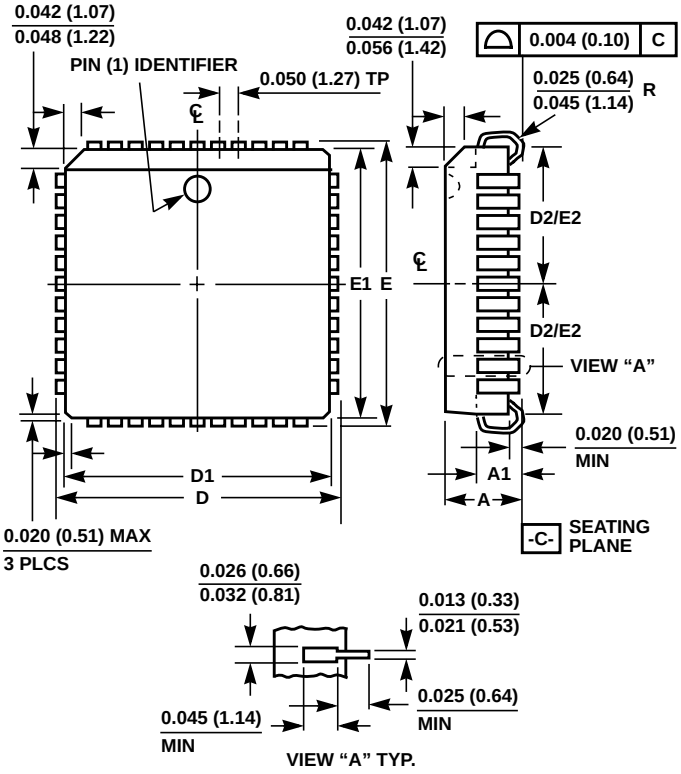


FIGURE 4. TEC (THERMAL ELECTRIC COOLER) CIRCUIT WITH REFERENCE RESISTOR AND THERMAL RESISTOR SENSOR OF LASER TEMPERATURE

Plastic Leaded Chip Carrier Packages (PLCC)



N68.95 (JEDEC MS-018AE ISSUE A)
68 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.985	0.995	25.02	25.27	-
D1	0.950	0.958	24.13	24.33	3
D2	0.441	0.469	11.21	11.91	4, 5
E	0.985	0.995	25.02	25.27	-
E1	0.950	0.958	24.13	24.33	3
E2	0.441	0.469	11.21	11.91	4, 5
N	68		68		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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