HIP9021

PRELIMINARY

August 1996

Portable Battery Drive/Torque Controller for N-Channel MOSFETs in Motor Control Systems

Features

- **MOSFET Driver and DC Motor Controller**
- **Torque Control and Overload Protection**
- **Battery Power Supply . . . . . +5V to +15V**
- **BiMOS IC with Low Operating Current**
  - **Maximum Supply Current 1.5mA**
  - **Maximum Input Leakage Currents 1.5μA**
- **500μA Maximum Supply Current**
- **1μA Maximum Input Leakage Currents**
- **Typical Oscillator Frequency 5kHz**
- **Power-On-Reset Control**
- **10mA Drive Capability for Gate Output**
- **Operating Temperature . . . . . -40°C to +85°C Range**

Applications

- **Portable Battery Operated Electric Drills**
- **Controller for Small DC Electric Motors**
- **Torque/Drive Controller for Inductive Loads**
- **Intelligent MOSFET Drive**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP9021IB	-40 to +85	8 Ld SOIC	M8.15

Description

The HIP9021IB is a dedicated Power MOSFET driver which drives a DC motor. As a system, motor speed is controlled while controlling torque. The primary application is drive control for portable drills while providing overload protection.

The main function of the HIP9021IB is to produce a pulse width modulated square wave signal which drives the gate of an N-Channel Power MOSFET. The duty-cycle is determined by the setting of an external potentiometer at the TRIGGER (speed control) input. As the TRIGGER voltage level is decreased the duty-cycle of the square wave and the speed of the motor is increased.

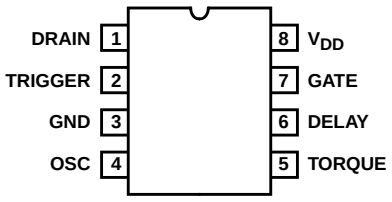
The torque of the motor is limited by the voltage level sensed at the drain of the external Power MOSFET. When the current reaches an adjustable limit set at the TORQUE input, the drive of the Power MOSFET is disabled.

The system control components include 2 adjustable potentiometer controls and 2 capacitors for the operating frequency and torque delay control. A fixed or battery supply voltage in the range of 5V to 15V may be used.

The HIP9021IB is provided in a small outline plastic package for a compact surface mount to a ceramic substrate. The surface mount assembly can be fit directly into the trigger of a portable electric drill.

Pinout

HIP9021IB
(SOIC)
TOP VIEW



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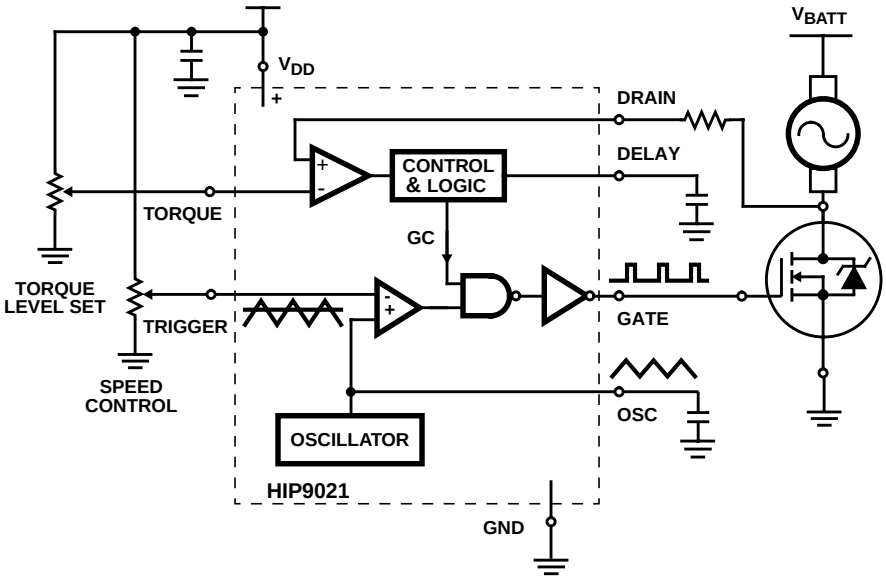
Block Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +16V
Input Voltage. . . . . GND -0.3V to V_{CC} +0.3V
Maximum Current, I_{DD} 50mA
Maximum Transient Reverse Current, I_R (10s). . . . . -50mA

Operating Conditions

Typical Power Supply Voltage. 7.5V
Operating Voltage Range . . . . . +5V to +15V
Operating Temperature Range . . . . . -40°C to 150°C
Typical Oscillator Frequency. 5kHz

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	175

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

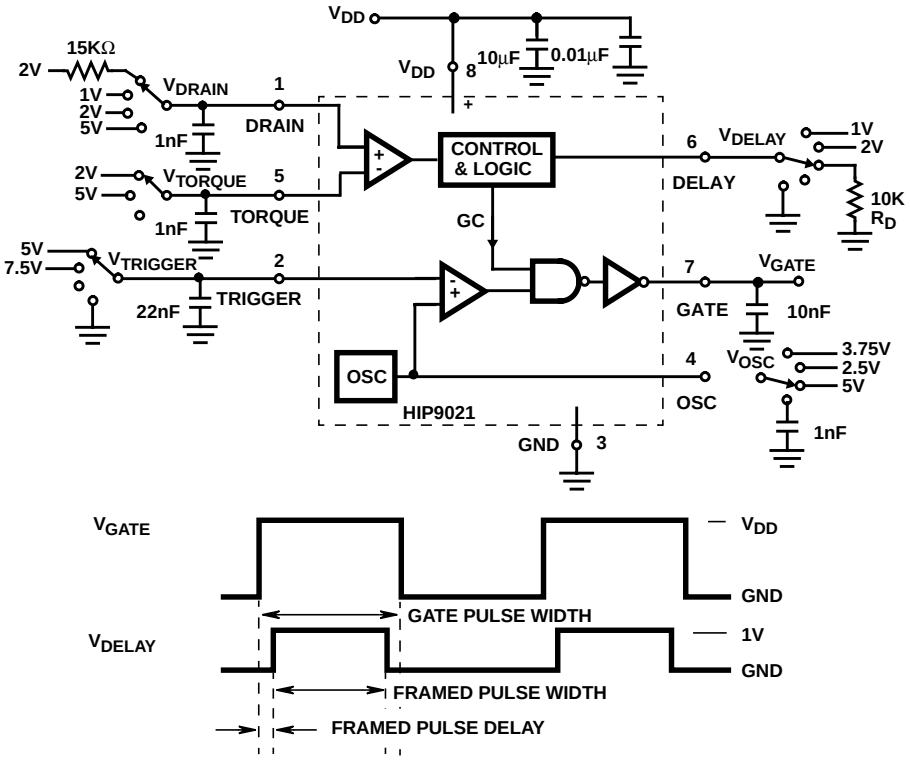
Electrical Specifications

V_{DD} = 7.5V, Figure 1 Test Circuit, Table 1 Conditions, T_A = +25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Supply Current	I_{DD}		0.1	1.2	3.1	mA
OSC Source Current	$+I_{OSC}$		19	25	32	µA
OSC Sink Current	$-I_{OSC}$		-32	-25	-19	µA
OSC Threshold Voltage	$V_{OSC(TH)}$		4.75	4.95	5.25	V
OSC Trigger Voltage	$V_{OSC(TR)}$		2.30	2.45	2.65	V
TRIGGER Input Leak Current	$I_{TRIGGER}$		-	0.02	1.5	µA
TORQUE Input Leak Current	I_{TORQUE}		-	0.02	1.5	µA
DELAY Current at 1V	I_{DELAY1}		1.5	3.4	6	µA
DELAY Current at 2V	I_{DELAY2}		1	32	50	mA
DELAY Threshold Voltage	$V_{DELAY(TH)}$		1.8	1.9	2	V
DRAIN Input Resistance	R_{DRAIN}		150	260	350	kΩ
DRAIN Current	I_{DRAIN}		1	1.7	4.6	mA
GATE Output Source Current	I_{GATE}		10	18	-	mA
GATE Output Voltage	V_{GATE}		6.5	7.4	-	V
GATE Output Slew Rate	$V_{GATE(S/R)}$	Measured in Typical Application Circuit, Duty Cycle = 50%, See Figure 2	-	10	-	V/µs
DELAY Output Framed Pulse Duty Cycle	FP/DC	Gate Duty Cycle = 50%; V_{TORQUE} = GND; V_{DRAIN} = V_{GATE}; DELAY =10kΩ to GND, Refer to Figure 1 for the Test circuit and Timing Diagram of the DELAY Output Pulse Frame.	-	44	-	%
DELAY Output Framed Pulse Delay, V_{GATE} to V_{DELAY}	FP/DLY		-	3	-	%
Typical Oscillator Frequency	f_{OSC}	T_A = 25°C	-	5	-	kHz
		T_A = -40°C	-	7.2	-	kHz
		T_A = 85°C	-	3.6	-	kHz

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.



NOTE: The timing diagrams relate to the delay output framed pulse and show the time duration of the delay pulse "framed" inside of the gate pulse. The framed pulse duty cycle and delay, in percent, are measured in reference to the gate pulse which is set at 50% duty cycle. The Delay output framed pulse delay is one-half of the difference of the gate pulse width minus delay output framed pulse width.

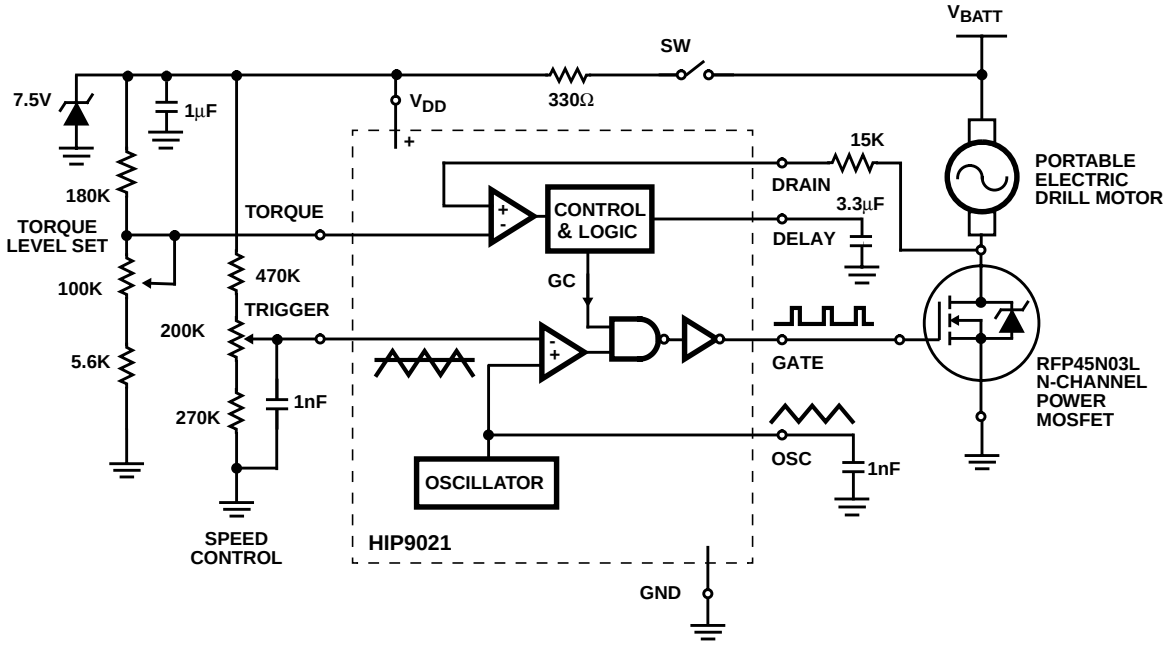
FIGURE 1. ELECTRICAL CHARACTERISTICS TEST CIRCUIT FOR SIGNAL FUNCTIONS OF THE HIP9021

TABLE 1. SWITCH POSITIONS OF FIGURE 1 FOR ELECTRICAL CHARACTERISTIC TESTING

SYMBOL	DRAIN	TRIGGER	OSC	TORQUE	DELAY	GATE	MEASURE
I_{DD}	15KΩ to 2V	GND	3.75V	2V	Open	Open	I_{DD} Current Into V_{DD} Pin
$+I_{OSC}$	15KΩ to 2V	GND	2.5V	2V	Open	Open	Source Current From OSC Pin
$-I_{OSC}$	15KΩ to 2V	GND	5V	2V	Open	Open	Sink Current Into OSC Pin
$V_{OSC(TH)}$	1V	Open	1nF	2V	Open	Open	Positive Peak OSC Voltage
$V_{OSC(TG)}$	1V	Open	1nF	2V	Open	Open	Negative Peak OSC Voltage
$I_{TRIGGER}$	15KΩ to 2V	5V	5V	2V	Open	Open	TRIGGER Leakage Current
I_{TORQUE}	15KΩ to 2V	Open	5V	5V	Open	Open	TORQUE Leakage Current
I_{DELAY1}	15KΩ to 2V	7.5V	1nF	Open	1V	Open	Current to DELAY Pin
I_{DELAY2}	15KΩ to 2V	7.5V	1nF	Open	2V	Open	Current to DELAY Pin
$V_{DELAY(TH)}$	1V	Ramp Up	1nF	2V	GND	Read V_{GATE}	Measure $V_{TRIGGER}$ When V_{GATE} Less Than 0.5V
R_{DRAIN}	5V	GND	1nF	2V	GND	Open	DRAIN Current; Calculate $R_{DRAIN} = 5V/I_{DRAIN}$
I_{DRAIN}	1V	7.5V	5V	2V	Open	Open	DRAIN Current
V_{GATE}	5V	GND	1nF	2V	Open	Open	Measure $V_{GATE} = V_{OUT}$
I_{GATE}	2V	GND	1nF	2V	GND	Set to V_{OUT} -0.5V	Measure I_{GATE} Source Current with $V_{GATE} = V_{OUT}$ -0.5V
$V_{GATE(S/R)}$	Refer to Figure 2 Application Circuit, 50% GATE Output Duty Cycle						GATE Output Slew Rate
FP/DC							Reference Figure 1 Waveforms
FP/DLY							Reference Figure 1 Waveforms
f_{OSC}	1V	$V_{OSC(TH)}$ - -1V	1nF	2V	GND	25KΩ Load	GATE Output Timing

Pin Descriptions

NAME	NUMBER	DESCRIPTION
DRAIN	1	The input to the DRAIN pin senses the drain of a power MOSFET Output Motor Driver. The DRAIN voltage is an image of the current flowing through the power MOSFET. By limiting this voltage, the torque of the motor can be controlled.
TRIGGER	2	The TRIGGER input is an analog voltage control level used to fix the duty-cycle at the DRAIN Output. A voltage level here is determined by a potentiometer adjustment. The TRIGGER voltage level is compared with the triangle signal from the internal oscillator to produce a pulse-width modulated signal.
GND	3	Negative pole of the battery or system ground reference.
OSC	4	Oscillator output normally terminated in a charge/discharge capacitor. A constant current is flowing in and out to charge and discharge the external capacitor.
TORQUE	5	The TORQUE input is a reference level adjustment for torque control. The voltage reference is compared with DRAIN input. If $V_{DRAIN} > V_{TORQUE}$, the GATE output pulse drive must be disabled.
DELAY	6	An external capacitor at the DELAY output is used to delay the torque control action. The external capacitor at the DELAY pin will start to be charged if a MOSFET output over-current condition is detected. The purpose of the capacitor is to delay the disabling action of the signal GATE drive.
GATE	7	The GATE output drives the Gate of the Power MOSFET.
V_{DD}	8	Positive pole of the battery or Power Supply Voltage, nominally 7.5V.



NOTE: The value chosen for the torque level set pot is dependent on the type of power MOSFET and motor characteristics. The TRIGGER is a combined SW/Speed Control function. Motor speed increases as the TRIGGER voltage decreases. Speed control range: 2.35V (Min) < $V_{TRIGGER}$ < 5.25V (Max)

FIGURE 2. TYPICAL OPERATING CIRCUIT SHOWING THE HIP9021IB AS AN N-CHANNEL MOSFET DRIVER IN A PORTABLE BATTERY ELECTRIC DRILL APPLICATION

Functional Description

Oscillator

The Oscillator triangle waveform is generated by the charge and discharge of a 1nF external capacitor connected to the OSC pin. The OSC terminal has a source and sink drive from a current mirror which delivers ±25µA. The charge and discharge of the external capacitor is controlled by 2 comparators which compare respectively V_{OSC} with 2/3 V_{DD} and V_{OSC} with 1/3 V_{DD}. The period of the triangle wave is nominally 200µs.

Gate Driver

The TRIGGER input signal is compared from the triangle waveform of the oscillator to produce a square wave signal. The duty cycle of the GATE drive signal is increased as the TRIGGER input level increases. The output of the comparator is then NANDed with a GATE Control signal which can enable or disable the GATE output. The NAND gate output is buffered to deliver 18mA typical GATE drive current.

Torque Effect

The triangle signal, after going through a divider, is also compared with TRIGGER input level. This produces another square wave of the same period but with a duty-cycle that is smaller than the GATE by ~5%. This square wave is used to enable the comparison between DRAIN and TORQUE inputs while the MOSFET is conducting.

A torque effect condition exists when 80% of the DRAIN signal is higher than the TORQUE input level set voltage of the potentiometer. During this time, the external delay capacitor of 3.3µF is charged through an internal 100K resistor. When the voltage at the DELAY pin reaches 0.25 x V_{DD}, the RS flip-flop is then set and the Gate Control (GC) signal shown in Figure 3 goes to low. The Output GATE drive signal is then disabled. This situation remains even if the voltage on the DELAY pin stays under 0.25 x V_{DD} for a sustained period of time.

At the same time, when the RS flip-flop is set, the external capacitor at the DELAY pin is discharged via the nMOS device, Q2 which is driven by the Q output of the flip-flop.

Power-On Reset (POR)

In reference to Figure 3, the power on of the chip will cause the reset of the RS Gate Control flip-flop when Q1 is switched low. As an initial condition, the Gate Control (GC) signal is reset high. Since power on is the only way to reset the RS flip-flop, a disabled GATE drive signal due to a torque effect condition requires a switched (trigger) reset.

The POR (power on reset) threshold requires that V_{DD} be less than 2V to initiate a reset. The POR circuit is based on the behavior of the voltage reference cell that produces a constant 1.15V (REF. BIAS) when V_{DD} is over 2V. When Q1 is forward biased, the Q1 drain voltage goes low to reset the input of the RS flip-flop.

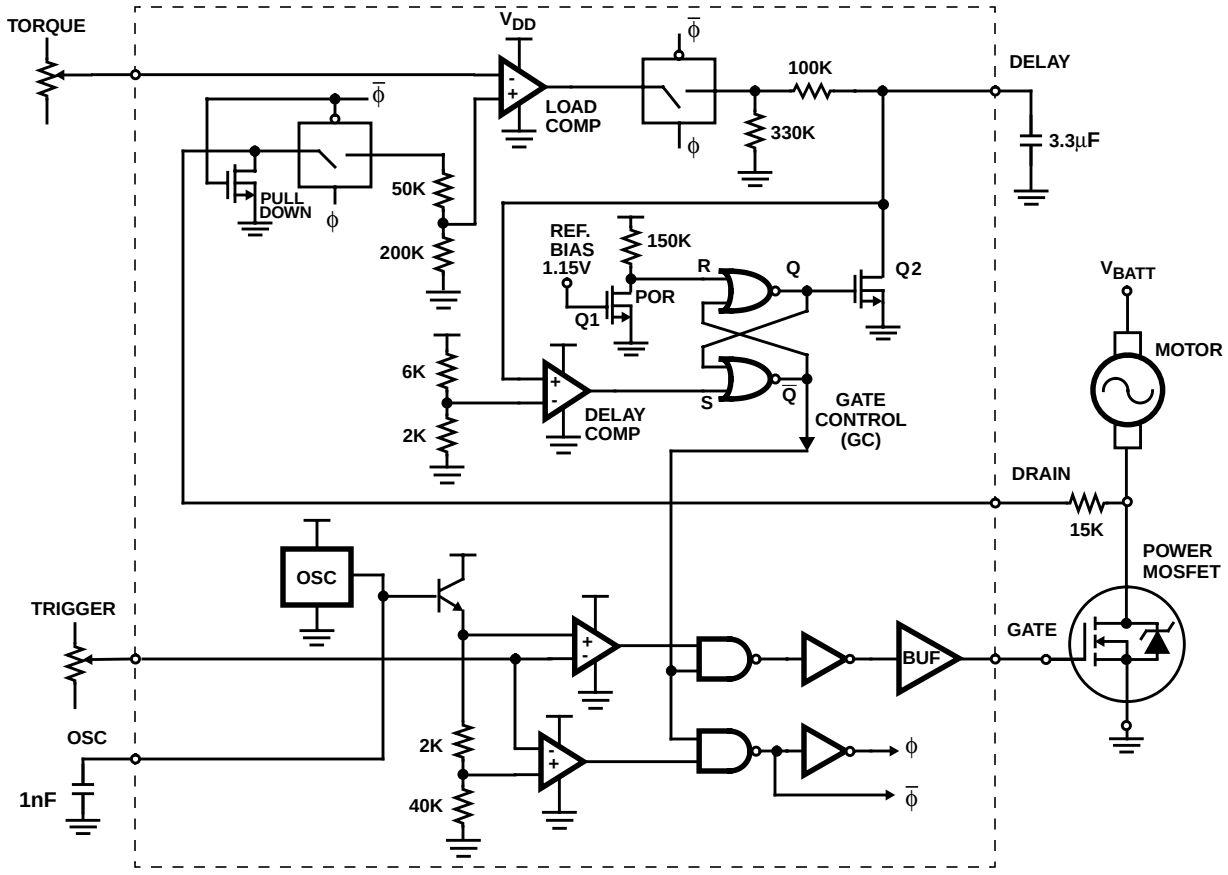
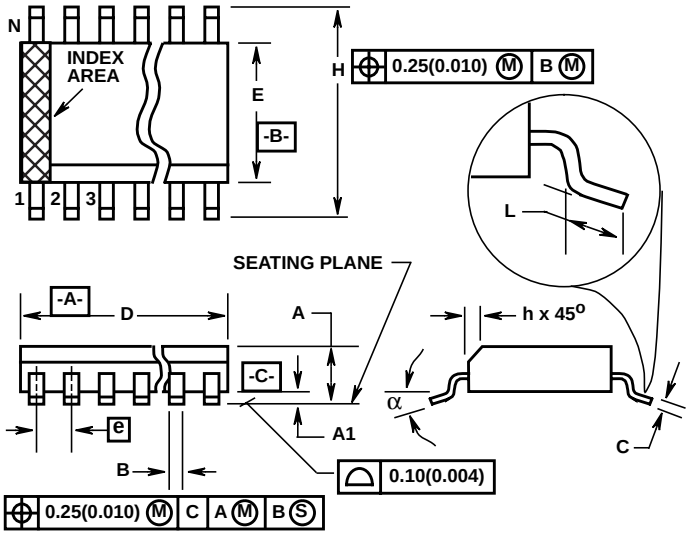


FIGURE 3. DETAILED LOGIC DIAGRAM OF THE PORTABLE DRIVE/TORQUE CONTROLLER FOR N-CHANNEL POWER MOSFETS SHOWING THE DRAIN AND TORQUE, THE GATE CONTROL LOGIC AND THE TRIGGER (SPEED) CONTROL.

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.