

Band-pass filter for spectrum analyzer

BA3826S

The BA3826S is a 7-band ($\times 2$), band-pass filter that uses microprocessor time division to output in serial to left and right stereo channels. To minimize the number of external components required and enable compact and reliable designs, all of the capacitors for the filters are on the chip.

●Applications

CD radio cassette players, mini-component stereo systems, car stereos

●Features

- 1) Seven band-pass filter elements for spectrum analyzer displays.
- 2) Microprocessor time division used for serial output on L and R channels.
- 3) All filter capacitors are built-in to minimize external attached requirements.
- 4) Low current dissipation (8mA Typ.).
- 5) Ideal for mini-component stereos and other stereo equipment.

●Absolute maximum ratings (Ta = 25°C)

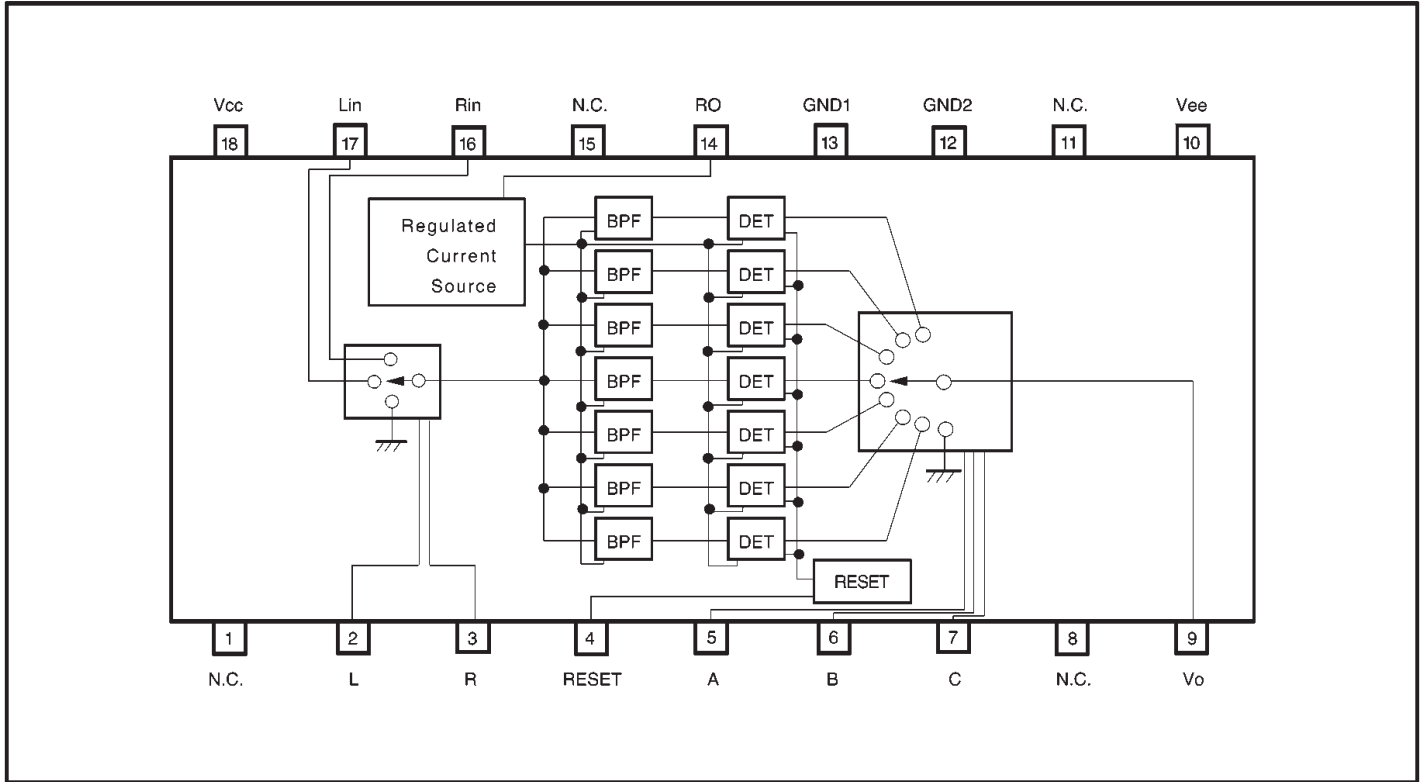
Parameter	Symbol	Limits	Unit
Applied voltage	Vcc Vee	7.0 -7.0	V
Power dissipation	Pd	600 *	mW
Operating temperature	Topr	-25~+75	°C
Storage temperature	Tstg	-55~+125	°C

* Reduced by 6.0 mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	4.0	5.0	6.5	V
	Vee	-4.0	-5.0	-6.5	V

●Block diagram



●Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{cc} = 5\text{V}$, $V_{ee} = -5\text{V}$, $R_L = 10\text{k}\Omega$, and $R_\phi = 120\text{k}\Omega$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_q	—	8.0	12	mA	
Standard output level	V_o	-3	0	3	dB	$V_{IN}=150\text{mV}_{\text{rms}}$, $V_o=1.5\text{V}$ (0dB) $f = \text{center frequency input}$
Maximum output level	V_{omax}	2.0	3.0	—	V	$V_{IN}=300\text{mV}_{\text{rms}}$, $f = \text{center frequency input}$
Output offset voltage	V_{off}	—	0	100	mV	For no signal
Center frequency 1	f_{o1}	51	60	69	Hz	$V_{IN}=150\text{mV}_{\text{rms}}$
Center frequency 2	f_{o2}	127	150	173	Hz	$V_{IN}=150\text{mV}_{\text{rms}}$
Center frequency 3	f_{o3}	340	400	460	Hz	$V_{IN}=150\text{mV}_{\text{rms}}$
Center frequency 4	f_{o4}	0.85	1	1.15	kHz	$V_{IN}=150\text{mV}_{\text{rms}}$
Center frequency 5	f_{o5}	2.04	2.4	2.76	kHz	$V_{IN}=150\text{mV}_{\text{rms}}$
Center frequency 6	f_{o6}	5.1	6	6.9	kHz	$V_{IN}=150\text{mV}_{\text{rms}}$
Center frequency 7	f_{o7}	12.7	15	17.3	kHz	$V_{IN}=150\text{mV}_{\text{rms}}$
Signal input impedance	R_{in}	30	50	70	$\text{k}\Omega$	$V_{IN}=150\text{mV}_{\text{rms}}$
Input current when reset pin "H" *1	I_{in}	120	250	380	μA	$V_{th}=5\text{V}$
Threshold level for reset pin on	V_{th}	1.7	—	—	V	
Threshold level for reset pin off	V_{th}	—	—	1.1	V	

*1 The current flowing in when the voltage on the control pin is 5V.

©Not designed for radiation resistance.

R_ϕ is a metal film resistor.

● Measurement circuit

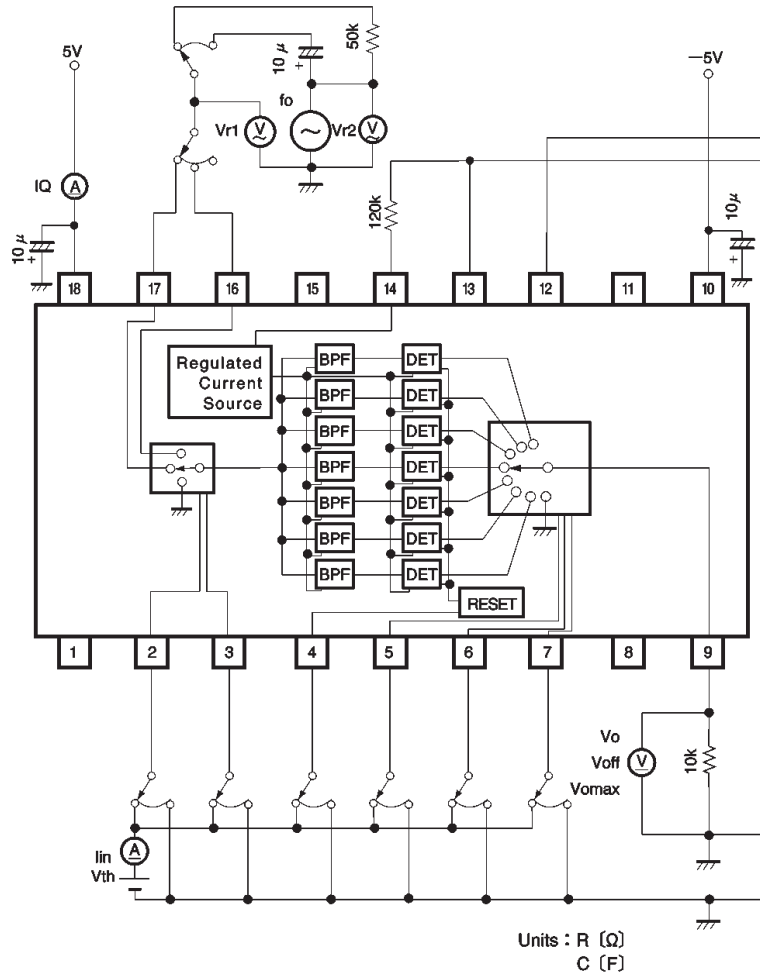
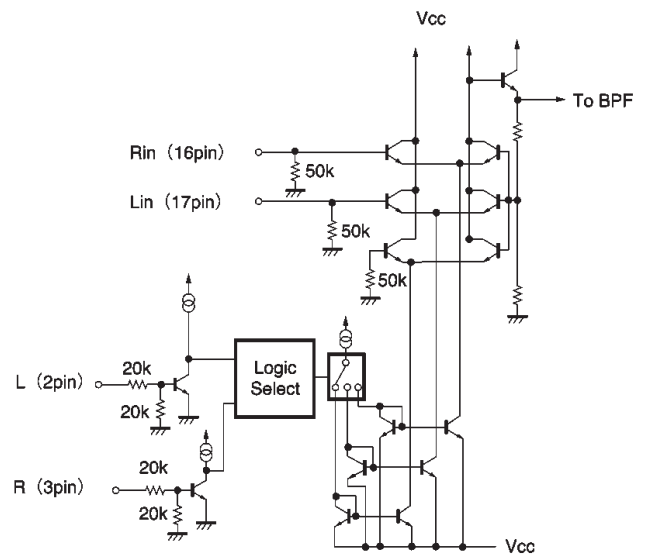


Fig. 1

● Circuit operation

(1) Input switch circuit

The BA3826S alternately switches between the left and right stereo channel signals using time division to serialize and process the signals.



The input pin biased by a 50kΩ resistor connected to ground. The control logic threshold is set at 1.4V (Typ.) (refer to the input switching logic table that follows).

Fig. 2 Equivalent circuit diagram for the input switching block.

(2) Band-pass filter circuit

This circuit extracts the required frequency range from the input signal and amplifies it.

The center frequency is determined by the value of the current flowing through the resistor connected to pin 14. Q is set to 3.5 (Typ.).

Due to the characteristics of the band-pass filter circuit, the circuit has a transition rise and fall characteristic. Due to the transition rise characteristic, five input cycles are required until peak output is reached.

When RESET is input, a built-in circuit cancels the fall transition characteristic (input the reset signal for 0.5ms).

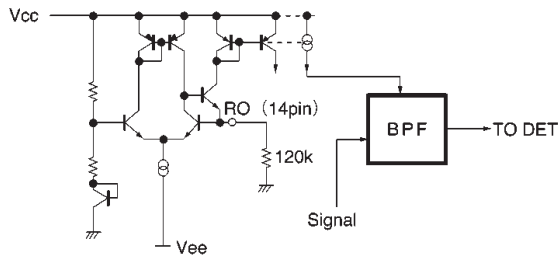


Fig. 3 Equivalent circuit diagram for the band-pass filter block.

(3) DET circuit

The DET circuit detects the signal selected by the band pass filter and performs peak hold.

The RESET Driver discharges the charge stored in the capacitor. After the RESET input is released, the RESET Driver discharges continuously for 14ms.

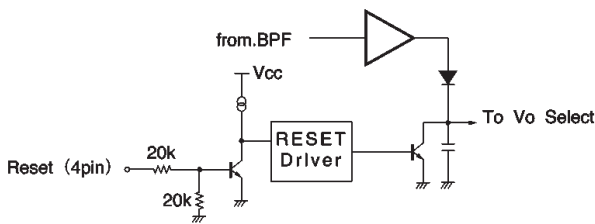
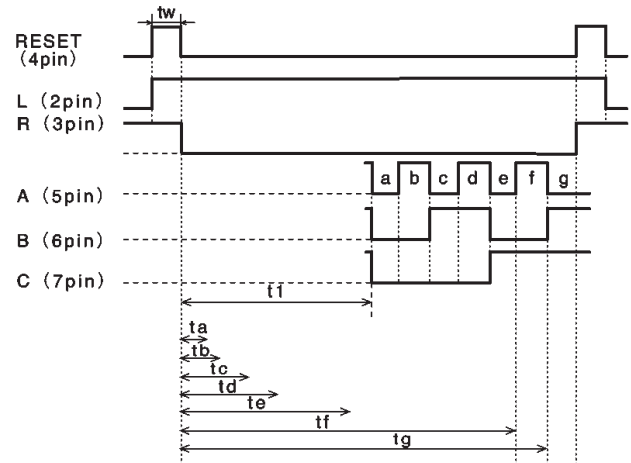


Fig. 4 Equivalent circuit diagram for the DET circuit block.

(4) Timing



t1	>	14	ms	
ta	>	0.4	ms =	5 × 1 / fo7
tb	>	1.0	ms =	5 × 1 / fo6
tc	>	2.5	ms =	5 × 1 / fo5
td	>	5.9	ms =	5 × 1 / fo4
te	>	14.7	ms =	5 × 1 / fo3
tf	>	40	ms =	5 × 1 / fo2
tg	>	98	ms =	5 × 1 / fo1
tw	>	0.5	ms	

* fo is calculated at the minimum value.

Fig. 5 Timing

1) RESET timing

The RESET input is used as the RESET signal for the band-pass filter circuit and the DET circuit. The setting time is 0.5ms min.

When performing a RESET input, disable both the Lin and Rin inputs. The synchronous shift in this case must be ±0.1ms max.

2) Output select timing

The audio input signal is not accepted when the RESET input and L (R) inputs are low. There are no particular restrictions on the select input for the various frequencies, but there are delay times until the peak voltage is settles (see (a) and (b) below). Accordingly, set the read timing for the DET signal after the longer of the delay times in (a) and (b).

(a) For the band-pass filter, a sampling time of at least 5 cycles is required due to the transition rise characteristic.

(b) For DET, after release of RESET, there is a discharge time of 14mS (Max.)
 The read enable period for Vo starts 0.5ms after the output switch logic settles.

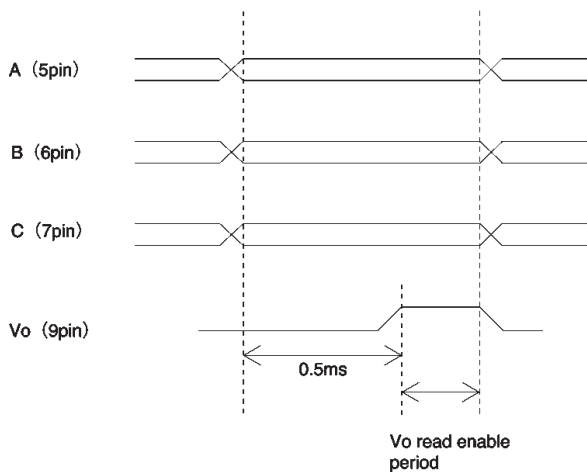


Fig. 6 Read enable timing

(5) Application example with reduced cycle time
 The transition characteristics for the band-pass filter are shown in the graph below. The time for at least 5 fo cycles is required until the DET output peaks. Therefore, the lower the frequency, the longer the time required and fo1 requires the longest time. Refer to the values given below for applications that require a shorter cycle time.
 When fo1 = 60Hz, the time requires for output > 60% is tg > 45ms.

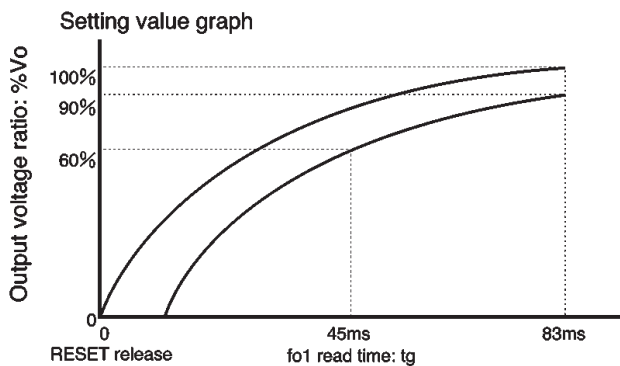


Fig. 7 fo1 read time vs. output voltage

(6) Output switch circuit
 This circuit uses time division switching to output the peak hold signal from each DET.
 Switching occurs when the control signal reaches 1.4V, and when A, B, and C are all high, output is disabled (GND level). Refer to the table below regarding the output switching logic.
 The recommended output load resistance is 10kΩ.

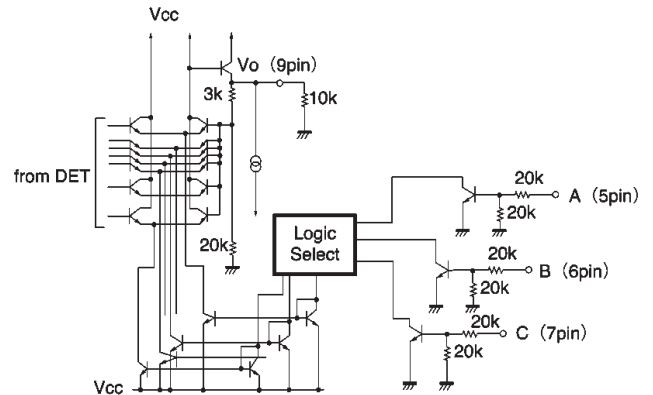


Fig. 8 Output switching circuit

(2) Frequency characteristics

The frequency characteristics for this IC are set by an external resistor. The value of this resistor for the specification conditions is 120kΩ. Use a potentiometer if you wish to set the frequency characteristics accurately.

(3) Operating voltage range

Operation of the application example circuit is guaranteed provided that the V_{CC} and V_{EE} voltages are within the specified power supply voltage range, and the ambient temperature is within the specified range. With regard to the characteristic values, the output voltage level will differ from the rated values for the specification conditions if the power supply voltage is reduced, but the inherent function of the band-pass filters is preserved.

(4) Load resistance

The various circuit characteristics in this specification sheet were measured using an output load resistance of 10kΩ. If the load resistance is too low, the I/O gain and control range vary slightly. Be aware of this when connecting the next stage.

(5) Coupling capacitors

Set the polarity of the input electrolytic coupling capacitors after establishing the electrical potential relationship with the connected input.

●Electrical characteristics curves

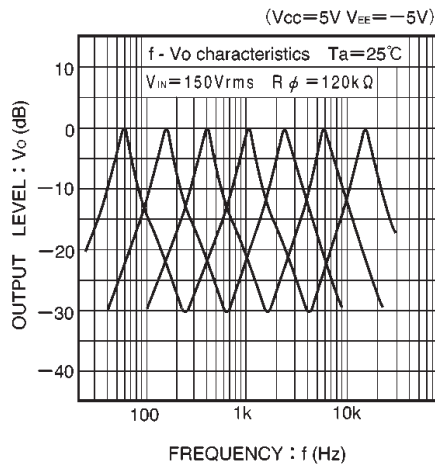


Fig. 10 Output level vs. frequency

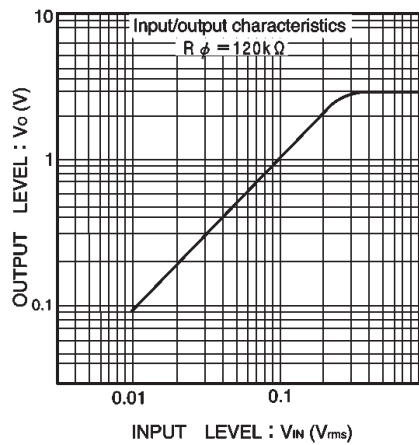


Fig. 11 Input level vs. output level

●External dimensions (Units: mm)

