General Application Guide for the HSDL-1100 4 Mb/s Infrared Transceiver

Application Note 1112

HSDL-1100 Performance Capability

Designed to Meet the IrDA Physical Layer Specification version 1.1

- Performance is guaranteed at the 1.152 Mb/s and 4.0 Mb/s data rates. The HSDL-1100 is also backward compatible to 2.4-115.2 kb/s data rates as required by the IrDA specification.
- Errorless 4 Mb/s performance at link distances of 1.3-1.95 meters has been verified using the HSDL-1100 and I/O chips such as the National Semiconductor PC87108, the VLSI VL82C147, and the SMC FDC37C957.
- Nose-to-Nose (0-5 cm) errorless performance has also been verified for an Ir link using the HSDL-1100 and I/O chips.
- Sharp ASK/DASK errorless performance on the Rxd-B channel has been verified at 38.4 kb/s using the National Semiconductor PC87108. Link distance exceeded 2 meters for typical HSDL-1100 units.
- As with the HSDL-1000, the one-piece package of the HSDL-1100 allows the Ir system designer to easily meet all IrDA viewing angle specifications.
- Switching between IrDA data rates is effortless as data is always present at one of two receiver outputs RxdA and RxdB. Rxd-A provides 2.4-115.2 kb/s data, and Rxd-B provides 0.5-4 Mb/s data.

Capable of Receiving and Transmitting Sharp ASK/DASK and TV Remote

- The Rxd-B receiver channel has been verified to correctly receive Sharp ASK/DASK 500 kHz carrier for data rates of 9.6 kb/s, 19.2 kb/s, and 38.4 kb/s. The National Semiconductor PC87108 has ASK/DASK capability on both receive pins IRRX1 and IRRX2.
- The Rxd-A receiver channel is proven capable of receiving

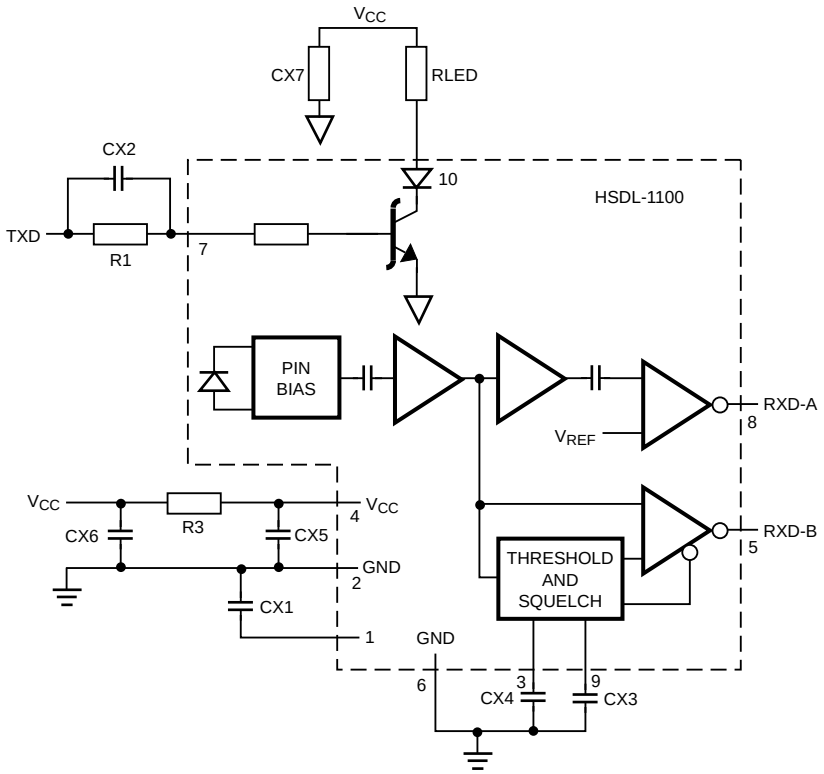


Figure 1. HSDL-1100 Application Diagram.

TV Remote signals correctly. However, the sensitivity will allow only 2-3 meters of transmit to receive distance unless the transmit power of the remote signal is >100 mW/sr.

- The HSDL-1100 transmitter is capable of correct Sharp ASK/ DASK and TV Remote data transmission at IrDA levels for transmitted intensity (mW/sr).

HSDL-1100 Functional Description

Transmitter

The transmitter uses a high speed, high efficiency TS AlGaAs LED to produce an Ir signal of intensity and speed required by IrDA. The LED drive transistor is Schottky clamped to aid in meeting the IrDA optical rise time, and pulse width specifications. The external components CX2 and R1 are recommended to obtain current peaking, which creates faster optical pulse edges. Fast optical edges will help the link meet the required IrDA power budget. LED current is set by selection of RLED. See the Transmitter Drive Requirements section.

Receiver

The receiver consists of two channels, Rxd-A (2.4-115.2 kb/s) and Rxd-B (0.5-4 Mb/s). Both channels use the same detector and pre-amplifier stage. Both channels use CX1, CX5, CX6, and R3 to filter out power supply noise. The Rxd-B channel uses an adaptive threshold circuit to minimize pulse width distortion (PWD) over the IrDA required dynamic range. The Rxd-B channel also uses a squelch circuit to eliminate noise bits on Rxd when no Ir signal is present. The adaptive threshold circuit makes use of CX3 and CX4.

In general, 2.4-115.2 kb/s Ir signals create output pulses on Rxd-A, and 0.5-4 Mb/s Ir signals create output pulses on Rxd-B. However, Ir signals in the 10 kHz - 1 MHz range may appear on both Rxd-A and Rxd-B, depending on the Ir signal strength. The presense of signal at both Rxd-A and Rxd-B should not be a problem for any properly designed I/O chip. The I/O chip should be designed to look at only one channel at a time, depending upon which data mode has been selected by the software.

Dynamic Range

The dynamic range required by IrDA for a 1 meter link is 4 µW/cm^2 500 mW/cm^2 for 2.4-115.2 kb/s, and 10 µW/cm^2-500 mW/cm^2 for 0.5-4 Mb/s. The wide dynamic range requires a special circuit which adjusts to the signal level for comparison to a threshold. The adaptive threshold circuit quickly adjusts to the incoming signal level and eliminates the need for any external AGC circuitry or adjustment.

Power Supply Noise Immunity

The HSDL-1100 receiver circuitry is specially designed for power supply noise immunity. The result of the receiver design is improved power supply noise immunity over that of the HSDL-1000. Table 1 describes the HSDL-1100 noise immunity as compared to that of the HSDL-1000.

Power Supply Noise immunity is the maximum amount of ripple or noise on V_{CC} that the receiver can tolerate without generating any bit errors. Noise levels above the noise immunity will effectively reduce the receiver sensitivity and therefore the Ir link distance. Without any infrared signal present, noise levels above the noise immunity could generate pulses on RxdA or RxdB. The worst case immunity is defined as the lowest level of noise immunity in any frequency range.

Ambient Light

The HSDL-1100 receiver design allows for the ambient light levels of sunlight, flourescent light, and incandescent light specified in the IrDA Physical Layer Specification. As with the HSDL-1000, several technologies are used in the HSDL-1100 design to reduce the effects of interfering ambient light. The package mold compound is tinted with dye to filter out light wavelengths below the Ir wavelengths of 850-900 nm. The lens of the detector is designed to focus light within the IrDA viewing angle. The pre-

Table 1.

Worst Case Immunity	HSDL-1000	HSDL-1100	
	Rxd	Rxd-A	Rxd-B
Power Supply Noise Immunity with no external V_{CC} filter or decoupling	20 mV	90 mV	70 mV
Power Supply Noise Immunity with recommended V_{CC} filter including Cx5, R3, Cx6		> 1 volt pk-pk	> 1 volt pk-pk

amplifier for both receiver channels contains daylight cancellation circuitry to eliminate the ambient light portion of incoming Ir signals.

Lead Bend Options
Lead bend options for the HSDL-1100 include the TOP (#X08 option), and FRONT (#X07 option). The TOP and FRONT options are similar to that shown on page 13 of the Hewlett-Packard IrDA Design Guide, and are shown in detail on the HSDL-1100 datasheet. The TOP option lies flat on the circuit board, while the FRONT stands upright on the circuit board.

Implementation of the HSDL-1100

Required External Components
Table 2 describes the external components required for obtaining datasheet performance (Actual values for the components may vary with the I/O chip, controller chip, EnDec chip, or buffer chip that the HSDL-1100 interfaces to).

Board Layout Requirements
Proper board layout is crucial to the noise immunity of the overall Ir system. Compromised board layout may lead to reduced sesitivity, and therefore shorter achievable Ir link distance. Proper board layout is descibed in detail in page 16 of the Hewlett-Packard IrDA Design Guide.

Keys aspects of proper board layout are:

- V_{CC} to Gnd bypass capacitor CX5 should be placed within 0.5 cm of the HSDL-1100 module pins 2,4, AND on the same side of the PC board as the HSDL-1100 module.
- The PIN bypass capacitor CX1 should be <0.5 cm from pin 1 of the HSDL-1100 module.
- A multi-layer PC board should be used, and one layer devoted to a ground plane for the HSDL-1100 module. The ground plane should be laid out as an island, with one connection to a clean (<20 mV noise) system ground or analog system ground, and separated from the ground connection of fast switching devices, or noise sources.
- The board underneath and 1 cm in any direction around the module is defined as the

Table 2.

Component	Description	Recommended Value
R1	Txd input resistor for transmitter peaking.	560 Ω ±5%, 0.125 watt
RLED (R2)	LED bias resistor which sets LED current pulse amplitude.	4.7 Ω ±5%, 0.5 watt (See Transmitter Drive Requirements Section)
R3	Power supply noise filter resistor. The higher the value, the lower the minimum filter frequency. 1/(R3•CX5) is the minimum filter frequency.	10-50 Ω ±5%, 0.125 watt
CX1	PIN bypass capacitor to reduce noise at the PIN detector.	0.47 µF, ±10%, X7R ceramic, <0.5 cm from pin 1.
CX2	Txd input capacitor for transmitter peaking.	220 pF, ±10%, X7R ceramic
CX3	Adaptive threshold capacitor.	1000 pF, ±10%, X7R ceramic
CX4	Adaptive threshold averaging capacitor.	0.010 µF, ±10%, X7R ceramic
CX5	V_{CC} to Gnd bypass capacitor. Should be within 0.5 cm of module pins 2,4.	0.47 µF, ±20%, X7R ceramic, <0.5 cm lead length, within 0.5 cm from pins 2, 4.
CX6	V_{CC} to Gnd bypass capacitor.	6.8 µF, Tantalum. Larger value recommended for noisy supplies or environments.
CX7	V_{CC} transmitter bypass capacitor	0.47 µF, ceramic. Used to eliminate ripple on V_{CC} caused by the LED current during infrared transmission.

critical ground plane zone. The board layer chosen as the ground plane island should be maximized in area within the ground plane zone, and should include all resistor and capacitor components recommended for use with the HSDL-1100.

- The ground plane for the HSDL-1100 module should be connected ONLY to the least noisy ground node available on the PC board.
- The DC-DC converter should be located as far away from the HSDL-1100 on the PC board as possible (at least 3 cm away). The board may then look like Figure 2.

If any of the above aspects of board layout are compromised, and it is suspected that an EMI shield over the HSDL-1100 may be necessary, Hewlett-Packard can provide EMI shields, or shielded HSDL-1100s in production volumes. The PC board should be prepared with the proper through holes, if it is suspected that an EMI shield will be necessary (see datasheets for HP part numbers HSDL-810x, or HSDL-1100#S07).

Application Specific Transmitter Design:

Transmitter Drive

The infrared LED in the HSDL-1100 is driven by signals present at TXD. See Figure 3.

The IrDA physical layer specification requires t_{rise} and t_{fall} of the transmitted optical signal at 4 Mb/s to be 40 ns or less. The HSDL-1100 budgets 30 ns of t_{rise} and t_{fall} for the LED, and 10 ns for t_{rise} and t_{fall} of the electrical ILED pulse. In order to reach < 30 ns t_{rise} and t_{fall} for the LED, a peaking circuit of R1 and CX2 is recommended. The R1•CX2 time constant provides overdrive for both turn-on and turn-off of the LED, shortening the optical t_{rise} and t_{fall}. In order to limit the electrical ILED pulse t_{rise} and t_{fall} to 5-10 ns, TXD must be driven with a pulse current Iih of approximately ILED/125. See Figure 4.

The HSDL-1100 datasheet Electrical Specifications show that at Vih = 4.25 V, the required Iih ≤6.6 mA. Using R1 = 560 ohms, Iih will be sufficient for 5-10ns t_{rise} and t_{fall} of ILED, if Vih ≥4.25 V. If the chosen I/O chip, controller chip, or EnDec chip does not support Vih ≥ 4.25 V at the required Iih, then R1 and CX2 can be chosen to allow for a lower Vih at the required Iih value. R1 can be lowered from 560 ohms to allow for Vih < 4.25 V. CX2 should then be increased to preserve the peaking characteristic.

If the I/O chip or controller chip cannot provide the required Iih even at Voh = 2.4 V, then a buffer chip can be used to drive TXD of the HSDL-1100. The output of the buffer chip should be able to source current of at least

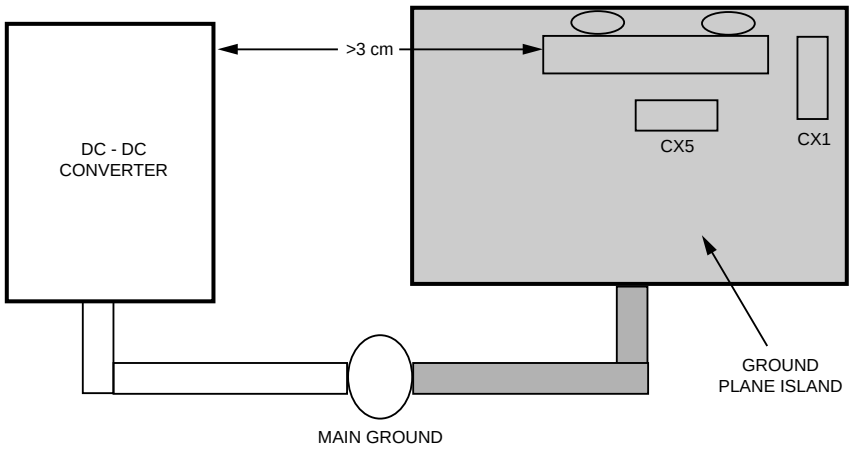


Figure 2.

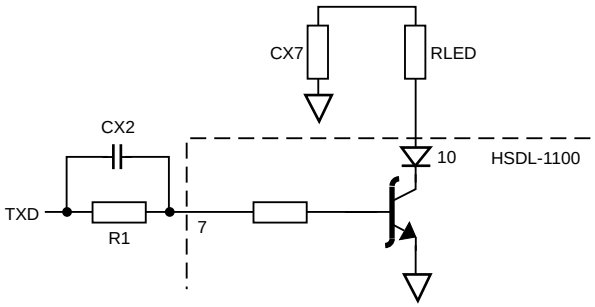


Figure 3.

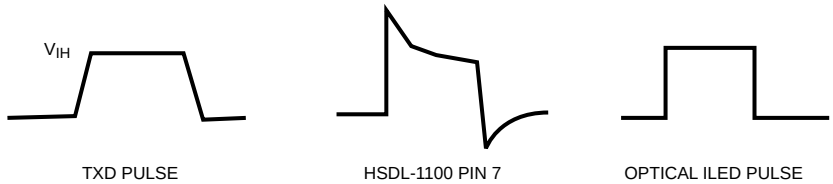


Figure 4.

IOH = 6 mA in magnitude. LS/HC241 and LS/HC244 are buffer chips that can be used to drive the TXD of the HSDL-1100.

Heat Dissipation for LEDA
The PC board must be designed to dissipate heat from the HSDL-1100's LED. The junction temperature of the LED should be kept below 125°C. The thermal resistance of the PC board can be minimized in order to keep $T_{junction}$ of the LED below 125°C while operating up to 660 mA. For typical applications, the LEDA pin 10 trace should be at least 38 mm^2 in area and no narrower than 2.5 mm at any point. Such a trace should provide a thermal resistance of approximately 100°C/Watt. The HSDL-1100 evaluation board presents a thermal resistance of approximately 100°C/Watt for the LEDA pin 10 trace. An opening in the solder mask for the whole trace can be made to further decrease the thermal resistance.

If you do not know your PC board's thermal resistance (deg C/Watt), then the easiest way to determine the maximum allowable LED current is from maximum pin 10 = LEDA case temperature, see Table 5. From the LED current table you can see the maximum pin10 lead temperature on the HSDL-1100 for the #007 leadform. A thermacouple can be placed on pin10 while operating the HSDL-1100 transmitter in their PC board. If the pin 10 temperature exceeds the listed maximum temperature, the PC board thermal resistance must be reduced, or the LED current must be reduced. The PC board thermal resistance can be reduced by increasing the metal area of the pin10 trace on the PC board, and by leaving it bare (no epoxy glass over a section of that trace).

For Example: If ILED = 550 mA, then the PC board should be designed so that the pin10 temperature does not exceed 92.1°C when the PC board is enclosed in a notebook or handy terminal box.

Table 3. Recommended Minimum Iih for a chosen ILED pulse amplitude.

ILED Pulse Amplitude (mA)	Recommended Minimum Iih (mA)
400	3.2
500	4.0
600	4.8
660	5.3

Table 4. Electrical Specifications.

Minimum Vih (V)	R1 (Ω)	CX2 (pF)
4.25	560	220
3.5	420	300
2.4	220	560

Table 5. LED Current

LED Current Amplitude (25% duty cycle) (mA)	Maximum Pin 10 (Case) Temperature for the HSDL-1100 (degrees C)
400	101.3
450	98.4
500	95.3
550	92.1
600	88.7
660	83.0

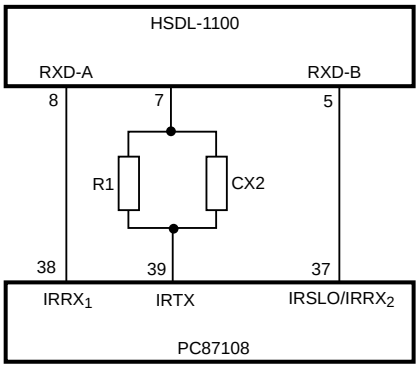
Interface to Recommended I/O Chips

4 Mb/s Ir link distances of 1.3-1.95 meters between transmitter and receiver have been demonstrated using typical HSDL-1100 units, and either the National Semiconductor PC87108 I/O chip, the VLSI VL82C147 I/O chip, or the SMC FDC37C957 I/O chip. In reference to the HSDL-1100 diagram on page 1 of this note, the TXD, RXD-A, and RXD-B nodes can be connected directly to the chosen I/O chip.

National Semiconductor PC87108

For the National Semiconductor PC87108 I/O chip, the Ir link can be realized with the following connections:
Connect IRTX pin 39 of the PC87108 to the I/O side of R1/CX2 labeled TXD on the diagram of page 1.

Connect IRRX1 pin 38 of the PC87108 to RXD-A (pin 8 of the HSDL-1100).

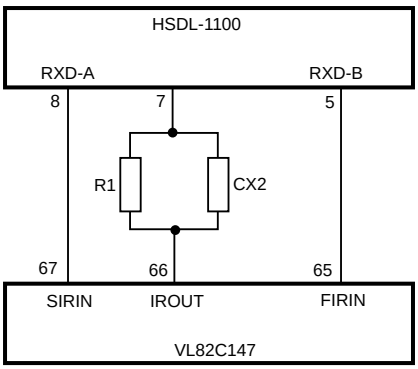


Connect IRSLO/IRRX2 pin 37 of the PC87108 to RXD-B (pin 5 of the HSDL-1100).

For Sharp ASK/DASK using the NS PC87108, the PC87108 should be configured by the ASK/DASK software to:
1. Receive data from only one receive pin
2. Set the receive to the AUX input IRRX2

VLSI VL82C147
For the VLSI VL82C147 I/O chip, the Ir link can be realized with the following connections:

Connect IROUT pin 66 of the VL82C147 to the I/O side of R1/CX2 labeled TXD on the HSDL-1100 diagram.

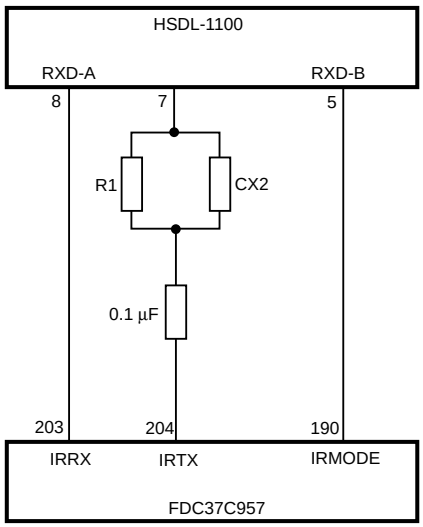


Connect SIRIN pin 67 of the VL82C147 to RXD-A (pin 8 of the HSDL-1100).

Connect FIRIN pin 65 of the VL82C147 to RXD-B (pin 5 of the HSDL-1100).

SMC FDC37C957
For the SMC FDC37C957 I/O chip, the Ir link can be realized with the following connections:

Connect IRTX pin 204 of the FDC37C957 to the 0.1 µF capacitor connected to R1/CX2 of the HSDL-1100 diagram.



Connect IRRX pin 203 of the FDC37C957 to RXD-A (pin 8 of the HSDL-1100).

Connect IRMODE pin 190 of the FDC37C957 to RXD-B (pin 5 of the HSDL-1100).

CX3 must be 1000 pF in the application circuit (other I/O chips use 4700 pF).

Note that the 0.1 µF capacitor connected to the transmit line is necessary since the SMC I/O chip IRTX pin could be left in a logic high state for an indeterminate period of time. Connection of the IRTX directly to R1/CX2 would damage the HSDL-1100's LED if the IRTX line was left in the logic high state.

Software Recommendations
Please see page 24 in the Hewlett-Packard IrDA Design Guide.

Microsoft (Windows 95) or PUMA Technology are the most likely vendors to have released 4Mb/s Ir software.

Evaluation Boards
HSDL-1100 FRONT lead form evaluation boards can be obtained from your Hewlett-Packard Sales Representative. The evaluation boards can be plugged into a standard 6-8 pin edge connector, or hard-wired via cable to your Ir system's I/O chip. The connection to the I/O chip should be as shown above in the Interface to Recommended I/O Chips section of this note. Both V_{CC} pins can be connected to the same power supply, or separate supplies as desired. The ground pin should be connected to the most noise free ground on the system board.

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