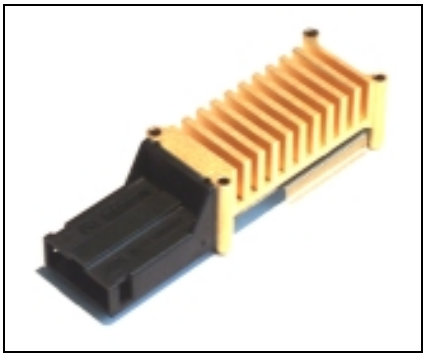
Parallel Optical Link: PAROLI® Tx AC, 1.25 Gbit/s — V23814-K1306-M136

Parallel Optical Link: PAROLI® Rx AC, 1.25 Gbit/s — V23815-K1306-M136



Features

- Power supply 3.3 V
- Multistandard differential signal electrical interface
- 12 electrical data channels
- Asynchronous, AC-coupled optical link
- 12 optical data channels
- Transmission data rate of up to 1250 Mbit/s per channel, total link data rate up to 15 Gbit/s
- 850 nm VCSEL array technology
- PIN diode array technology
- 62.5 µm graded index multimode fiber ribbon
- MT based optical port
- SMD technology
- OIF[1)] compliant
- IEC Class 1 laser safety compliant
- GBE mask compliant

Optical Port

- Designed for the Simplex MT Connector (SMC)
- Port outside dimensions: 15.4 mm x 6.8 mm (width x height)
- MT compatible (IEC 61754-5) fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Alignment pins fixed in module port
- Integrated mechanical keying
- Process plug (SMC dimensions) included with every module

1) OIF-VSR4-01.0 Implementation Agreement (VSR OC-192/STM-64)

Features of the Simplex MT Connector (SMC)

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule (IEC 61754-5)
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Snap-in mechanism
- Ferrule bearing spring loaded
- Integrated mechanical keying

Applications

Telecommunication

- Switching equipment
- Access network

Data Communication

- Interframe (rack-to-rack)
- Intraframe (board-to-board)
- On board (optical backplane)

Pin Configuration

The numbering conventions for the Tx and Rx modules are the same.

Numbering Conventions Transmitter/Receiver

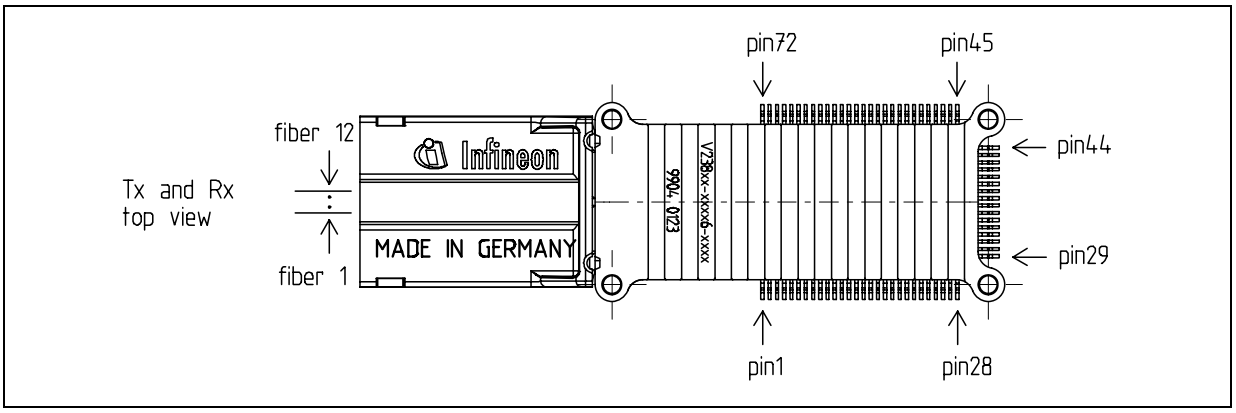


Figure 1

Pin Description Transmitter

Pin No.	Symbol	Level/ Logic	Description
1	V_{CC}		Power supply voltage of laser driver
2	t.b.l.o.		to be left open
3	t.b.l.o.		to be left open
4	t.b.l.o.		to be left open
5	t.b.l.o.		to be left open
6	LCU	LVCMOS Out	Laser Controller Up High = normal operation Low = laser fault or –RESET low
7	V_{EE}		Ground
8	V_{IN}		Input V_{IN} rail CML: V_{IN} = Reference supply (e.g. V_{CC}) LVPECL, LVDS: V_{IN} = V_{EE}
9	t.b.l.o.		to be left open
10	t.b.l.o.		to be left open
11	V_{EE}		Ground
12	V_{EE}		Ground
13	DI01N	Data In	Data Input #1, inverted
14	DI01P	Data In	Data Input #1, non-inverted

Pin Description Transmitter (cont'd)

Pin No.	Symbol	Level/ Logic	Description
15	V_{EE}		Ground
16	V_{EE}		Ground
17	DI02N	Data In	Data Input #2, inverted
18	DI02P	Data In	Data Input #2, non-inverted
19	V_{EE}		Ground
20	V_{EE}		Ground
21	DI03N	Data In	Data Input #3, inverted
22	DI03P	Data In	Data Input #3, non-inverted
23	V_{EE}		Ground
24	V_{EE}		Ground
25	t.b.l.o.		to be left open
26	DI04N	Data In	Data Input #4, inverted
27	DI04P	Data In	Data Input #4, non-inverted
28	V_{EE}		Ground
29	DI05N	Data In	Data Input #5, inverted
30	DI05P	Data In	Data Input #5, non-inverted
31	V_{EE}		Ground
32	V_{EE}		Ground
33	DI06N	Data In	Data Input #6, inverted
34	DI06P	Data In	Data Input #6, non-inverted
35	V_{EE}		Ground
36	V_{EE}		Ground
37	DI07N	Data In	Data Input #7, inverted
38	DI07P	Data In	Data Input #7, non-inverted
39	V_{EE}		Ground
40	V_{EE}		Ground
41	DI08N	Data In	Data Input #8, inverted
42	DI08P	Data In	Data Input #8, non-inverted
43	V_{EE}		Ground
44	V_{EE}		Ground
45	V_{EE}		Ground
46	DI09N	Data In	Data Input #9, inverted
47	DI09P	Data In	Data Input #9, non-inverted
48	t.b.l.o.		to be left open

Pin Description Transmitter (cont'd)

Pin No.	Symbol	Level/ Logic	Description
49	V_{EE}		Ground
50	V_{EE}		Ground
51	DI10N	Data In	Data Input #10, inverted
52	DI10P	Data In	Data Input #10, non-inverted
53	V_{EE}		Ground
54	V_{EE}		Ground
55	DI11N	Data In	Data Input #11, inverted
56	DI11P	Data In	Data Input #11, non-inverted
57	V_{EE}		Ground
58	V_{EE}		Ground
59	DI12N	Data In	Data Input #12, inverted
60	DI12P	Data In	Data Input #12, non-inverted
61	V_{EE}		Ground
62	V_{IN}		V_{IN} rail CML: V_{IN} = Reference supply (e.g. V_{CC}) LVPECL, LVDS: V_{IN} = V_{EE}
63	t.b.l.o.		to be left open
64	–RESET	LVCMOS In	High = laser diode array is active Low = switches laser diode array off This input has an internal pull-down to ensure laser safety switch off in case of unconnected –RESET input
65	V_{EE}		Ground
66	V_{EE}		Ground
67	LE	LVCMOS In	Laser ENABLE. High active. High = laser array is on if –LE is also active. Low = laser array is off. This input has an internal pull-up, therefore can be left open.
68	–LE	LVCMOS In	Laser ENABLE. Low active. Low = laser array is on if LE is also active. This input has an internal pull-down, therefore can be left open.
69	t.b.l.o.		to be left open
70	t.b.l.o.		to be left open
71	t.b.l.o.		to be left open
72	V_{CC}		Power supply voltage of laser driver

Pin Description Receiver

Pin No.	Symbol	Level/ Logic	Description
1	V_{EE}		Ground
2	V_{CC}		Power supply voltage of preamplifier and analog circuitry
3	V_{CC}		Power supply voltage of preamplifier and analog circuitry
4	t.b.l.o.		to be left open
5	OEN	LVCMOS In	Output Enable High = normal operation Low = sets all Data Outputs to low This input has an internal pull-up which pulls to high level when this input is left open
6	SD1	LVCMOS Out	Signal Detect on fiber #1. High = signal of sufficient AC power is present on fiber #1 Low = signal on fiber #1 is insufficient.
7	V_{CCO}		Power supply voltage of output stages
8	V_{EE}		Ground
9	t.b.l.o.		to be left open
10	V_{EE}		Ground
11	V_{EE}		Ground
12	V_{EE}		Ground
13	DO01P	LVDS Out	Data Output #1, non-inverted
14	DO01N	LVDS Out	Data Output #1, inverted
15	V_{EE}		Ground
16	V_{EE}		Ground
17	DO02P	LVDS Out	Data Output #2, non-inverted
18	DO02N	LVDS Out	Data Output #2, inverted
19	V_{EE}		Ground
20	V_{EE}		Ground
21	DO03P	LVDS Out	Data Output #3, non-inverted
22	DO03N	LVDS Out	Data Output #3, inverted
23	V_{EE}		Ground
24	V_{EE}		Ground
25	t.b.l.o.		to be left open

Pin Description Receiver (cont'd)

Pin No.	Symbol	Level/ Logic	Description
26	DO04P	LVDS Out	Data Output #4, non-inverted
27	DO04N	LVDS Out	Data Output #4, inverted
28	V_{EE}		Ground
29	DO05P	LVDS Out	Data Output #5, non-inverted
30	DO05N	LVDS Out	Data Output #5, inverted
31	V_{EE}		Ground
32	V_{EE}		Ground
33	DO06P	LVDS Out	Data Output #6, non-inverted
34	DO06N	LVDS Out	Data Output #6, inverted
35	V_{EE}		Ground
36	V_{EE}		Ground
37	DO07P	LVDS Out	Data Output #7, non-inverted
38	DO07N	LVDS Out	Data Output #7, inverted
39	V_{EE}		Ground
40	V_{EE}		Ground
41	DO08P	LVDS Out	Data Output #8, non-inverted
42	DO08N	LVDS Out	Data Output #8, inverted
43	V_{EE}		Ground
44	V_{EE}		Ground
45	V_{EE}		Ground
46	DO09P	LVDS Out	Data Output #9, non-inverted
47	DO09N	LVDS Out	Data Output #9, inverted
48	t.b.l.o.		to be left open
49	V_{EE}		Ground
50	V_{EE}		Ground
51	DO10P	LVDS Out	Data Output #10, non-inverted
52	DO10N	LVDS Out	Data Output #10, inverted
53	V_{EE}		Ground
54	V_{EE}		Ground
55	DO11P	LVDS Out	Data Output #11, non-inverted
56	DO11N	LVDS Out	Data Output #11, inverted
57	V_{EE}		Ground
58	V_{EE}		Ground

Pin Description Receiver (cont'd)

Pin No.	Symbol	Level/ Logic	Description
59	DO12P	LVDS Out	Data Output #12, non-inverted
60	DO12N	LVDS Out	Data Output #12, inverted
61	V_{EE}		Ground
62	V_{EE}		Ground
63	V_{EE}		Ground
64	t.b.l.o.		to be left open
65	V_{EE}		Ground
66	V_{CCO}		Power supply voltage of output stages
67	–SD12	LVCMOS Out low active	Signal Detect on fiber #12. Low = signal of sufficient AC power is present on fiber #12. High = signal on fiber #12 is insufficient.
68	ENSD	LVCMOS In	Enable Signal Detect High = SD1 and SD12 function enabled Low = SD1 and SD12 are set to permanent active. This input has an internal pull-up which pulls to high level when this input is left open
69	t.b.l.o.		to be left open
70	V_{CC}		Power supply voltage of preamplifier and analog circuitry
71	V_{CC}		Power supply voltage of preamplifier and analog circuitry
72	V_{EE}		Ground

Description

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI system consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module.The transmitter supports LVDS, CML and LVPECL differential signals. The receiver module is described for the LVDS electrical output only. A specification for Infineon's adjustable CML output can be provided separately.

Transmitter V23814-K1306-M136

The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Multistandard Differential Signals (LVDS compatible; they also support LVPECL and CML because of the wide common input range). The electrical interface (LVDS, LVPECL or CML) is selected by the supply inputs V_{IN}. The data rate is up to 1250 Mbit/s for each channel.The transmitter module's min. data rate of 500 Mbit/s is specified for the CID[1)] worst case pattern (disparity 72) or any pattern with a lower disparity.

A logic low level at –RESET switches all laser outputs off. During power-up –RESET must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3.135 V level.

The Laser Controller Up (LCU) output is low if a laser fault is detected or –RESET is forced to low.

All non data signals have LVCMOS levels.

Transmission delay of the PAROLI system is ≤ 1 ns for the transmitter, ≤ 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

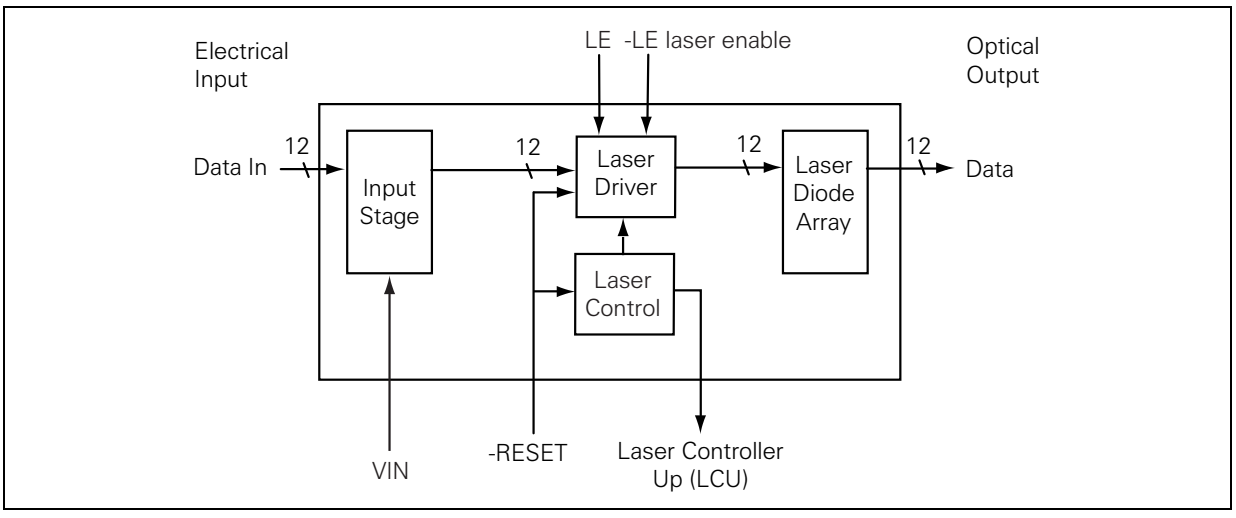


Figure 2 Transmitter Block Diagram

[1)] Consecutive Identical Digit (CID) immunity test pattern for STM-N signals. ITU-T recommendation G.957 sec. II.

Receiver V23815-K1306-M136

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, transimpedance amplifiers, and gain amplifiers. There are two different modules available for LVDS and Infineon's adjustable CML output. This description only refers to a module with LVDS output. A module description for CML output can be provided separately.

The data rate is up to 1250 Mbit/s for each channel. The receiver module's min. data rate of 500 Mbit/s is specified for the CID[1)] worst case pattern (disparity 72) or any pattern with a lower disparity.

Additional Signal Detect outputs (SD1 active high / SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.

A logic low at LVDS Output Enable (OEN) sets all data outputs to logic low. SD outputs will not be effected.

All non data signals have LVCMOS levels.

Transmission delay of the PAROLI system is at a maximum 1 ns for the transmitter, 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

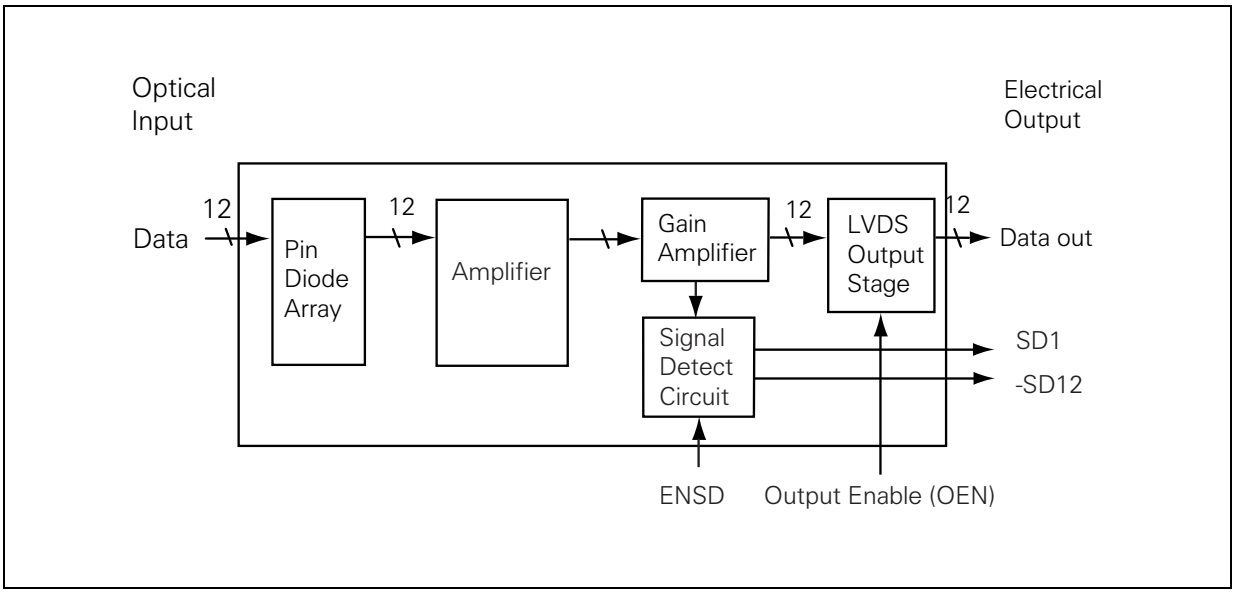


Figure 3 Receiver Block Diagram

[1)] Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

Laser Safety

The transmitter of the AC coupled Parallel Optical Link (PAROLI) is an IEC 60825-1 Amend.2 Class 1 laser product. It complies with FDA performance standards (21 CFR 1040.10 and 1040.11) for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

The PAROLI module must be operated under the specified operating conditions (supply voltage can be adjusted between 3.0 V and 3.6 V) under any circumstances to ensure laser safety.

Attention: Class 1 Laser Product

Note: Any modification of the module will be considered an act of "manufacturing", and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).

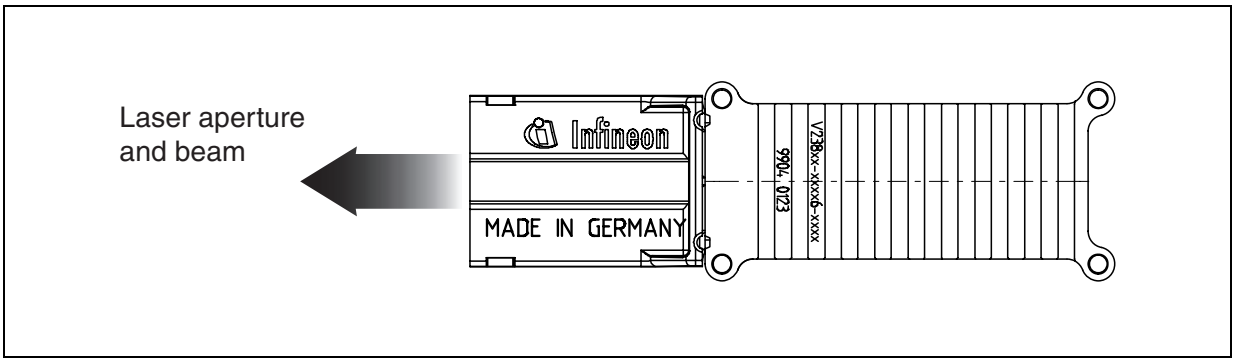


Figure 4 Laser Emission

Laser Safety Design Considerations

To ensure laser safety for all input data patterns each channel is controlled internally and will be switched off if the laser safety limits are exceeded.

A channel alerter switches the respective data channel output off if the input duty cycle permanently exceeds 57%. The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.

The minimum alerter response time is 1 µs with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1 µs, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.

All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

Technical Data

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply Voltage	V_{CC}–V_{EE}	–0.3	4.5	V
Data/Control Input Levels[1]	V_{IN}	–0.5	V_{CC}+0.5	
Data Input Differential Voltage[2]	$\|V_{ID}\|$		2.0	
Operating Case Temperature[3]	T_{CASE}	0	80	°C
Storage Ambient Temperature	T_{STG}	–20	100	
Operating Moisture		20	85	%
Storage Moisture		20	85	
ESD Resistance (all pins to V_{EE}, human body model)[4]			1	kV

[1] At Data and LVCMOS inputs.
[2] $|V_{ID}|$ = |(input voltage of non-inverted input minus input voltage of inverted input)|.
[3] Measured at case temperature reference point (see Package Outlines **Figure 15**).
[4] To avoid electrostatic damage, handling cautions similar to those used for MOS devices must be observed.

Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Transmitter					
Power Supply Voltage	V_{CC}	3.135		3.6	V
Noise on Power Supply[1]	N_{PS1}			50	mV
Noise on Power Supply[2]	N_{PS2}			100	
Data Input Voltage Range[3] [4]	V_{DATAI}	500		V_{CC}	
Data Input Differential Voltage[4] [5]	$\|V_{ID}\|$	80		1000	
Data Input Skew[6]	t_{SPN}			0.5 x t_R, t_F	ps
Data Input Rise/Fall Time[7]	t_R, t_F	50		400	
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0		V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}		0.8	
LVCMOS Input Rise/Fall Time[8]	t_R, t_F			20	ns
Receiver					
Power Supply Voltage	V_{CC}	3.0		3.6	V
Noise on Power Supply[1]	N_{PS1}			50	mV
Noise on Power Supply[2]	N_{PS2}			100	
Differential LVDS Termination Impedance	R_t	80		120	Ω
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0		V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}		0.8	
LVCMOS Input Rise/Fall Time[8]	t_R, t_F			20	ns
Optical Input Rise/Fall Time[9]	t_R, t_F			400	ps
Input Extinction Ratio	ER	6.0			dB
Input Center Wavelength	λ_C	830		860	nm

Voltages refer to V_{EE} = 0 V.

1) Noise frequency is 1 kHz to 10 MHz. Voltage is peak-to-peak value.
2) Noise frequency is > 10 MHz. Voltage is peak-to-peak value.
3) This implies that the input stage can be AC coupled.
4) Level diagram: see **Figure 5**
5) $|V_{ID}|$ = |(input voltage of non-inverted input minus input voltage of inverted input)|.
6) Skew between positive and negative inputs measured at 50% level.
7) 20% - 80% level.
8) Measured between 0.8 V and 2.0 V.
9) 20% - 80% level. Non filtered values.

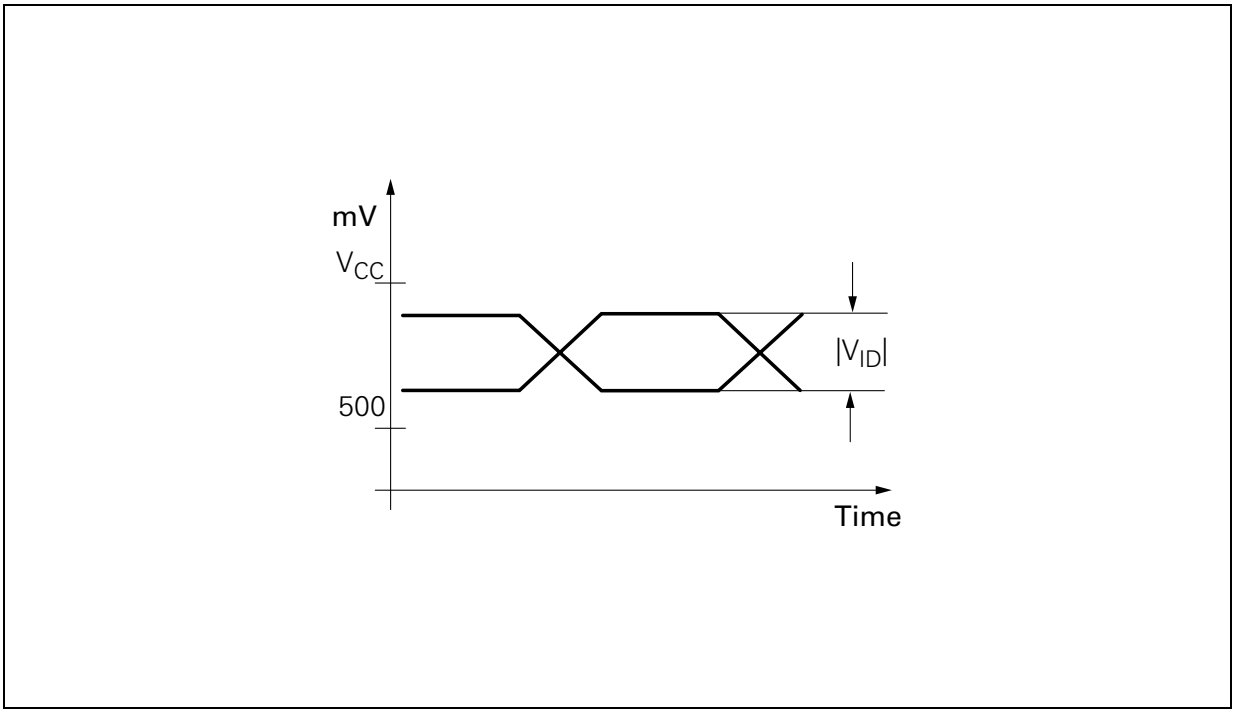


Figure 5 Input Level Diagram

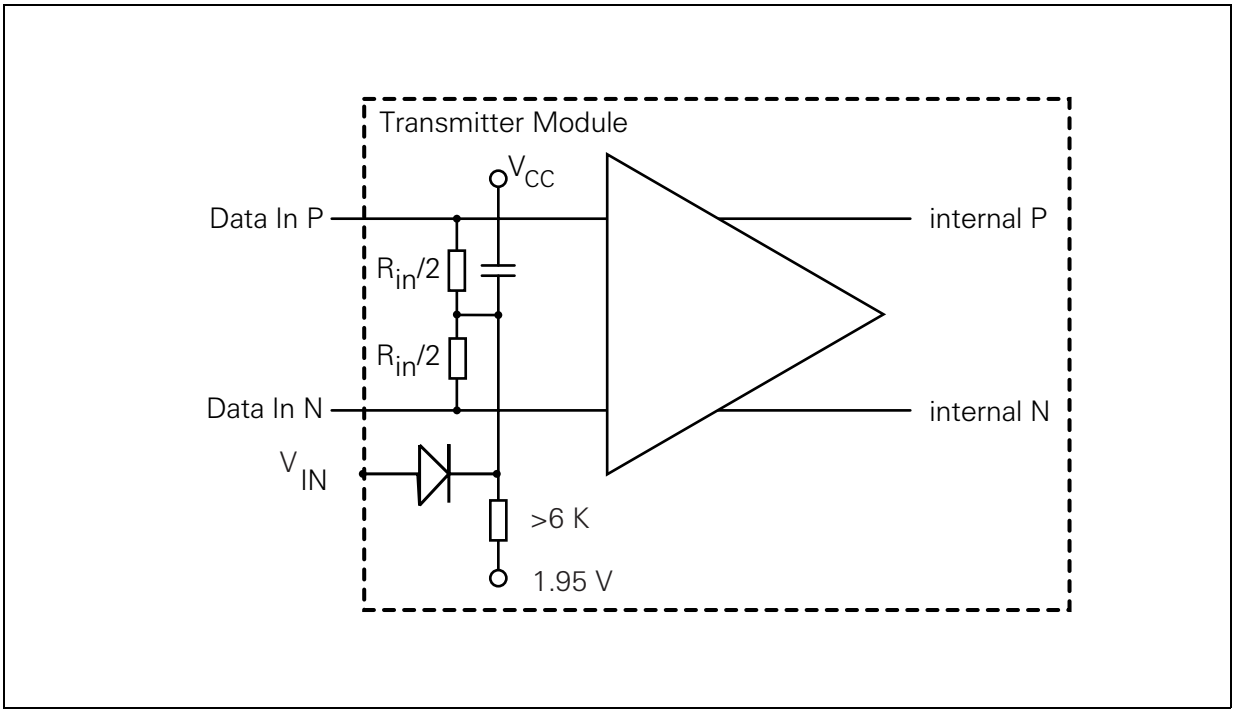


Figure 6 Input Stage

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Transmitter Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply Current	I_{CC}		350	450	mA
Power Consumption	P		1.2	1.6	W
Data Rate per Channel	DR	500[1)]		1250	Mbit/s
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			0.4	V
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2.5			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output Current High[2)]	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low[3)]	$I_{LVCMOSOL}$			4.0	
Data Differential Input Impedance[4)]	R_{IN}	80		120	Ω
Data Input Differential Current	$\|I_I\|$			5.5	mA

1) Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
2) Source current.
3) Sink current.
4) Data input stage.

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Optical Rise Time[1)]	t_R			200	ps
Optical Fall Time[1)]	t_F			200	
Total Jitter[2)]	J_T			0.284	UI
Deterministic Jitter	J_D			0.1	
Channel-to-channel skew[3)]	t_{CSK}			100	ps
Launched Average Power	P_{AVG}	–9.0	–5.0	–3.0	dBm
Launched Power Shutdown	P_{SD}			–30.0	
Center Wavelength	λ_C	830		860	nm
Spectral Width (FWHM)	$\Delta\lambda$			2	
Spectral Width (rms)	$\Delta\lambda$			0.85	
Relative Intensity Noise	RIN			–117	dB/Hz
Extinction Ratio (dynamic)	ER	6.0			dB
Optical Modulation Amplitude[4)]	OMA	0.15[5)]	0.46[6)]		mW
Eye mask compliance			GBE[7)]		

Optical parameters valid for each channel.

1) 20% - 80% level, non filtered values.
2) Measured using a filter as defined in IEEE 802.3 (2000-edition) Gigabit Ethernet specification, section 38.6.5.
3) With input channel-to-channel skew 0 ps and a maximum data channel-to-channel average deviation and swing deviation of 5%.
4) Peak to peak values.
5) Corresponds to a minimum extinction ratio of 6 dB.
6) Corresponds to a typical extinction ratio of 8 dB.
7) IEEE 802.3, sec. 38.6.5.

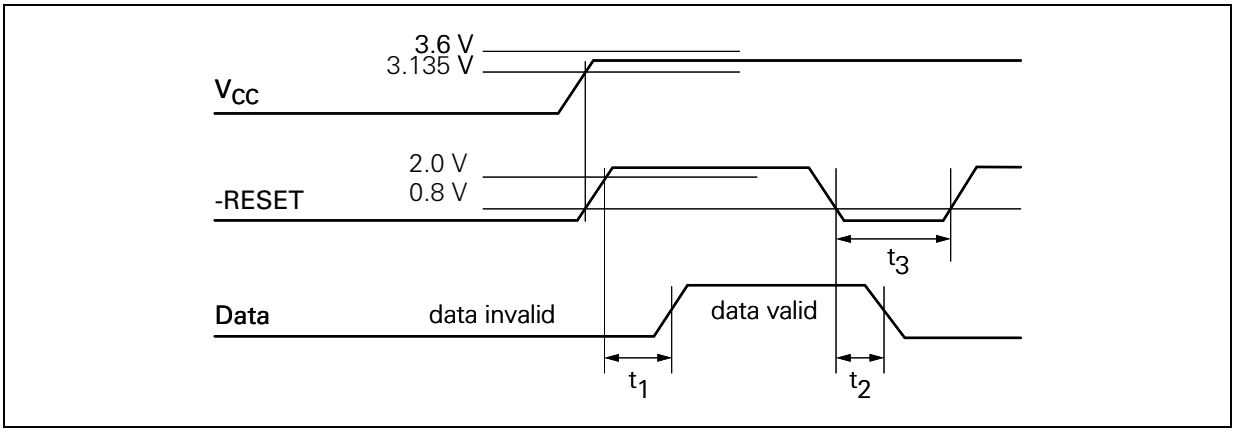


Figure 7 Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
–RESET on Delay Time	t_1		100	ms
–RESET off Delay Time	t_2		50	µs
–RESET Low Duration[1)]	t_3	10		

1) Only when not used as power on reset. At any failure recovery, –RESET must be brought to low level for at least t_3.

Receiver Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply Current	I_{CC}		250	350	mA
Power Consumption	P		0.8	1.3	W
LVDS Output Low Voltage[1), 2)]	V_{LVDSOL}	925			mV
LVDS Output High Voltage[1), 2)]	V_{LVDSOH}			1475	
LVDS Output Differential Voltage[1), 2), 3)]	$\|V_{OD}\|$	250		400	
LVDS Output Offset Voltage[1), 2), 4)]	V_{OS}	1125		1275	
LVDS Rise/Fall Time[5)]	t_R, t_F			400	ps
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2500			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output Current High[6)]	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low[7)]	$I_{LVCMOSOL}$			4.0	
Total Jitter[8), 9)]	J_T			0.332	UI
Deterministic Jitter[8)]	J_D			0.08	
Channel-to-channel skew[10)]	t_{CSK}			100	ps

1) Level Diagram: see **Figure 8**
2) LVDS output must be terminated differentially with R_t.
3) $|V_{OD}|$ = |(output voltage of non-inverted output minus output voltage of inverted output)|.
4) V_{OS} = 1/2 (output voltage of inverted output + output voltage of non-inverted output).
5) Measured between 20% and 80% level with a maximum capacitive load of 5 pF.
6) Source current.
7) Sink current.
8) With no optical input jitter.
9) At sensitivity limit of 0.028 mW OMA.
10) With input channel-to-channel skew 0 ps.

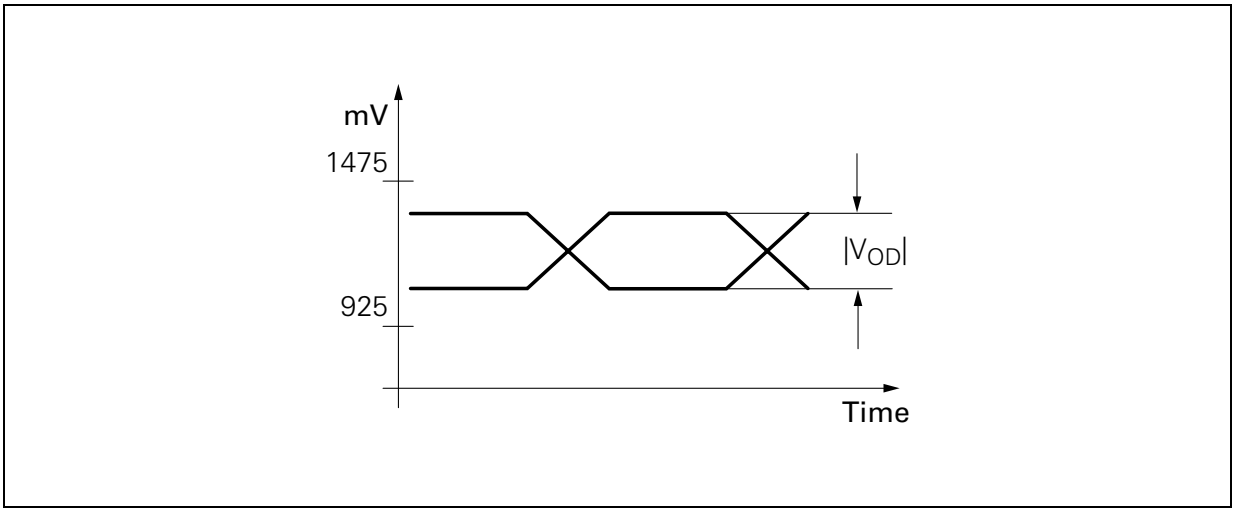


Figure 8 Output Level Diagram

Receiver Electro-Optical Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Data Rate Per Channel	DR	500[1]	1250	Mbit/s
Sensitivity (Average Power)[2]	P_{IN}		–18.5	dBm
Optical Modulation Amplitude [3]	OMA	0.028[4]		mW
Saturation (Average Power)	P_{SAT}	–3.0		dBm
Signal Detect Assert Level[5]	P_{SDA}		–19.5	
Signal Detect Deassert Level[5]	P_{SDD}	–29.0		
Signal Detect Hysteresis[5]	$P_{SDA} - P_{SDD}$	1.0	4.0	dB
Return Loss of Receiver	A_{RL}	12		

Optical parameters valid for each channel.

1) Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
2) BER = 10^{-12}, Extinction ratio = infinite, Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity.
3) Peak to peak value.
4) Corresponds to an maximum sensitivity (average power) of –18.5 dBm at an infinite extinction ratio.
5) Extinction ratio = infinite,
P_{SDA}: Average optical power when SD switches from inactive to active.
P_{SDD}: Average optical power when SD switches from active to inactive.

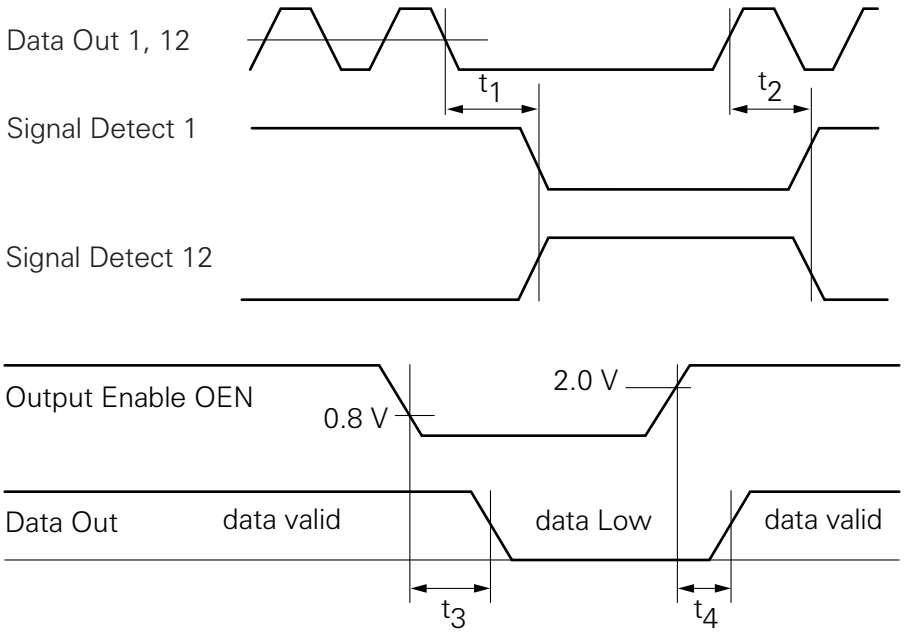


Figure 9 Timing Diagrams

Parameter	Symbol	Max.	Unit
Signal Detect Deassert Time	t_1	10	µs
Signal Detect Assert Time	t_2	10	
LVDS Output Enable off Delay Time	t_3	20	ns
LVDS Output Enable on Delay Time	t_4	20	

Assembly

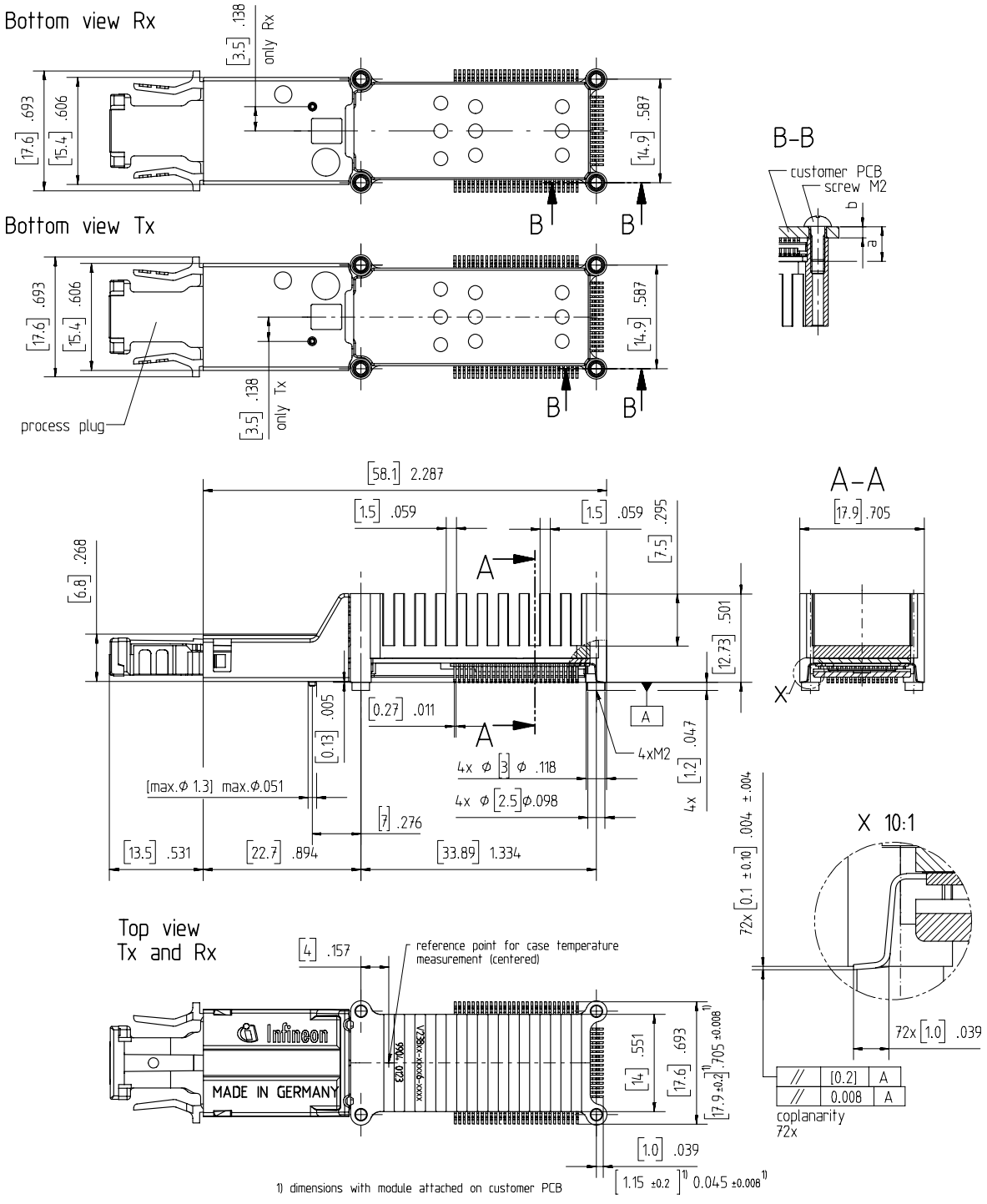
On the next pages are some figures to assist the customer in designing his printed circuit board (PCB). **Figure 10** shows the mechanical dimensions of the PAROLI transmitter and receiver modules and **Figure 11** to **Figure 13** give the dimensions of the holes and solder pads on a customer PCB that are necessary to mount the modules on this PCB. Keeping the tolerances for the PCB given in **Figure 11** to **Figure 13** is required to properly attach the PAROLI transmitter and receiver module to the PCB.

Attachment to the customer PCB should be done with four M2 screws torqued to 0.25 Nm +0.05 Nm (see **Figure 10**, cross section B-B). The screw length *a* should be 3 to 4 mm plus the thickness *b* of the customer PCB.

Special care must be taken to remove residues from the soldering and washing process which can impact the mechanical function. Avoid the use of aggressive organic solvents like ketones, ethers, etc. Consult the supplier of the PAROLI modules and the supplier of the solder paste and flux for recommended cleaning solvents.

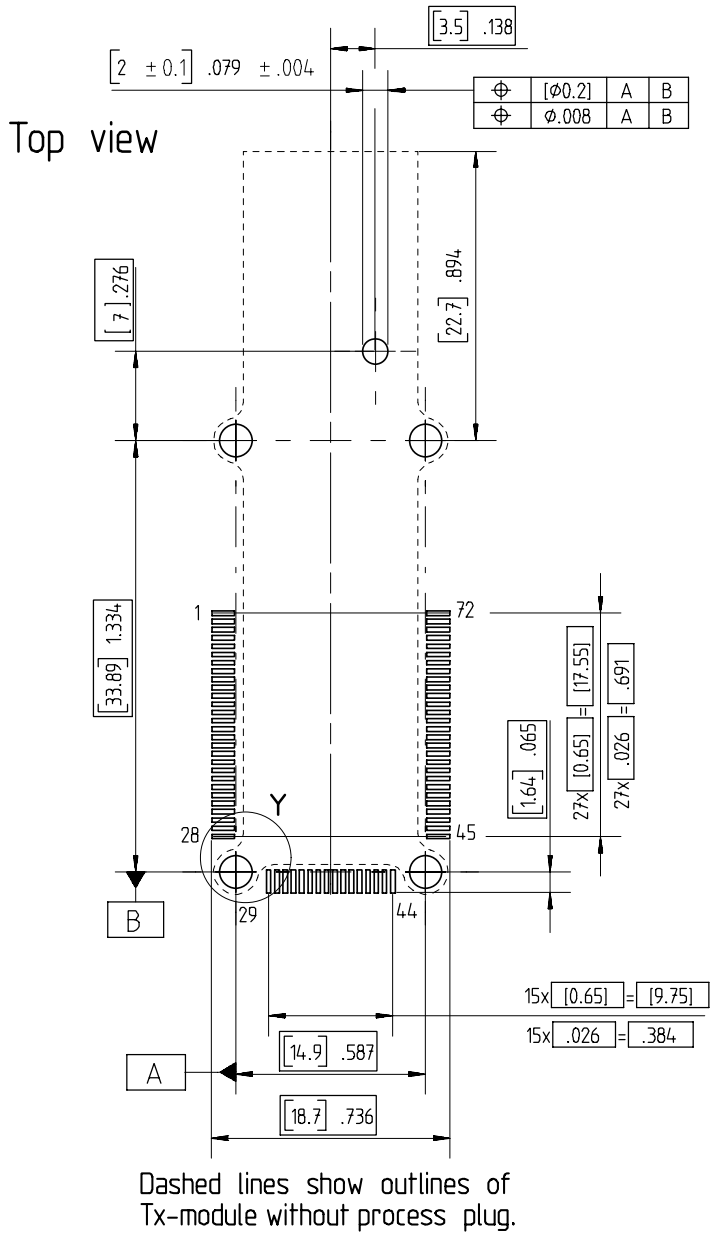
The following common cleaning solvents will not affect the module: deionized water, ethanol, and isopropyl alcohol. Air-drying is recommended to a maximum temperature of 150°C. Do not use ultrasonics.

During soldering, heat must be applied to the leads only, to ensure that the case temperature never exceeds 150°C. The module must be mounted with a hot-air or hot-bar soldering process using a SnPb solder type, e.g. Sn62Pb36Ag2, in accordance with ISO 9435.



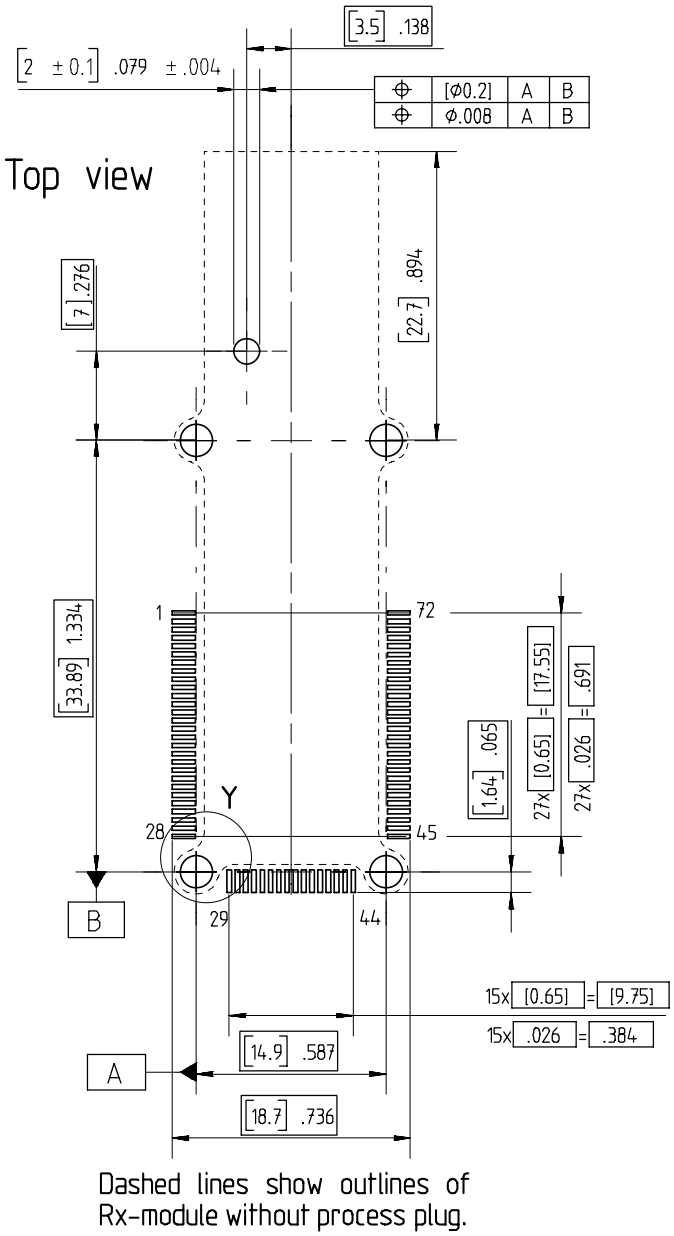
Dimensions in [mm] inches

Figure 10 Drawing of the PAROLI Transmitter and Receiver Module



Dimensions in [mm] inches

Figure 11 Recommended Circuit Board Layout: Transmitter



Dimensions in [mm] inches

Figure 12 Recommended Circuit Board Layout: Receiver

No electronic components are allowed on the customer PCB within the area covered by the PAROLI module and the jumper used to attach a ribbon fiber cable.

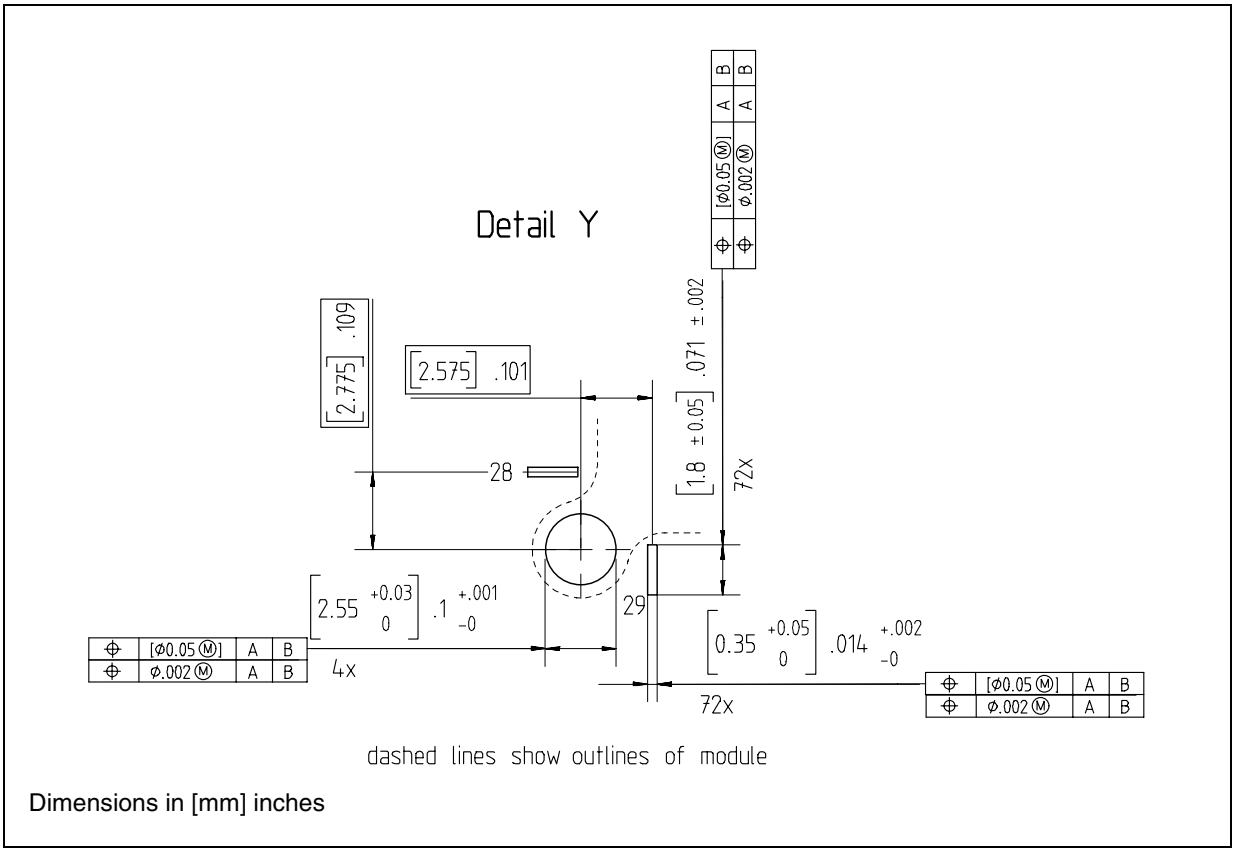


Figure 13 Mounting Hole, Detail Y (see **Figure 11** and **Figure 12**)

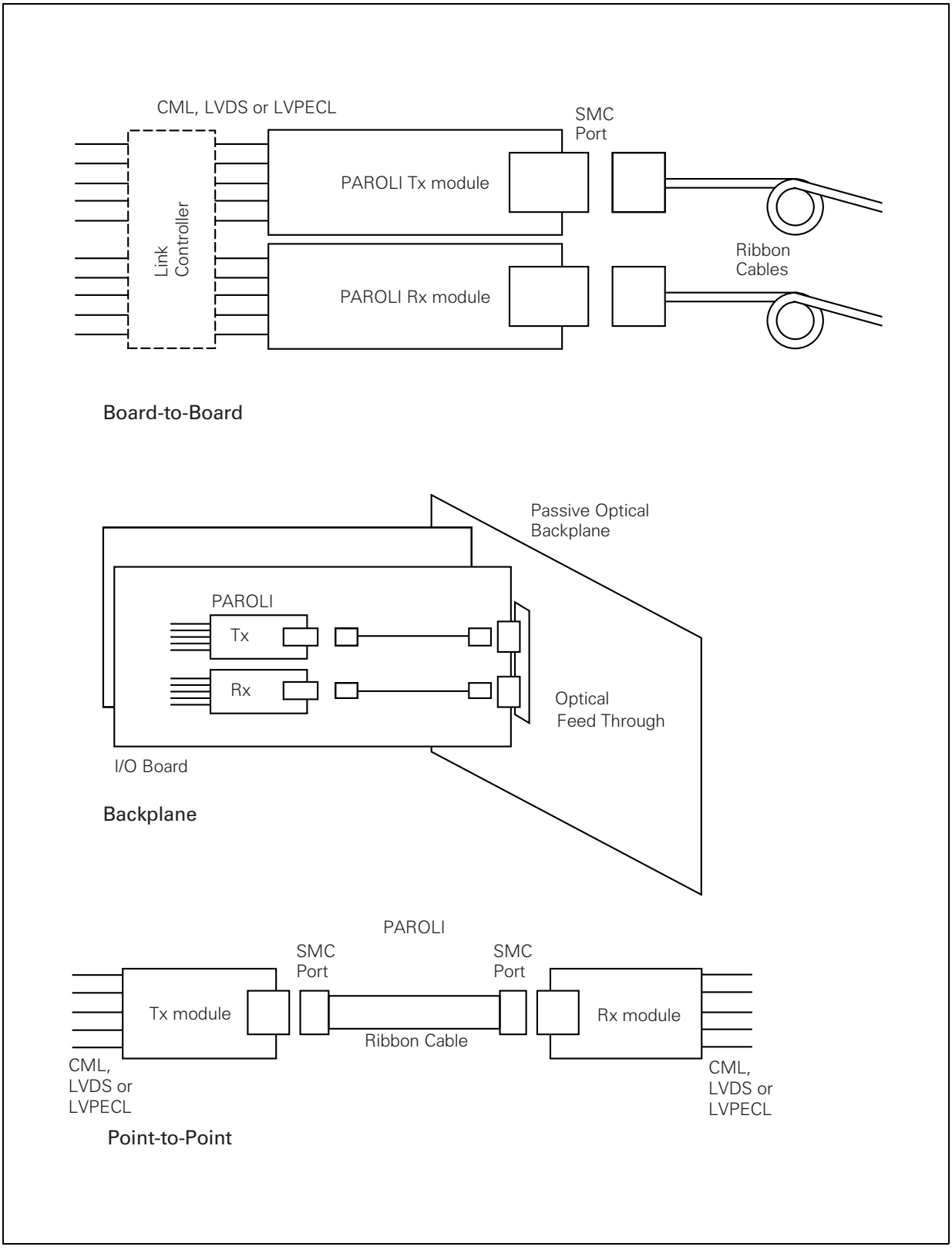
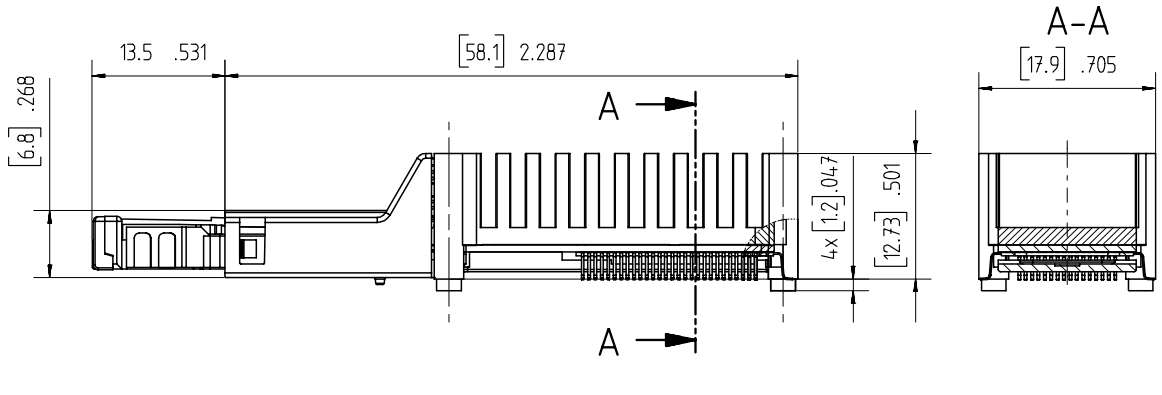


Figure 14 Applications

Package Outlines



Dimensions in [mm] inches

Figure 15

V23814-K1306-M136
V23815-K1306-M136
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