

M66258FP

8192 x 8-BIT LINE MEMORY

DESCRIPTION

The M66258FP is high speed line memory that uses high performance silicon gate CMOS process technology and adopts the FIFO (First In First Out) structure consisting of 8192 words x 8 bits.

The M66258FP, performing reading and writing operations at different cycles independently and asynchronously, is optimal for buffer memory to be used between equipment of different data processing speeds.

FEATURES

- Memory configuration 8192 words x 8 bits configuration
- High speed cycle 20 ns (Min.)
- High speed access 16 ns (Max.)
- Output hold 3 ns (Min.)
- Reading and writing operations can be completely carried out independently and asynchronously.
- Variable length delay bit
- Input/output TTL direct connection allowable
- Output 3 states

APPLICATION

- Digital copying machine, laser beam printer, high speed facsimile, etc.

FUNCTIONAL DESCRIPTION

When write enable input \overline{WE} is set to "L", the contents of data inputs D0 to D7 are read in synchronization with a rising edge of write lock input WCK to perform writing operation. When this is the case, the write address counter is also incremented simultaneously. When \overline{WE} is set to "H", the writing operation is inhibited and the write address counter stops.

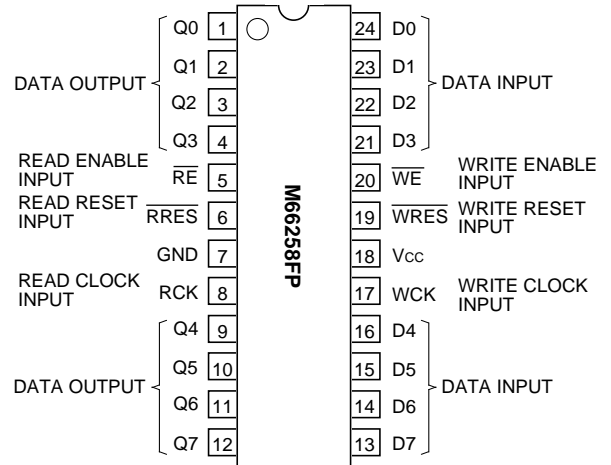
When write reset input \overline{WRES} is set to "L", the write address counter is initialized.

When read enable input \overline{RE} is set to "L", the contents of memory are output to data outputs Q0 to Q7 in synchronization with a rising edge of read clock input RCK to perform reading operation. When this is the case, the read address counter is incremented simultaneously.

When \overline{RE} is set to "H", the reading operation is inhibited and the read address counter stops. The outputs are placed in a high impedance state.

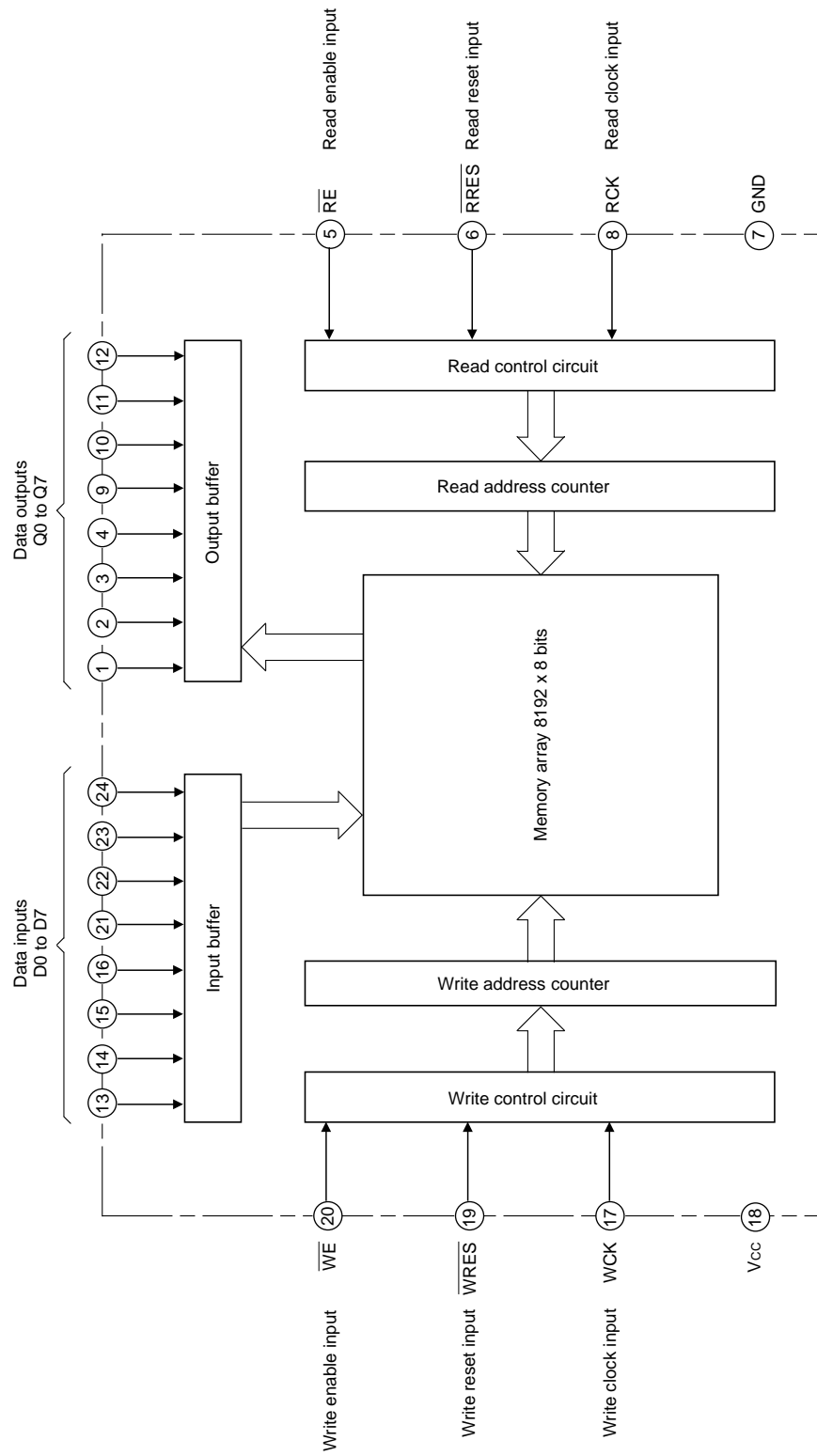
When read reset input \overline{RRES} is set to "L", the read address counter is initialized.

PIN CONFIGURATION (TOP VIEW)



Outline 24P2U-A(SSOP)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=0 – 70 °C unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|--------|---------------------|----------------------------|----------------|------|
| Vcc | Supply voltage | Value based on the GND pin | -0.5 – +6.0 | V |
| Vi | Input voltage | | -0.5 – Vcc+0.5 | V |
| Vo | Output voltage | | -0.5 – Vcc+0.5 | V |
| Pd | Power dispersion | Ta=25 °C | 825 | mW |
| Tstg | Storage temperature | | -65 – 150 | °C |

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|--------|-----------------------|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| Vcc | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply voltage | | 0 | | V |
| Topr | Operating temperature | 0 – 70 | | | °C |

ELECTRICAL CHARACTERISTICS (Ta=0 – 70 °C, Vcc=5V±10%, GND=0V unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|--------|---|---|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| VIH | High-level input voltage | | 2.0 | | | V |
| VIL | Low-level input voltage | | | | 0.8 | V |
| VOH | High-level output voltage | IOH = -4mA | Vcc-0.8 | | | V |
| VOL | Low-level output voltage | IOL = 4mA | | | 0.55 | V |
| IiH | High-level input current | Vi = Vcc | | | 1.0 | μA |
| IiL | Low-level input current | Vi = GND | | | -1.0 | μA |
| IOZH | Off-state high-level output current | Vo = Vcc | | | 5.0 | μA |
| IOZL | Off-state low-level output current | Vo = GND | | | -5.0 | μA |
| ICC | Average supply current during operation | Vi = Vcc, GND, output open twck, trck = 20ns | | | 150 | mA |
| CI | Input capacitance | f = 1MHz | | | 10 | pF |
| CO | Off-time output capacitance | f = 1MHz | | | 15 | pF |

SWITCHING CHARACTERISTICS (Ta=0 – 70 °C, Vcc=5V±10%, GND=0V unless otherwise noted)

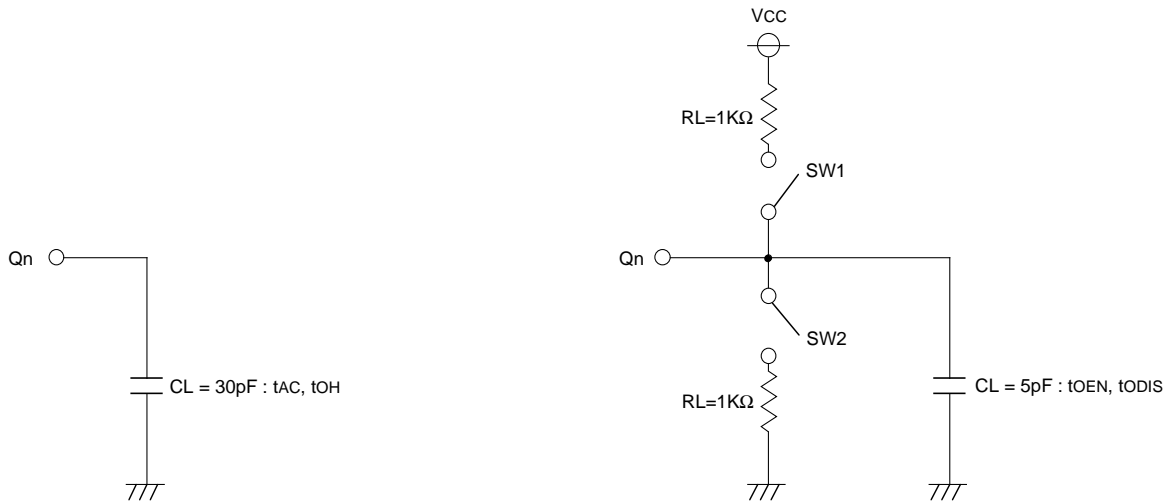
| Symbol | Parameter | Limits | | | Unit |
|--------|---------------------|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| tAC | Access time | | | 16 | ns |
| tOH | Output hold time | 3 | | | ns |
| tOEN | Output enable time | 3 | | 16 | ns |
| tODIS | Output disable time | 3 | | 16 | ns |

TIMING REQUIREMENTS (Ta=0 – 70 °C, Vcc=5V±10%, GND=0V unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| twCK | Write clock (WCK) cycle | 20 | | | ns |
| twCKH | Write clock (WCK) "H" pulse width | 8 | | | ns |
| twCKL | Write clock (WCK) "L" pulse width | 8 | | | ns |
| trCK | Read clock (RCK) cycle | 20 | | | ns |
| trCKH | Read clock (RCK) "H" pulse width | 8 | | | ns |
| trCKL | Read clock (RCK) "L" pulse width | 8 | | | ns |
| tDS | Input data set up time for WCK | 4 | | | ns |
| tDH | Input data hold time for WCK | 3 | | | ns |
| tRESS | Reset set up time for WCK/RCK | 4 | | | ns |
| tRESH | Reset hold time for WCK/RCK | 3 | | | ns |
| tnRESS | Reset non-selection set up time for WCK/RCK | 4 | | | ns |
| tnRESH | Reset non-selection hold time for WCK/RCK | 3 | | | ns |
| twES | \overline{WE} set up time for WCK | 4 | | | ns |
| tweH | \overline{WE} hold time for WCK | 3 | | | ns |
| tnwES | \overline{WE} non-selection set up time for WCK | 4 | | | ns |
| tnweH | \overline{WE} non-selection hold time for WCK | 3 | | | ns |
| tRES | \overline{RE} set up time for RCK | 4 | | | ns |
| treH | \overline{RE} hold time for RCK | 3 | | | ns |
| tnRES | \overline{RE} non-selection set up time for RCK | 4 | | | ns |
| tnREH | \overline{RE} non-selection hold time for RCK | 3 | | | ns |
| tr, tf | Input pulse up/down time | | | 20 | ns |
| tH | Data hold time (Note 1) | | | 20 | ms |

Note 1: For 1 line access, the following conditions must be satisfied:
 \overline{WE} high-level period ≤ 20 ms - 8192 • twCK - \overline{WRES} low-level period
 \overline{RE} high-level period ≤ 20 ms - 8192 • trCK - \overline{RRES} low-level period
 2: Perform reset operation after turning on power supply.

SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT

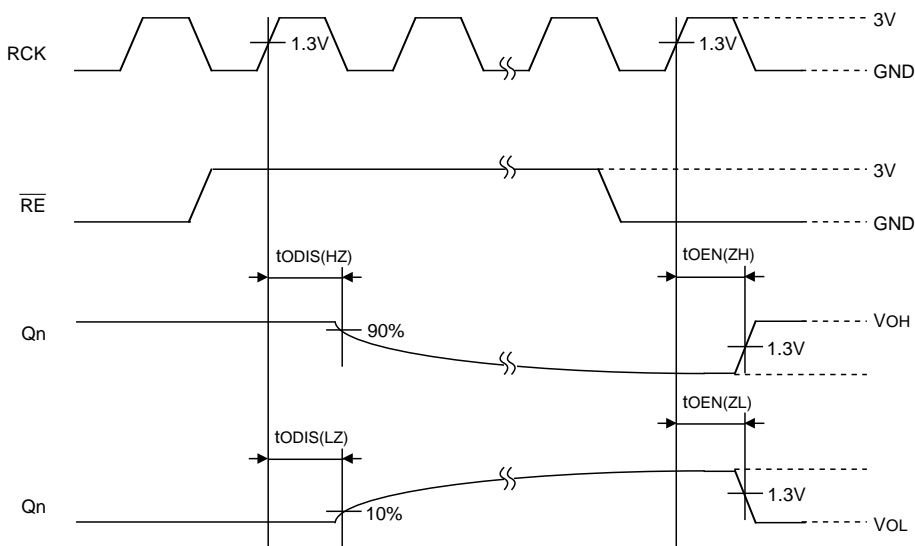


Input pulse level : 0 – 3V
 Input pulse up/down time : 3 ns
 Judging voltage Input : 1.3V
 Output : 1.3V(However, tODIS(LZ) is judged with 10% of the output amplitude, while tODIS(HZ) is judged with 90% of the output amplitude.)

Load capacitance CL includes the floating capacity of connected lines and input capacitance of probe.

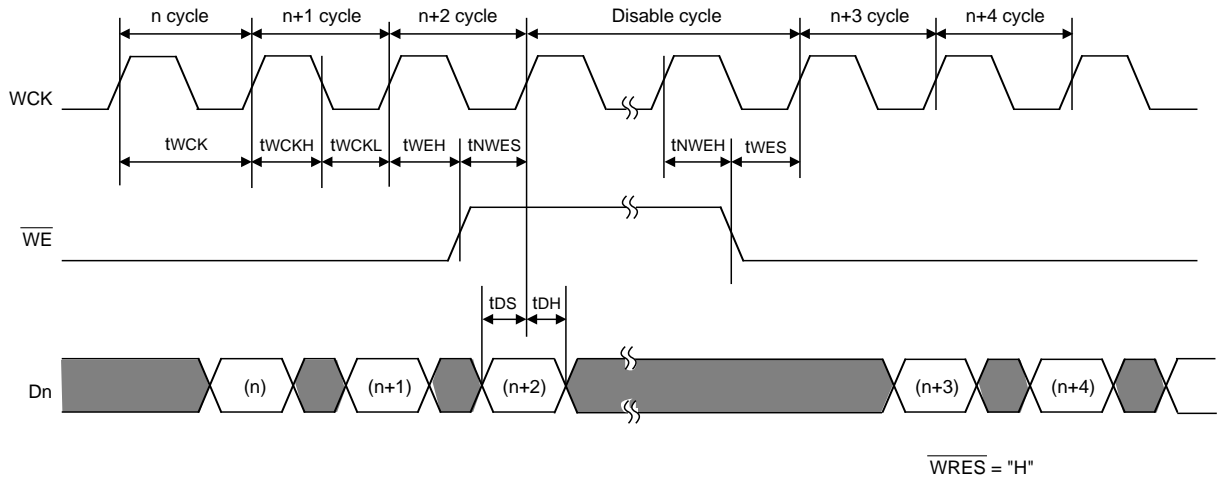
| Item | SW1 | SW2 |
|-----------|-------|-------|
| tODIS(LZ) | Close | Open |
| tODIS(HZ) | Open | Close |
| tOEN(ZL) | Close | Open |
| tOEN(ZH) | Open | Close |

tODIS and tOEN measurement condition

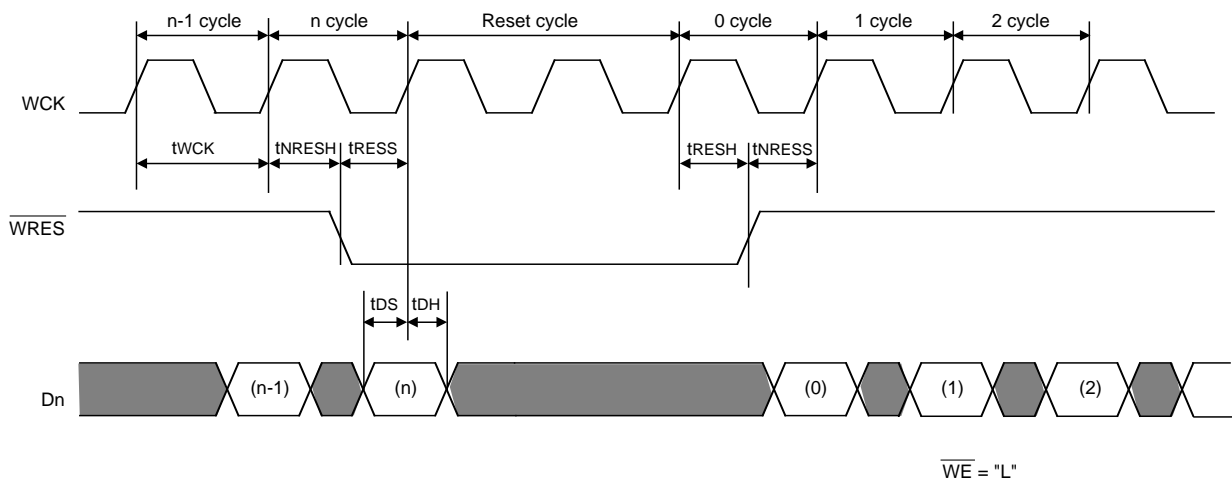


OPERATION TIMING

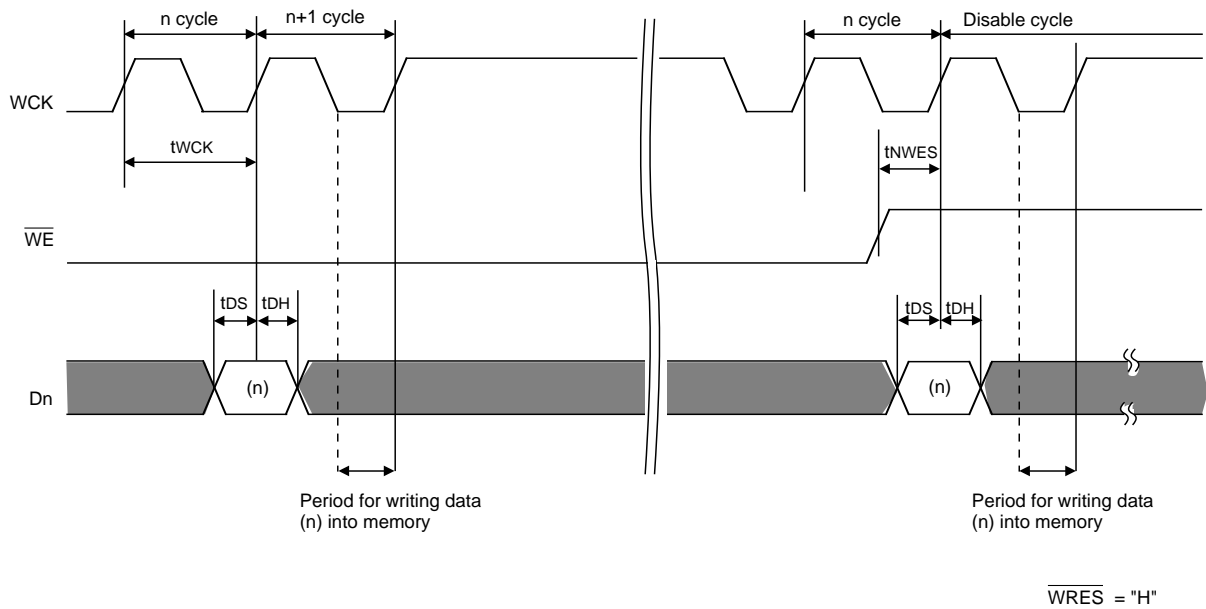
- Write cycle



- Write reset cycle



- Matters that needs attention when WCK stops

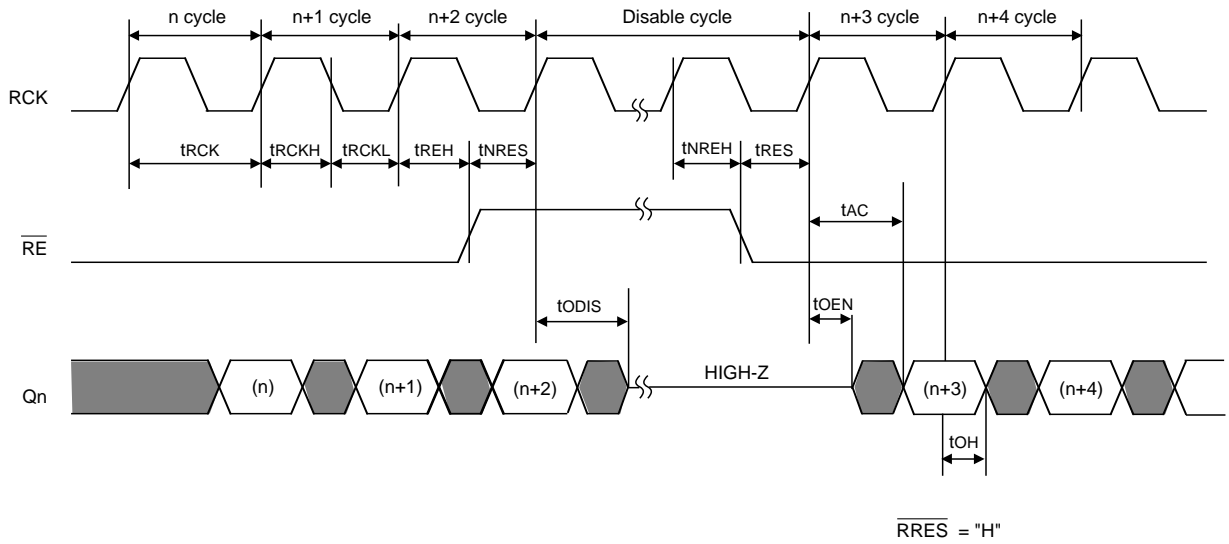


Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n+1 cycle. The writing operation is complete at the falling edge after n+1 cycle.

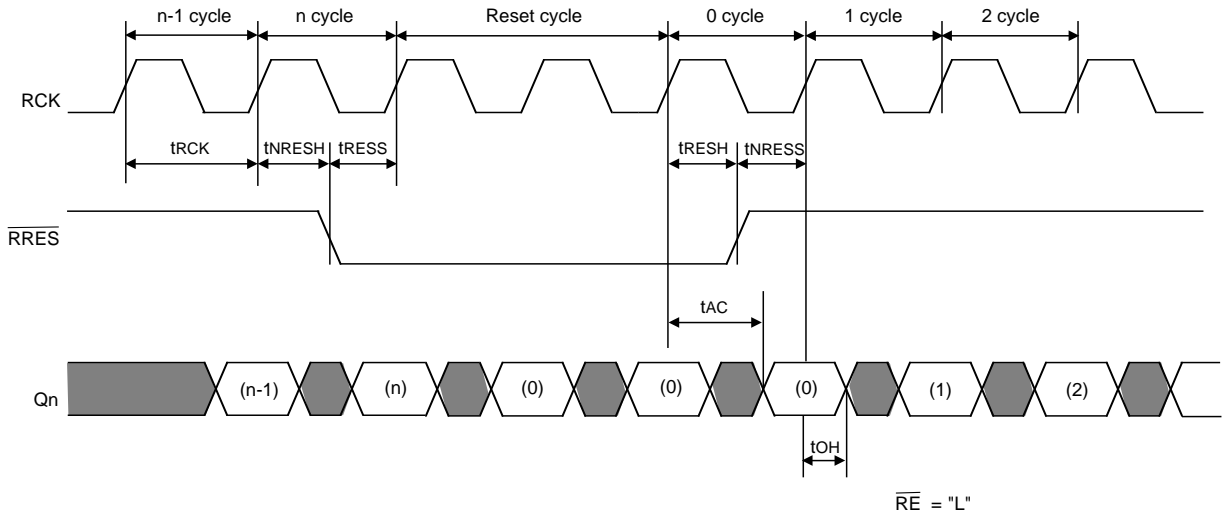
To stop reading write data at n cycle, enter WCK before the rising edge after n+1 cycle.

When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

• Read cycle



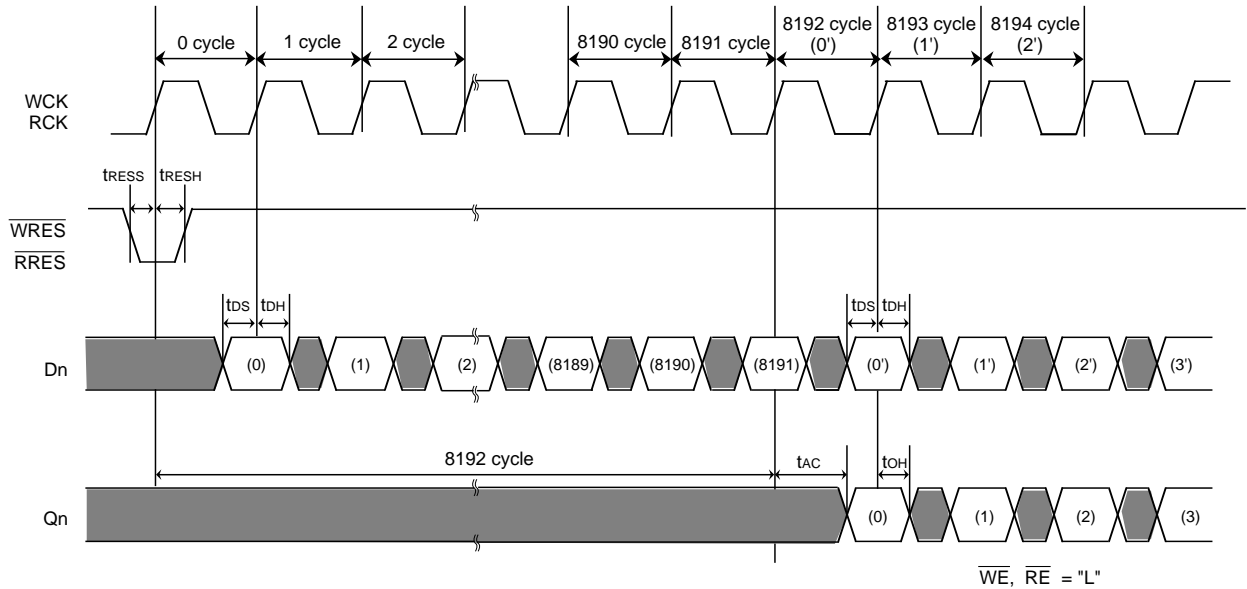
• Read reset cycle



VARIABLE LENGTH DELAY BIT

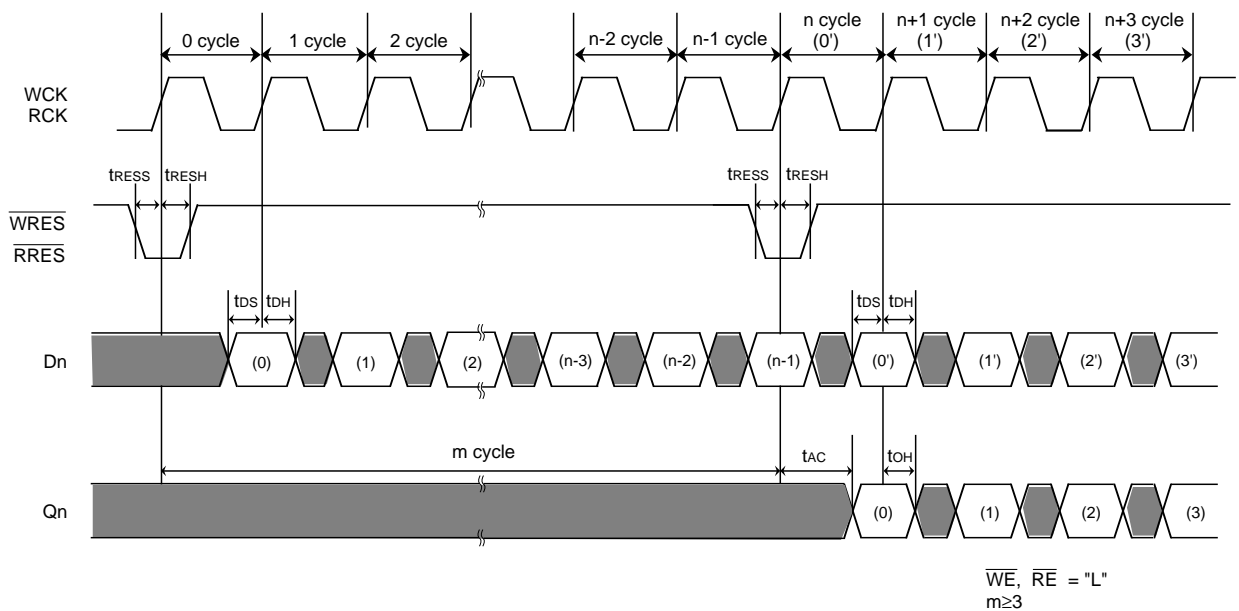
- 1 line (8192 bits) delay

Input data can be written at the rising edge of WCK after write cycle and output data is read at the rising edge of RCK before read cycle to easily make 1 line delay.



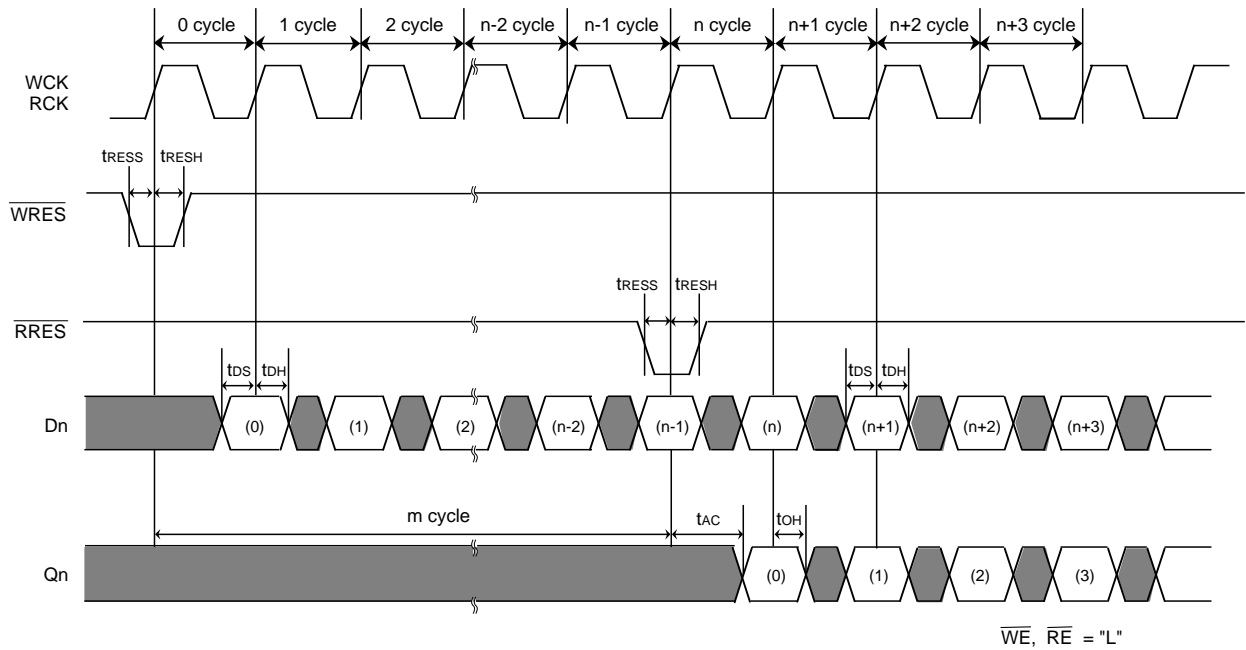
- n-bit delay bit

(Reset at cycles according to the delay length)



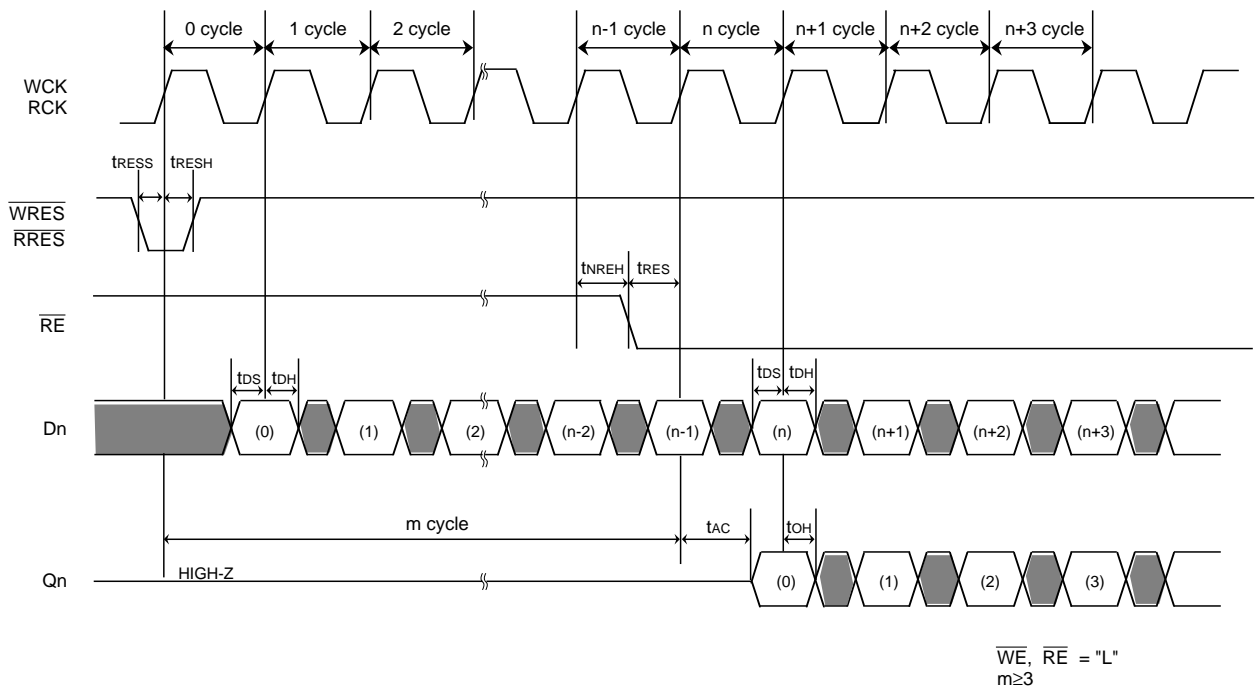
• n-bit delay 2

(Slides input timings of \overline{WRES} and \overline{RRES} at cycles according to the delay length.)



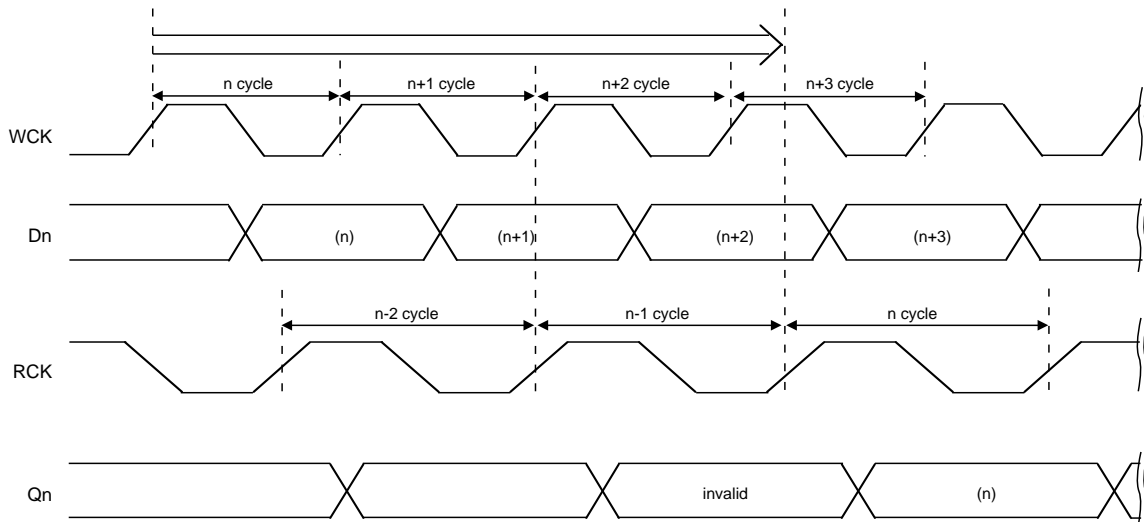
• n-bit delay 3

(Slides address by disabling \overline{RE} in the period according to the delay length.)



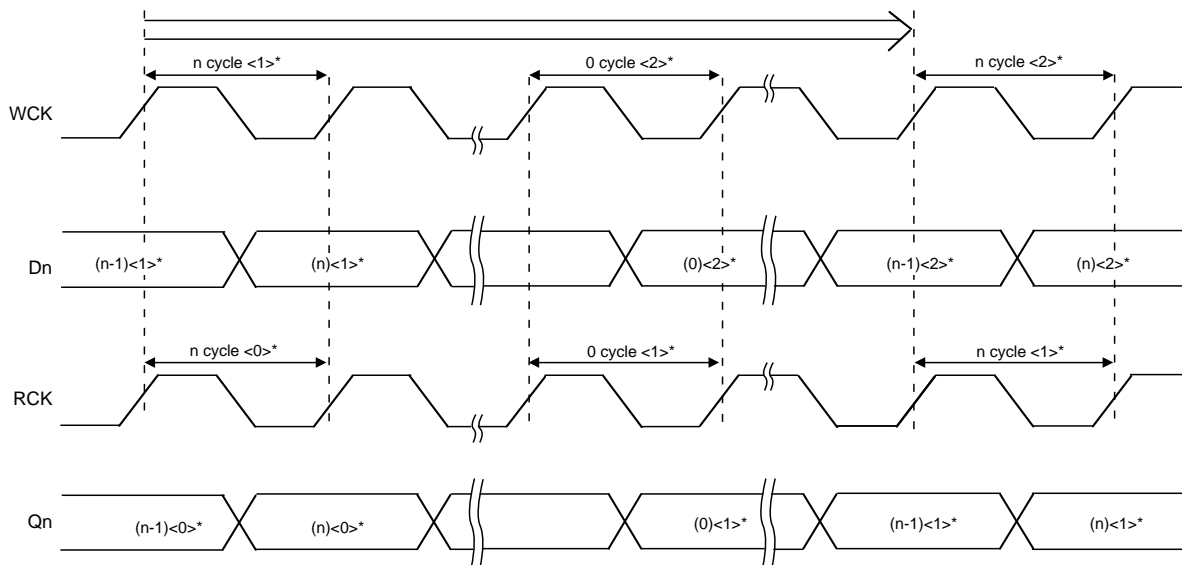
- Reading shortest n-cycle write data "n"
(Reading side n-1 cycle starts after the end of writing side n-1 cycle.)

When the reading side n-1 cycle starts before the end of the writing side n+1 cycle, output Qn of n cycle is made invalid. In the following diagram, reading operation of n-1 cycle is invalid.



- Reading longest n-cycle write data "n": 1 line delay
(When writing side n-cycle <2>* starts, reading side n cycle <1>* then starts.)

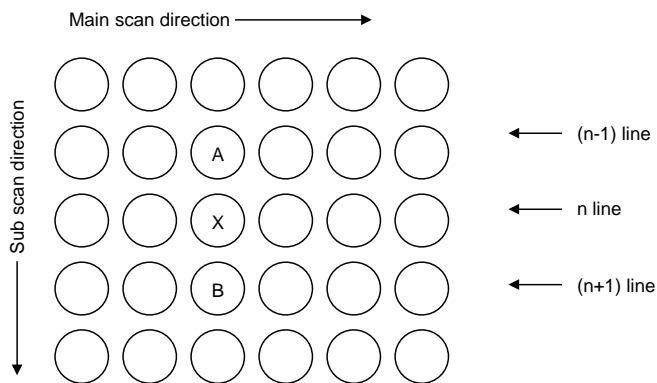
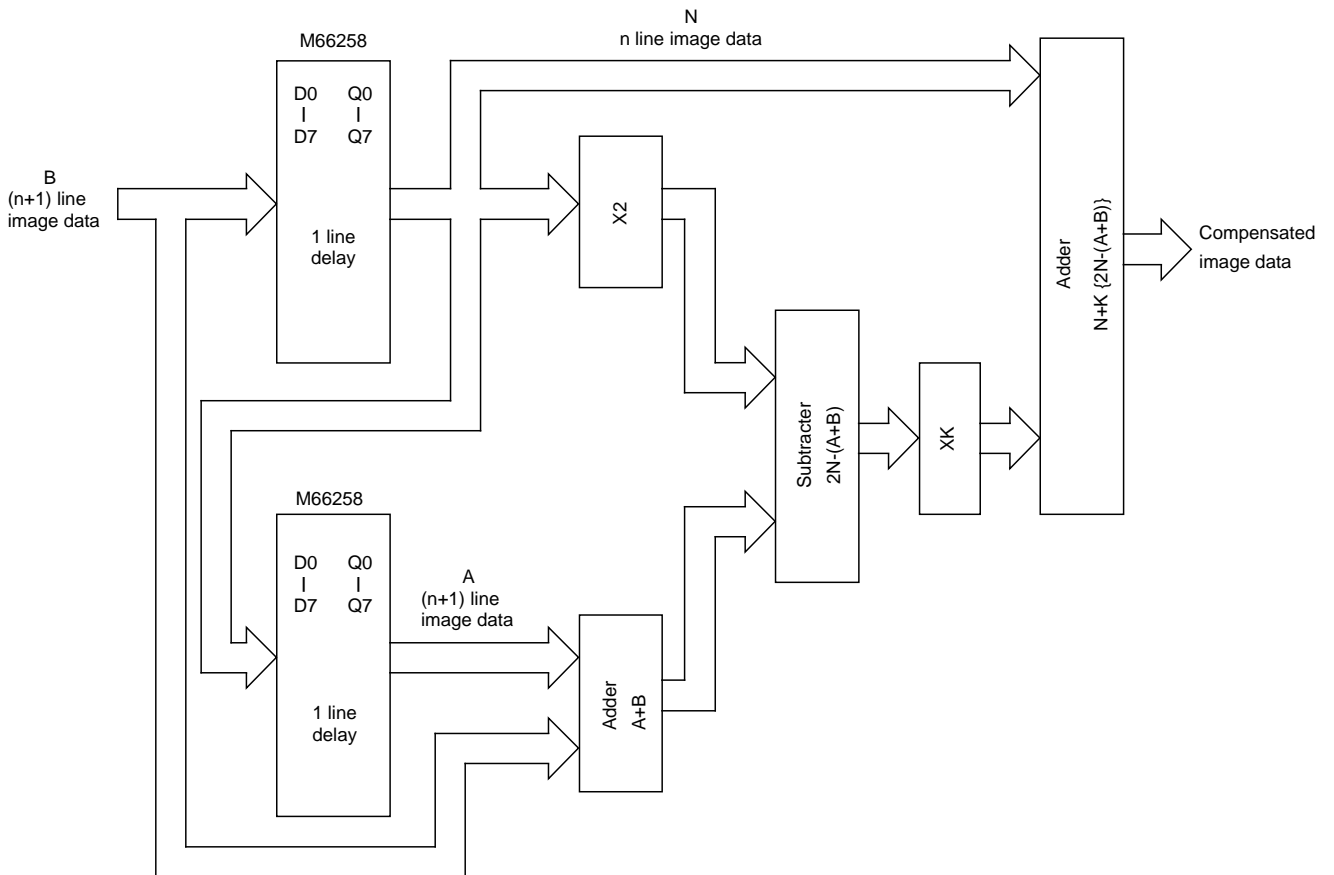
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.



<0>*, <1>* and <2>* indicate value of lines.

APPLICATION EXAMPLE

Sub Scan Resolution Compensation Circuit with Laplacean Filter



$$N' = N + K \{ (N-A) + (N-B) \}$$

$$= N + K \{ 2N - (A+B) \}$$

K: Laplacean coefficient