M66257FP

5120 × 8-BIT × 2 LINE MEMORY (FIFO)

DESCRIPTION

The M66257FP is a high-speed line memory with a FIFO (First In First Out) structure of 5120-word × 8-bit double configuration which uses high-performance silicon gate CMOS process technology.

It allows simultaneous output of 1-line delay data and 2-line delay data, and is most suitable for data correction over multiple lines.

It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

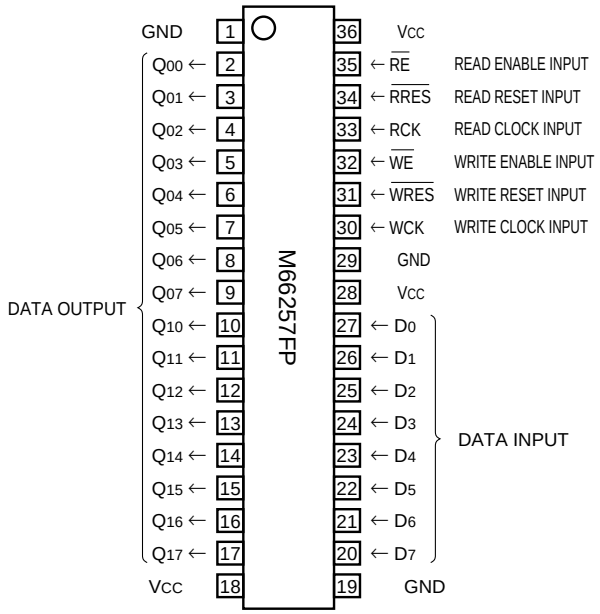
FEATURES

- Memory configuration of 5120 words × 8 bits × 2 (dynamic memory)
- High-speed cycle ..... 25ns (Min.)
- High-speed access ..... 18ns (Max.)
- Output hold ..... 3ns (Min.)
- Fully independent, asynchronous write and read operations
- Output ..... 3 states
- Q_{00} to Q_{07} ..... 1-line delay
- Q_{10} to Q_{17} ..... 2-line delay

APPLICATION

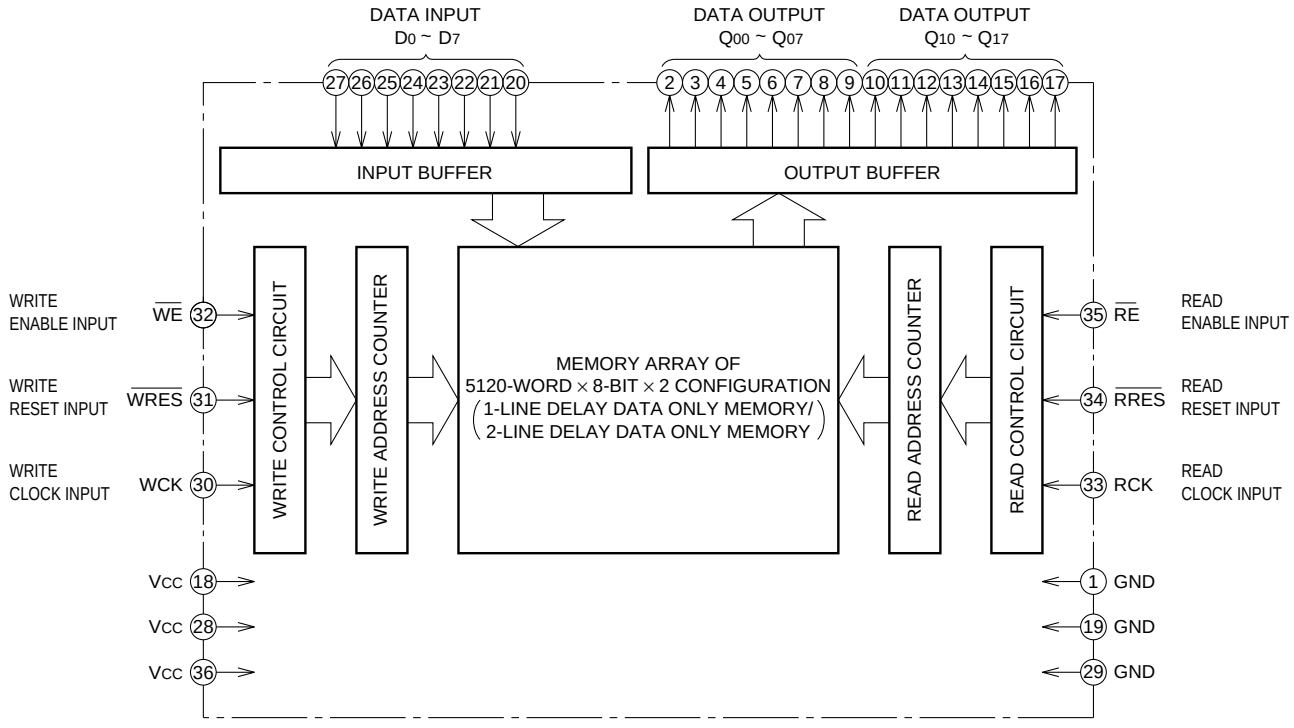
Digital photocopiers, high-speed facsimile, laser beam printers.

PIN CONFIGURATION (TOP VIEW)



Outline 36P2R-A

BLOCK DIAGRAM



FUNCTION

When write enable input $\overline{WE}$ is "L", the contents of data inputs D_0 to D_7 are written into 1-line delay data only memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter of 1-line delay data only memory is also incremented simultaneously.

The write functions given below are also performed in synchronization with rise edge of WCK.

When $\overline{WE}$ is "H", a write operation to 1-line delay data only memory is inhibited and the write address counter of 1-line delay data only memory is stopped.

When write reset input $\overline{WRES}$ is "L", the write address counter of 1-line delay data only memory is initialized.

When read enable input $\overline{RE}$ is "L", the contents of 1-line delay data only memory are output to data outputs Q_{00} to Q_{07} and those of 2-line delay data only memory to data outputs Q_{10} to Q_{17} in synchronization with the rise of read clock input RCK. At this time, the read address counters of 1-line and 2-line delay data only memories is also incremented simultaneously.

Moreover, data of Q_{00} to Q_{07} are written into 2-line delay data only memory in synchronization with rise edge of RCK. At this time, the write address of 2-line delay data only memory is incremented.

The read functions given below are also performed in synchronization with rise edge of RCK.

When $\overline{RE}$ is "H", a read operation from both of 1-line delay data only memory and 2-line delay data only memory is inhibited and the read address counter of each memory is stopped. The outputs of Q_{00} to Q_{07} and Q_{10} to Q_{17} are in the high impedance state.

Moreover, a write operation to 2-line delay data only memory is inhibited and the write address counter of 2-line delay data only memory is stopped.

When read reset input $\overline{RRES}$ is "L", the read address counter of 1-line delay data only memory, and the write address counter and read address counter of 2-line delay data only memory are initialized.

ABSOLUTE MAXIMUM RATINGS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	A value based on GND pin	–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
P_d	Maximum power dissipation	T_a = 25°C	660	mW
T_{stg}	Storage temperature		–65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
T_{opr}	Operating ambient temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	"H" input voltage			2.0			V
V_{IL}	"L" input voltage					0.8	V
V_{OH}	"H" output voltage	I_{OH} = –4mA		V_{CC}–0.8			V
V_{OL}	"L" output voltage	I_{OL} = 4mA				0.55	V
I_{IH}	"H" input current	V_I = V_{CC}	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 ~ D_7			1.0	μA
I_{IL}	"L" input current	V_I = GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 ~ D_7			–1.0	μA
I_{OZH}	Off state "H" output current	V_O = V_{CC}				5.0	μA
I_{OZL}	Off state "L" output current	V_O = GND				–5.0	μA
I_{CC}	Operating mean current dissipation	V_I = V_{CC}, GND, Output open t_{WCK}, t_{RCK} = 25ns				120	mA
C_I	Input capacitance	f = 1MHz				10	pF
C_O	Off state output capacitance	f = 1MHz				15	pF

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise noted)

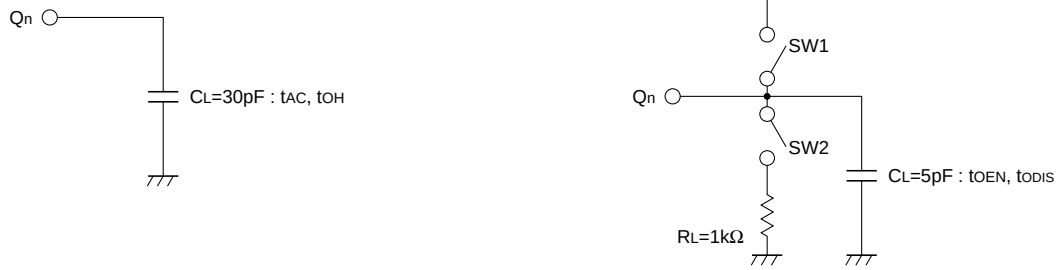
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AC}	Access time			18	ns
t_{OH}	Output hold time	3			ns
t_{OEN}	Output enable time	3		18	ns
t_{ODIS}	Output disable time	3		18	ns

TIMING CONDITIONS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WCK}	Write clock (WCK) cycle	25			ns
t_{WCKH}	Write clock (WCK) “H” pulse width	11			ns
t_{WCKL}	Write clock (WCK) “L” pulse width	11			ns
t_{RCK}	Read clock (RCK) cycle	25			ns
t_{RCKH}	Read clock (RCK) “H” pulse width	11			ns
t_{RCKL}	Read clock (RCK) “L” pulse width	11			ns
t_{DS}	Input data setup time to WCK	7			ns
t_{DH}	Input data hold time to WCK	3			ns
t_{RESS}	Reset setup time to WCK or RCK	7			ns
t_{RESH}	Reset hold time to WCK or RCK	3			ns
t_{NRESS}	Reset nonselect setup time to WCK or RCK	7			ns
t_{NRESH}	Reset nonselect hold time to WCK or RCK	3			ns
t_{WES}	$\overline{WE}$ setup time to WCK	7			ns
t_{WEH}	$\overline{WE}$ hold time to WCK	3			ns
t_{NWES}	$\overline{WE}$ nonselect setup time to WCK	7			ns
t_{NWEH}	$\overline{WE}$ nonselect hold time to WCK	3			ns
t_{RES}	$\overline{RE}$ setup time to RCK	7			ns
t_{REH}	$\overline{RE}$ hold time to RCK	3			ns
t_{NRES}	$\overline{RE}$ nonselect setup time to RCK	7			ns
t_{NREH}	$\overline{RE}$ nonselect hold time to RCK	3			ns
t_r, t_f	Input pulse rise/fall time			20	ns
t_H	Data hold time (Note 1)			20	ms

Note 1: For 1-line access, the following should be satisfied:
$\overline{WE}$ “H” level period **<** 20ms – 5120 t_{WCK} – $\overline{WRES}$ “L” level period
$\overline{RE}$ “H” level period **<** 20ms – 5120 t_{RCK} – $\overline{RRES}$ “L” level period
2: Reset the IC after power is turned on.

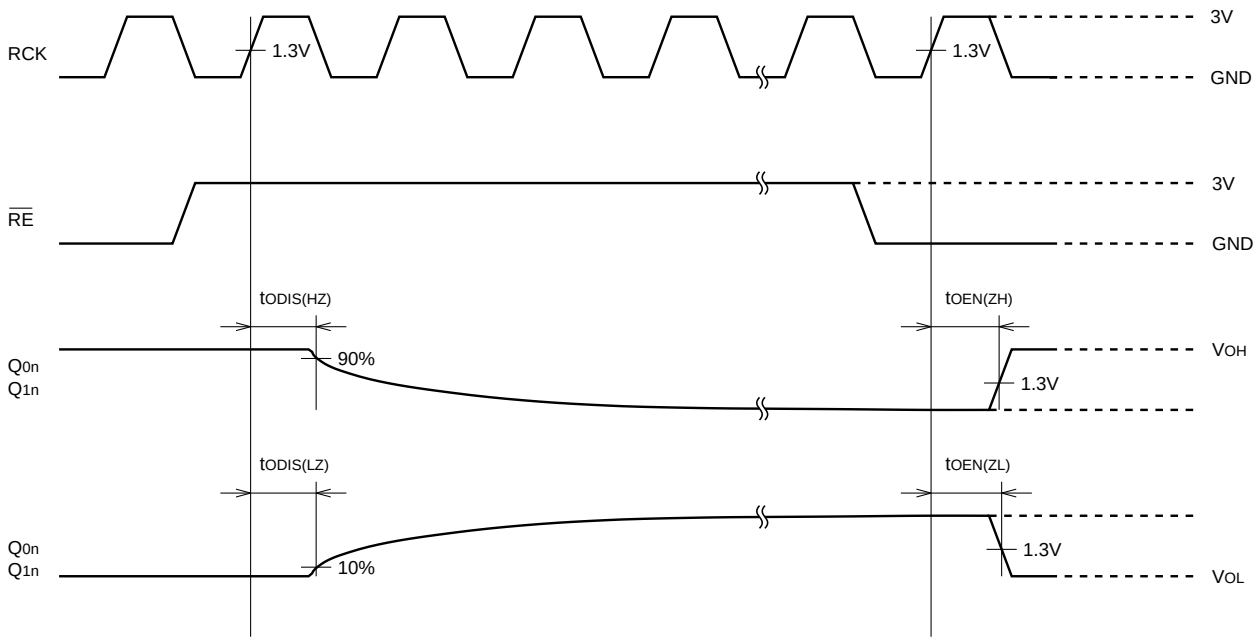
TEST CIRCUIT



Input pulse level : 0 ~ 3V
Input pulse rise/fall time : 3ns
Decision voltage input : 1.3V
Decision voltage output : 1.3V (However, $t_{ODIS(LZ)}$ is 10% of output amplitude and $t_{ODIS(HZ)}$ is 90% of that for decision).
The load capacitance C_L includes the floating capacitance of connection and the input capacitance of probe.

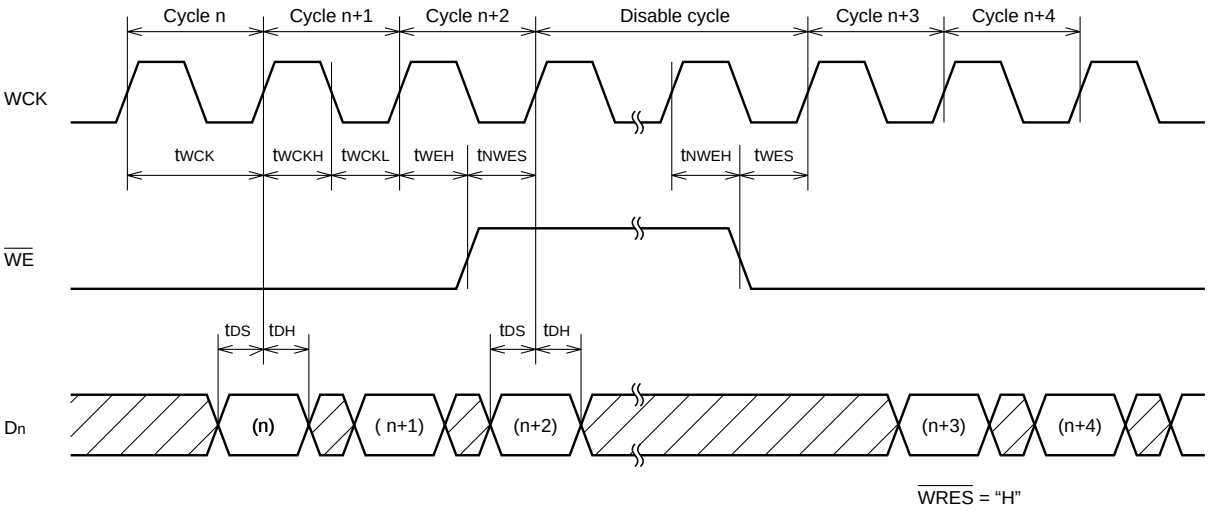
Parameter	SW1	SW2
$t_{ODIS(LZ)}$	Closed	Open
$t_{ODIS(HZ)}$	Open	Closed
$t_{OEN(ZL)}$	Closed	Open
$t_{OEN(ZH)}$	Open	Closed

t_{ODIS}/t_{OEN} TEST CONDITION

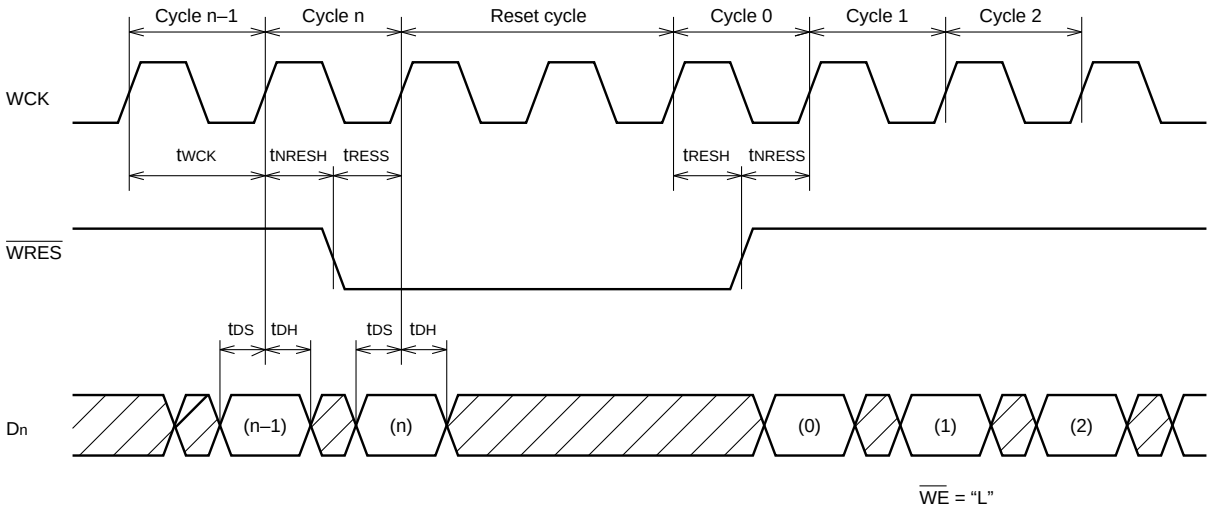


OPERATING TIMING

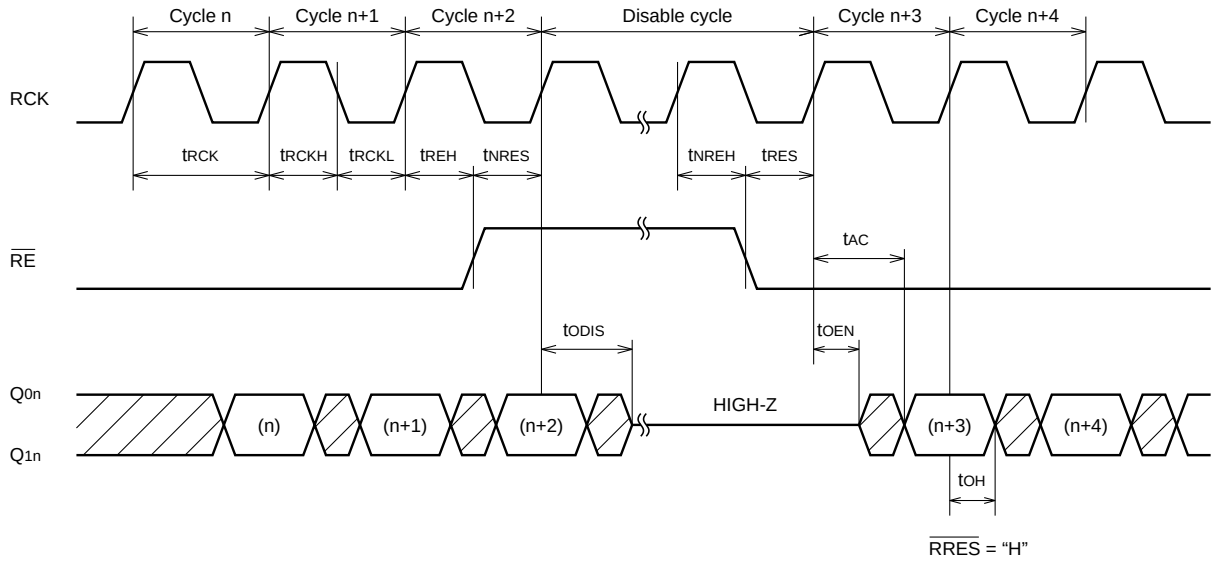
• Write cycle



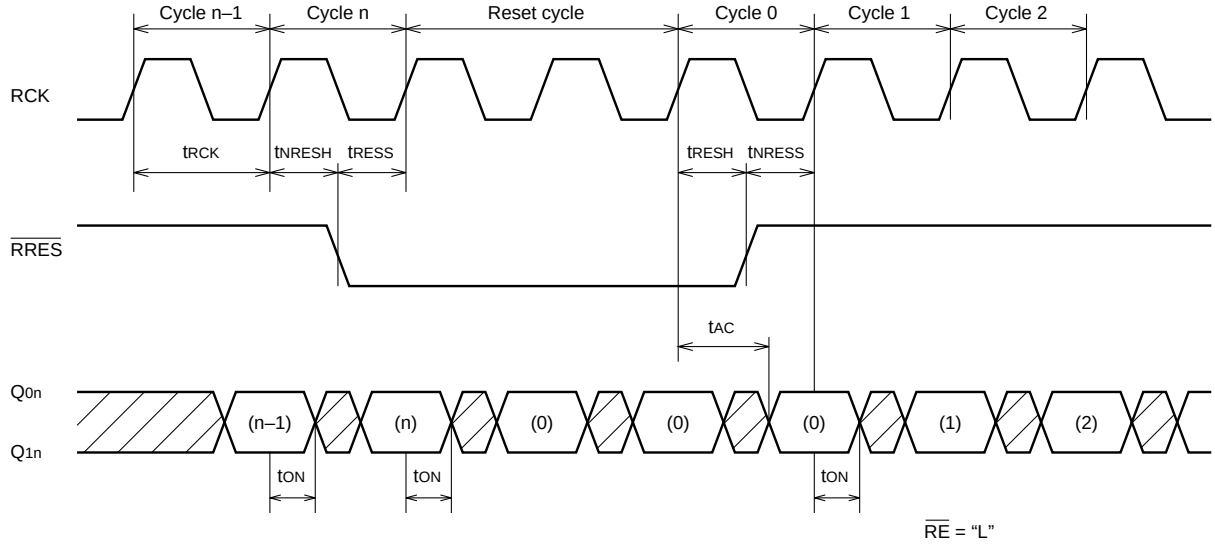
• Write reset cycle



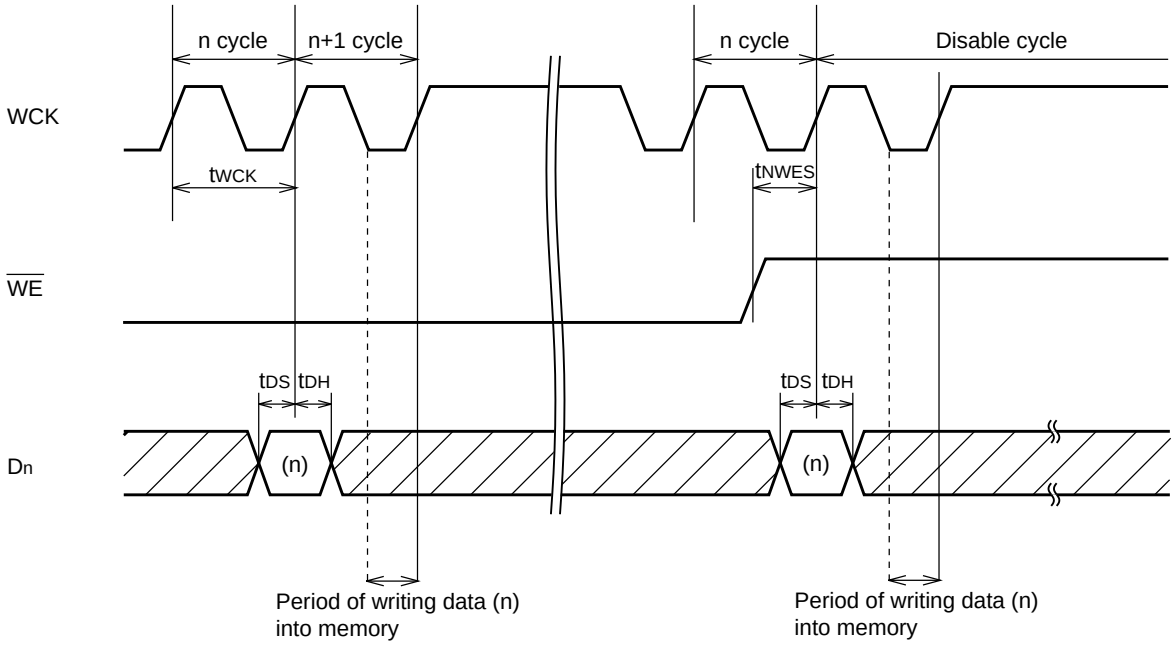
• Read cycle



• Read reset cycle



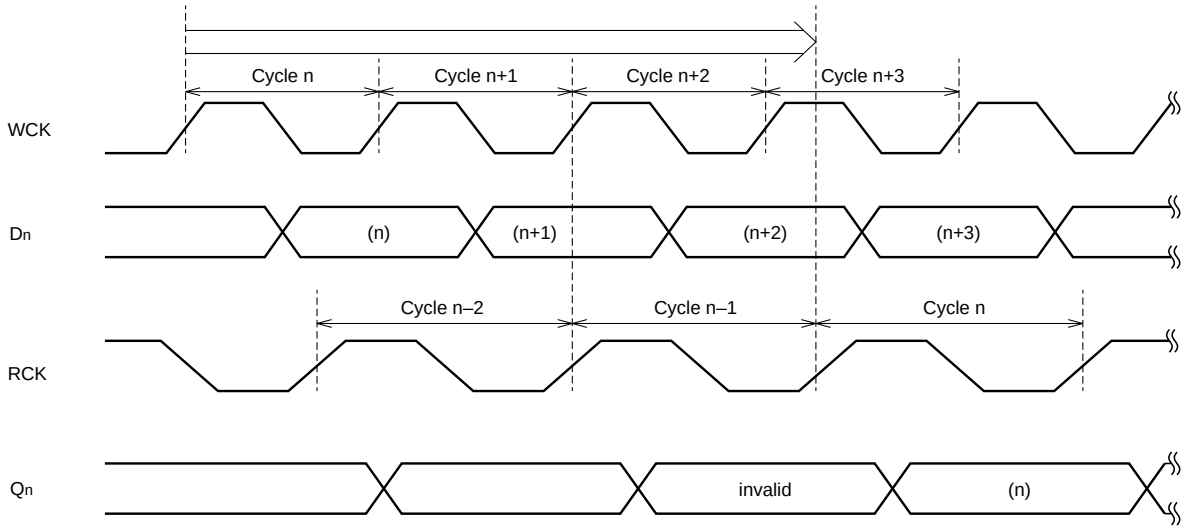
• Note at WCK stop



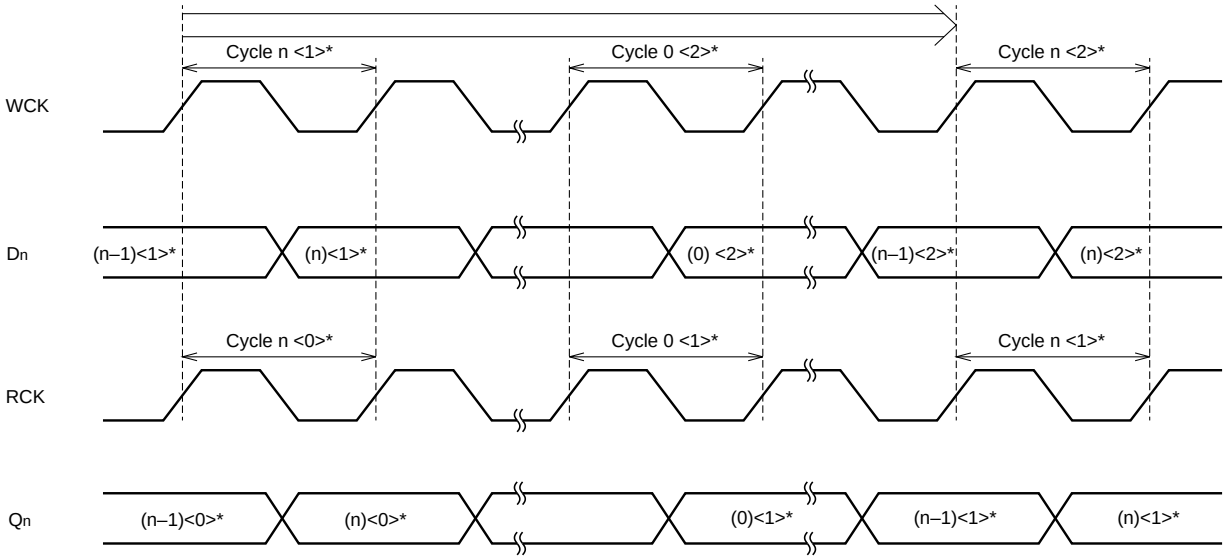
$\overline{WRES}$ = “H”

Input data Dn of n cycle is read at the rising edge after WCK of n cycle. Writing operation starts in the “L” period of WCK of n+1 cycle and ends at the rising edge after n+1 cycle.
To stop reading write data at n cycle, input WCK for up to the rising edge of n+1 cycle.
When the cycle next to n cycle is a disable cycle, input of WCK for a cycle is required after a disable cycle as well.

• Shortest read of data “n” written in cycle n
Cycle n–1 on read side should be started after end of cycle n+1 on write side
When the start of cycle n–1 on read side is earlier than the end of cycle n+1 on write side, output Q_n of cycle n becomes invalid. In the figure shown below, the read of cycle n–1 is invalid.



• Longest read of data “n” written in cycle n: 1-line delay
Cycle n <1>* on read side should be started when cycle n <2>* on write is started
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.



<0>*, <1>* and <2>* indicates a line value.

APPLICATION EXAMPLE

Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction.