Features

- **Smart Card Interface**
  - **Compliance with ISO 7816, EMV2000, GIE-CB, GSM and WHQL Standards**
    - **Card Clock Stop High or Low for Card Power-down Modes**
    - **Support Synchronous Cards with C4 and C8 Contacts**
    - **Card Detection and Automatic de-activation Sequence**
    - **Programmable Activation Sequence**
  - **Direct Connection to the Smart Card**
    - **Logic Level Shifters**
    - **Short Circuit Current Limitation (see electrical characteristics)**
    - **8kV+ ESD Protection (MIL/STD 883 Class 3)**
  - **Programmable Voltage**
    - **5V ±5% at 65 mA (Class A)**
    - **3V ±0.2V at 65 mA (Class B)**
    - **1.8V ±0.14V at 40 mA**
  - **Low Ripple Noise: < 200 mV**
- **Versatile Host Interface**
  - **ICAM (Conditional Access) Compatible**
  - **Two Wire Interface (TWI) Link**
    - **Programmable Address Allow up to 8 Devices**
  - **Programmable Interrupt Output**
  - **Automatic Level Shifter (1.6V to V_{CC})**
- **Reset Output Includes**
  - **Power-On Reset (POR)**
  - **Power-Fail Detector (PFD)**
- **High-efficiency Step-up Converter: 80 to 98% Efficiency**
- **Extended Voltage Operation: 3V to 5.5V**
- **Low Power Consumption**
  - **180 mA Maximum In-rush Current**
  - **30 µA Typical Power-down Current (without Smart Card)**
- **4 to 48 MHz Clock Input, 7 MHz Min for Step-up Converter (for AT83C24)**
- **18 to 48MHz Clock input (for AT83C24NDS)**
- **Industrial Temperature Range: -40 to +85°C**
- **Packages: SO28 and QFN28**

Description

The AT83C24 is a smart card reader interface IC for smart card reader/writer applications such as EFT/POS terminals and set top boxes. It enables the management of any type of smart card from any kind of host. Up to 8 AT83C24 can be connected in parallel using the programmable TWI address.

Its high efficiency DC/DC converter, low quiescent current in standby mode makes it particularly suited to low power and portable applications. The reduced bill of material allows reducing significantly the system cost. A sophisticated protection system guarantees timely and controlled shutdown upon error conditions.

The AT83C24NDS is a dedicated version approved by NDS for use with NDS VideoGuard conditional access software in set-top boxes. All AT83C24 datasheet is applicable to AT83C24NDS. The main differences between AT83C24 and AT83C24NDS are listed below:

1/ CLASS A card supplied with CVCC = 4.75 to 5.25V for AT83C24NDS,
CLASS A card supplied with CVCC = 4.6 to 5.25V for AT83C24

2/ 18MHz minimum on input clock for AT83C24NDS

3/ Up to 10µF for capacitor connected on CVCC pin for AT83C24,
3.3µF mandatory for AT83C24NDS

Smart Card Reader Interface with Power Management

AT83C24
AT83C24NDS

4234E–SCR–09/04

Acronyms

TWI: Two-wire Interface

POR: Power On Reset

PFD: Power Fail Detect

ART: Automatic Reset Transition

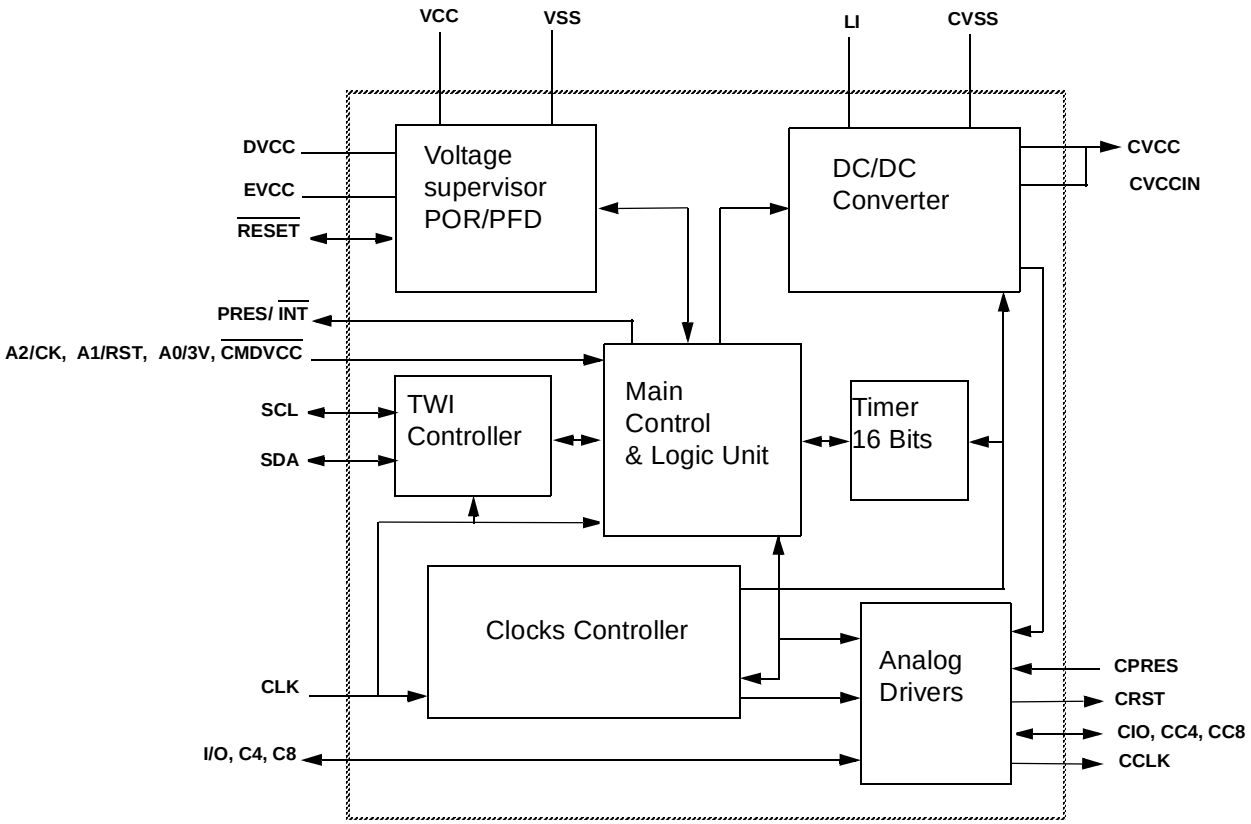
ATR: Answer To Reset

MSB: Most Significant Bit

LSB: Least Significant bit

SCIB: Smart Card Interface Bus

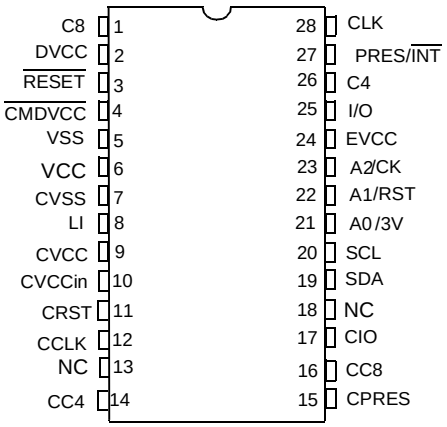
Block Diagram



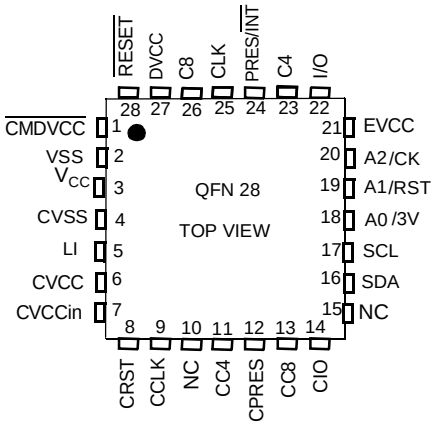
Pin Description

Pinouts (Top View)

28-pin SOIC Pinout



QFN28 pinout



Note: 1. NC = Not Connected

2. SOIC and QFN packages are available for AT83C24 and for AT83C24NDS

Signals

Table 1. Ports Description

Pad Name	Pad Internal Power Supply	ESD Limits	Pad Type	Description
A2/CK-A1/RST-A0/3V	EVCC	3 kV	I	Microcontroller Interface Function: TWI bus slave address selection input. A2/CK and A1/RST pins are respectively connected to CCLK and CRST signals in “transparent mode” (see page 18). A0/3V is used for hardware activation to select CVCC voltage (3V or 5V). The slave address of the device is based on the value present on A2, A1, A0 on the rising edge of $\overline{\text{RESET}}$ pin (see Table 2). In fact, the address is taken internally at the 11th CLK rising edge.
PRES/$\overline{\text{INT}}$	EVCC	3 kV	O open-drain	Microcontroller Interface Function: Depending on IT_SEL value (see CONFIG4 register), PRES/$\overline{\text{INT}}$ outputs card presence status or interruptions (page 9) An internal Pull-up (typ 330kΩ,see Table 18)to EVCC can be activated in the pad if necessary using INT_PULLUP bit (CONFIG4 register). Remark: during power up and before registers configuration, the PRES/$\overline{\text{INT}}$ signal must be ignored.
$\overline{\text{RESET}}$	VCC	3 kV	I/O open-drain	Microcontroller Interface Function: • Power-on reset • A low level on this pin keeps the AT83C24 under reset even if applied on power-on. It also resets the AT83C24 if applied when the AT83C24 is running (see Power monitoring §). • Asserting $\overline{\text{RESET}}$ when the chip is in Shut-down mode returns the chip to normal operation. • AT83C24 is driving the $\overline{\text{Reset}}$ pin Low on power-on-reset or if power fail on V_{CC} or DVCC (see POWERMON bit in CONFIG4 register), this can be used to reset or interrupt other devices. After reset, AT83C24 needs to be reconfigured before starting a new card session.

Table 1. Ports Description (Continued)

Pad Name	Pad Internal Power Supply	ESD Limits	Pad Type	Description
SDA	VCC	3 kV	I/O open-drain	Microcontroller Interface Function TWI serial data
SCL	VCC	3 kV	I/O open-drain	Microcontroller Interface Function TWI serial clock
I/O	EVCC	3 kV	I/O	Microcontroller Interface Function Copy of CIO pin and high level reference for EVCC. An external pull up to EVCC is needed on IO pin. I/O is the reference level for EVCC if EVCC is connected to a capacitor. This feature is unused if EVCC is connected to VCC.
C4	EVCC	3 kV	I/O (pull-up)	Microcontroller Interface Function Copy of Card CC4.
C8	EVCC	3 kV	I/O (pull-up)	Microcontroller Interface Function Copy of Card CC8.
CLK	EVCC	3 kV	I	Microcontroller Interface Function Master Clock
CIO	CVCC	8 kV+	I/O (pull-up)	Smart card interface function Card I/O
CC4	CVCC	8 kV+	I/O (pull-up)	Smart card interface function Card C4
CC8	CVCC	8 kV+	I/O (pull-up)	Smart card interface function Card C8
CPRES	VCC	8 kV+	I (pull-up)	Smart card interface function Card presence An internal Pull-up to VCC can be activated in the pad if necessary using PULLUP bit (CONFIG1 register).
CCLK	CVCC	8 kV+	O	Smart card interface function Card clock
CRST	CVCC	8 kV+	O	Smart card interface function Card reset
$\overline{\text{CMDVCC}}$	EVCC	3 kV+	I (pull-up)	Microcontroller Interface Function: Activation/Shutdown of the smart card Interface.
VCC		3 kV+	PWR	Supply Voltage V_{CC} is used to power the internal voltage regulators and I/O buffers.
LI		3 kV+	PWR	DC/DC Input LI **must be** tied to VCC pin through an external coil (typically 4.7 µH) and provides the current for the charge pump of the DC/DC converter. It may be directly connected to VCC if the step-up converter is not used (see STEPREG bit in CONFIG4 register and see minimum VCC values in Table 20 (class A) and Table 21 (class B)).

Table 1. Ports Description (Continued)

Pad Name	Pad Internal Power Supply	ESD Limits	Pad Type	Description
CVCC		8 kV+	PWR	Card Supply Voltage CVCC is the programmable voltage output for the Card interface. It must be connected to external decoupling capacitors (see page 35 and page 36).
CVCCin		8 kV+	PWR	Card Supply Voltage This pin must be connected to CVCC.
DVCC		3 kV+	PWR	Digital Supply Voltage Is internally generated and used to supply the digital core. This pin has to be connected to an external capacitor of 100 nF and should not be connected to other devices.
EVCC		3 kV+	PWR	Extra Supply Voltage (Microcontroller power supply) EVCC is used to supply the internal level shifters of host interface pins. EVCC voltage can be supplied from the external EVCC pin connected to the host power supply. If EVCC cannot be connected to the host power supply, it must be tied to an external capacitor. EVCC voltage can be generated internally by an automatic follow up of the logic high level on the I/O pin. In this configuration, connect a 100 nF + 100kOhms in parallel between EVCC pin and VSS pin.
CVSS		8 kV+	GND	DC/DC Ground CVSS is used to sink high shunt currents from the external coil.
VSS			GND	Ground

Note: ESD Test conditions: 3 positive and 3 negative pulses on each pin versus GND. Pulses generated according to Mil/STD 883 Class3. Recommended capacitors soldered on CVCC and VCC pins.

Operational Modes

TWI Bus Control

The Atmel Two-wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format.

The TWI-bus interface can be used:

- To configure the AT83C24
- To select the operating mode of the card: 1.8V, 3V or 5V
- To configure the automatic activation sequence
- To start or stop sessions (activation and de-activation sequences)
- To initiate a warm reset
- To control the clock to the card in active mode
- To control the clock to the card in stand-by mode (stop LOW, stop HIGH or running)
- To enter or leave the card stand-by or power-down modes
- To select the interface (connection to the host I/O / C4/ C8)
- To request the status (card present or not, over-current and out of range supply voltage occurrence)
- To drive and monitor the card contacts by software
- To accurately measure the ATR delay when automatic activation is used

TWI Commands

Frame Structure

The structure of the TWI bus data frames is made of one or a series of write and read commands completed by STOP.

Write commands to the AT83C24 have the structure:

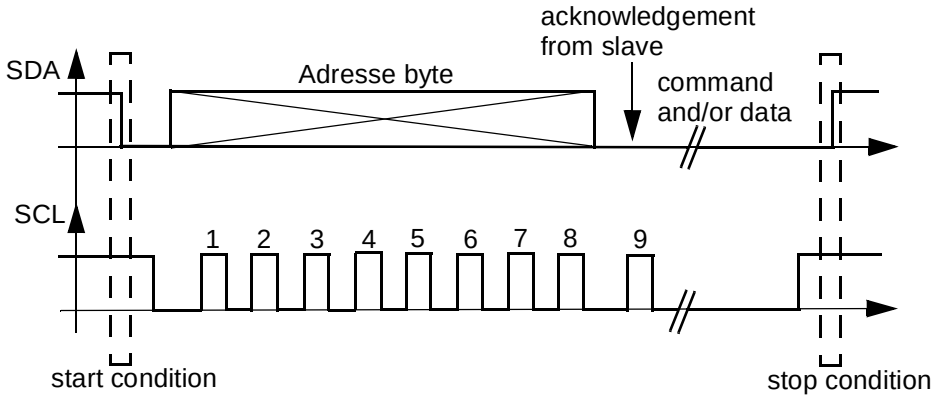
ADDRESS BYTE + COMMAND BYTE + DATA BYTE(S)

Read commands to the AT83C24 have the structure:

ADDRESS BYTE + DATA BYTE(S)

The ADDRESS BYTE is sampled on A2/CK, A1/RST, A0/3V after each reset (hard/soft/general call) but A2/CK, A1/RST, A0/3V can be used for transparent mode after the reset.

Figure 1. Data transfer on TWI bus



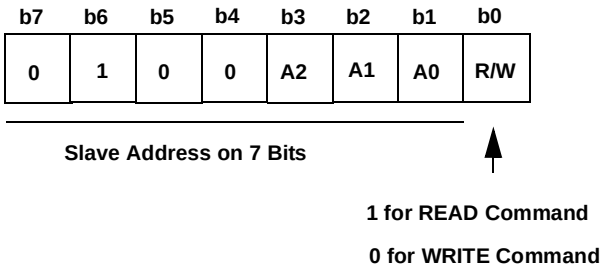
Address Byte

The first byte to send to the device is the address byte. The device controls if the hardware address (A2/CK, A1/RST, A0/3V pins on reset) corresponds to the address given in the address byte (A2, A1, A0 bits).

If the level is not stable on A2/CK pin (or A1/RST pin, or A0/3V pin) at reset, the user has to send the commands to the possible address taken by the device.

If A2/CK to A0/3V are tied to the host microcontroller and their reset values are unknown, a general call on the TWI bus allows to reset all the AT83C24 devices and set their address after A2/CK to A0/3V are fixed.

Figure 2. Address Byte



Up to 8 devices can be connected on the same TWI bus. Each device is configured with a different combination on A2/CK, A1/RST, A0/3V pins. The corresponding address byte values for read/write operations are listed below.

Table 2. Address Byte Values

A2 (A2/CK pin)	A1 (A1/RST pin)	A0 (A0/3V pin)	Address Byte for Read Command	Address Byte for Write Command
0	0	0	0x41	0x40
0	0	1	0x43	0x42
0	1	0	0x45	0x44
0	1	1	0x47	0x46
1	0	0	0x49	0x48
1	0	1	0x4B	0x4A
1	1	0	0x4D	0x4C
1	1	1	0x4F	0x4E

Write Commands

The write commands are:

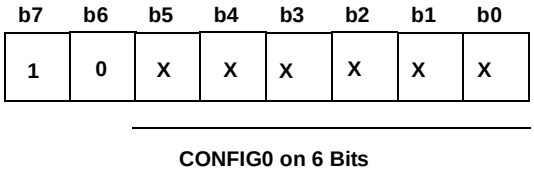
1. Reset:

   Initializes all the logic and the TWI interface as after a power-up or power-fail reset. If a smart card is active when RESET falls, a deactivation sequence is performed. This is a one-byte command.

2. Write Config:

   Configures the device according to the last six bits in the CONFIG0 register and to the following four bytes in CONFIG1, CONFIG2, CONFIG3 then CONFIG4 registers. This is a five bytes command.

Figure 3. Command byte format for Write CONFIG0 command



3. Write Timer:

   Program the 16-bit automatic reset transition timer with the following two bytes. This is a three bytes command.

4. Write Interface:

   Program the interface. This is a one-byte command. The MSB of the command byte is fixed at 0.

5. General Call Reset:

   A general call followed by the value 06h has the same effect as a Reset command.

Table 3. Write Commands Description

	Address Byte (See Table 2)	Command Byte	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4
1. Reset	0100 $A_2A_1A_0$0	1111 1111				
2. Write config	0100 $A_2A_1A_0$0	(10 + CONFIG0 6 bits)	CONFIG1	CONFIG2	CONFIG3	CONFIG4
3. Write Timer	0100 $A_2A_1A_0$0	1111 1100	TIMER1	TIMER0		
4. Write Interface	0100 $A_2A_1A_0$0	(0+INTERFACE 7 bits)				
5. General Call Reset	0000 0000	0000 0110				

Read Command

After the slave address has been configured, the read command allows to read one or several bytes in the following order:

- STATUS, CONFIG0, CONFIG1, CONFIG2, CONFIG3, INTERFACE, TIMER1, TIMER0, CAPTURE1, CAPTURE0
- FFh is completing the transfer if the microcontroller attempts to read beyond the last byte.

Note: Flags are only reset after the corresponding byte read has been acknowledged by the master.

Table 4. Read Command Description

Byte Description	Byte Value
Address byte	0100 $A_2A_1A_0$1
Data byte 1	STATUS
Data byte 2	CONFIG0
Data byte 3	CONFIG1
Data byte 4	CONFIG2
Data byte 5	CONFIG3
Data byte 6	CONFIG4
Data byte 7	INTERFACE
Data byte 8	TIMER 1 (MSB)
Data byte 9	TIMER 0 (LSB)
Data byte 10	CAPTURE 1 (MSB)
Data byte 11	CAPTURE 0 (LSB)
Data byte 12	0xFF

Interrupts

The PRES/$\overline{INT}$ behavior depends on IT_SEL bit value (see CONFIG4 register).

- If IT_SEL= 0, the PRES/$\overline{INT}$ output is High by default (on chip pull up or open drain). PRES/$\overline{INT}$ is driven Low by any of the following event:
  - INSERT bit set in CONFIG0 register (card insertion/extraction or bit set by software)
  - VCARD_INT bit set in STATUS register (the DC/DC output voltage has settled)
  - over-current detection on CVCC
  - VCARDERR bit set in CONFIG0 register (out of range voltage on CVCC or bit set by software)
  - ATRERR bit set in CONFIG0 register (no ATR before the card clock counter overflows or bit set by software).This control of ATR timing is only available if ART bit =1.

If IT_SEL=0, a read command of STATUS register and of CONFIG0 register will release PRES/$\overline{INT}$ pin to high level.

Several AT83C24 devices can share the same interrupt and the microcontroller can identify the interrupt sources by polling the status of the AT83C24 devices using TWI commands.

- If IT_SEL= 1 (mandatory for NDS applications and for software compatibility with existing devices) the PRES/INT output is High to indicate a card is present and none of the following event has occured:
  - over-current detection on CVCC
  - VCARDERR bit set in CONFIG0 register (out of range voltage on CVCC or bit set by software)

Card Presence Detection

The card presence is provided by the CPRES pin. The polarity of card presence contact is selected with the CARDDET bit (see CONFIG1 register). A programmable filtering is controlled with the CDS[2-0] bits (see CONFIG1 register).

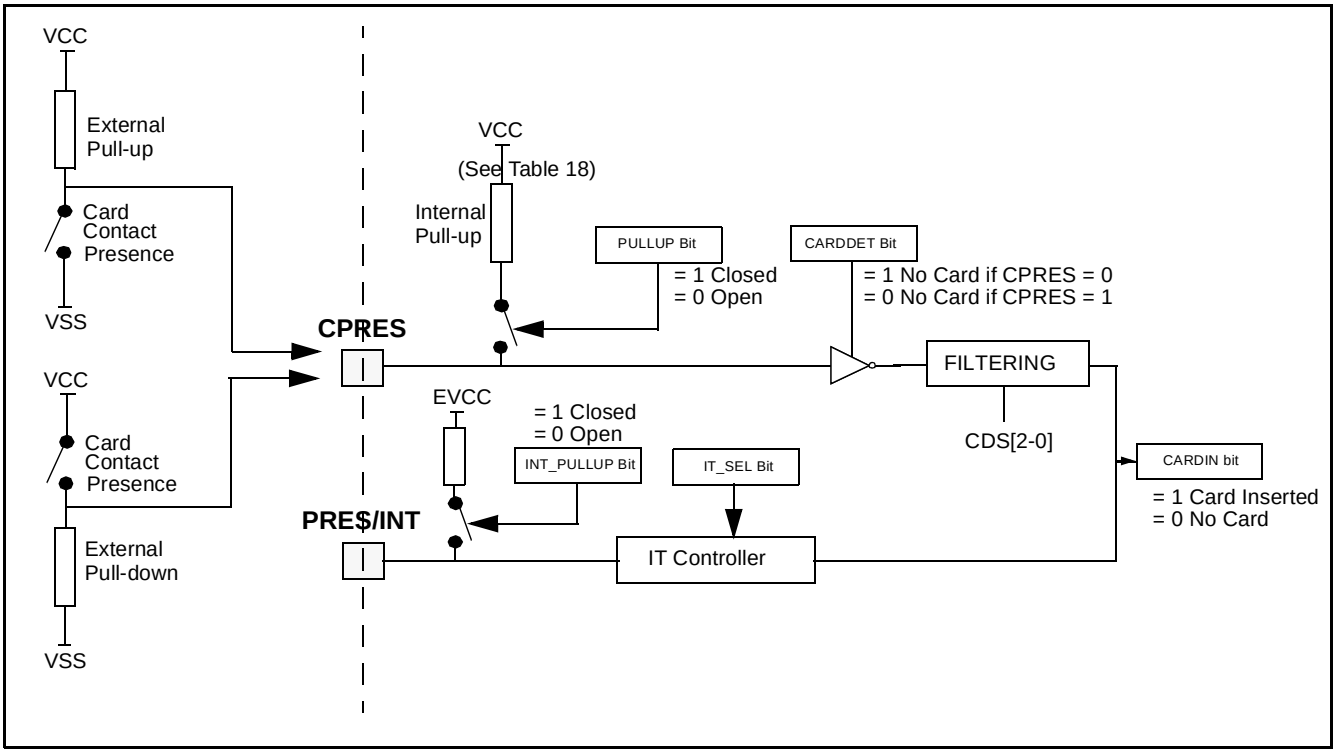
An internal pull-up on the CPRES pin can be disconnected in order to reduce the consumption, an external pull-up must then be connected to VCC. The PULLUP bit (see CONFIG1 register) controls this feature.

The card presence switch is usually connected to Vss (card present if CPRES=1). The CARDDET bit must be set. The internal pull up can be connected.

If the card presence contact is connected to Vcc (card present if CPRES=0), the internal pull-up must be disconnected (see PULLUP bit) and an external pull-down must be connected to the CPRES pin.

An interrupt can be generated if a card is inserted or extracted (see interrupts §).

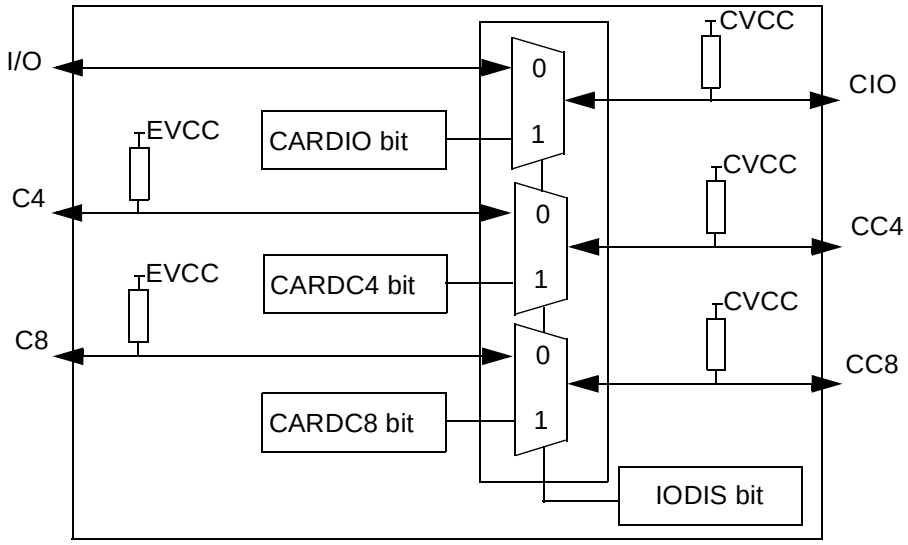
Figure 4. Card Presence Input



CIO, CC4, CC8 Controller

The CIO, CC4, CC8 output pins are driven respectively by CARDIO, CARDC4, CARDC8 bits values or by I/O, C4, C8 signal pins. This selection depends of the IODIS bit value. If IODIS is reset, data are bidirectional between respectively I/O, C4, C8 pins and CIO, CC4, CC8 pins.

Figure 5. CIO, CC4, CC8 Block Diagram



IO and CIO pins are linked together through the on chip level shifters if IODIS bit=0 in INTERFACE register. This is done automatically during an hardware activation.

Their iddle level are 1. With IO high, CIO is pulled up.

The same behavior is applicable on C4/ CC4 and C8/ CC8 pins.

The maximum frequency on those lines depends on CLK frequency (3 clock rising edges to transfer). With CLK=27MHz, the maximum frequency on this line is 1.5MHz.

Due to the minimum transfer delay allowed for NDS applications, the CLK minimum frequency is 18MHz.

Clock Controller

The clock controller generates two clocks (as shown in Figure 6 and Figure 7):

1. a clock for the CCLK: Four different sources can be used: CLK pin, DCCLK signal, CARDCK bit or A2/CK pin (in transparent mode).
2. a clock for DC/DC converter.

Figure 6. Clock Block Diagram with Software Activation (see page 14)

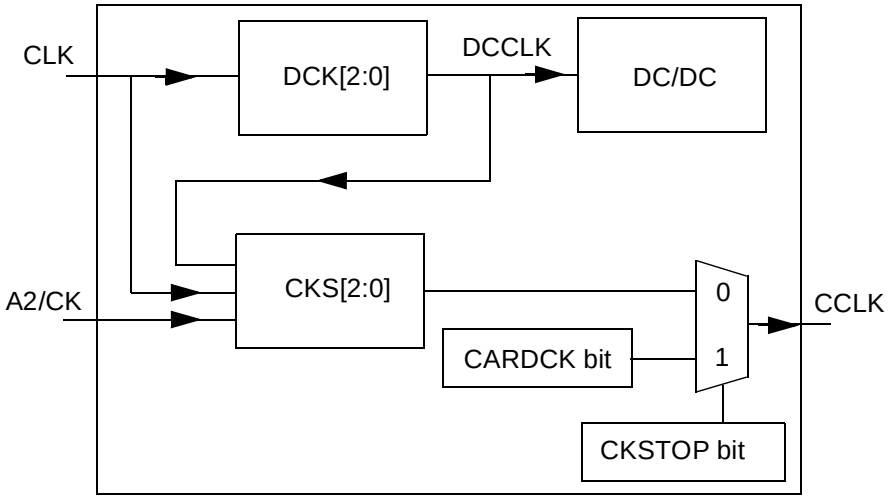
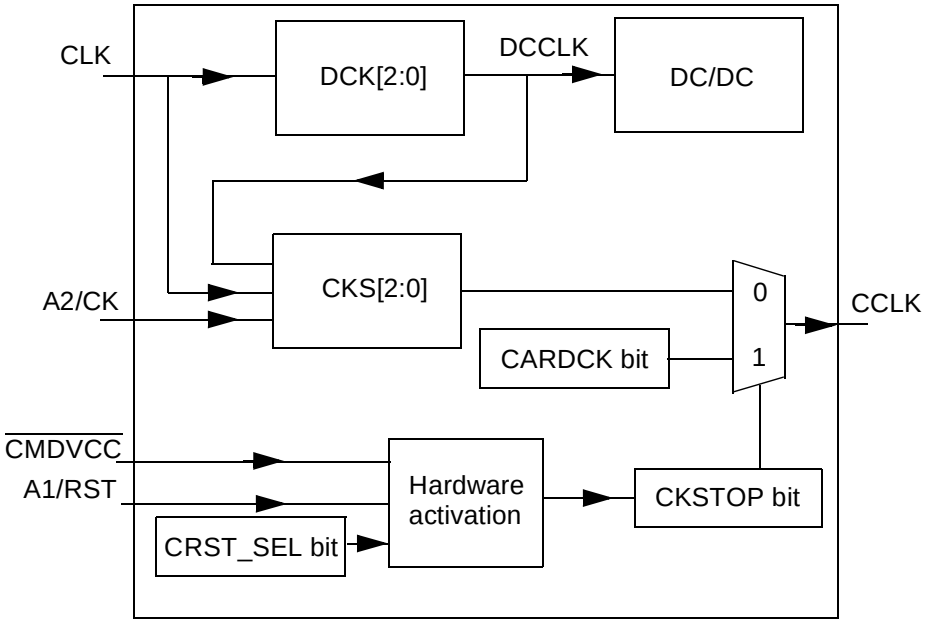


Figure 7. Clock Block Diagram with Hardware Activation (see page 14)



CRST Controller

The CRST output pin is driven by the A1/RST pin signal pin or by the CARDRST bit value. This selection depends of the CRST_SEL bit value (see CONFIG4 register).

If the CRST pin signal is driven by the CARDRST bit value, two modes are available:

- If the ART bit is reset, CRST pin is driven by CARDRST bit.
- If the ART bit is set, CRST pin is controlled and follows the “Automatic Reset Transition” (page 15).

Figure 8. CRST Block Diagram with soft activation

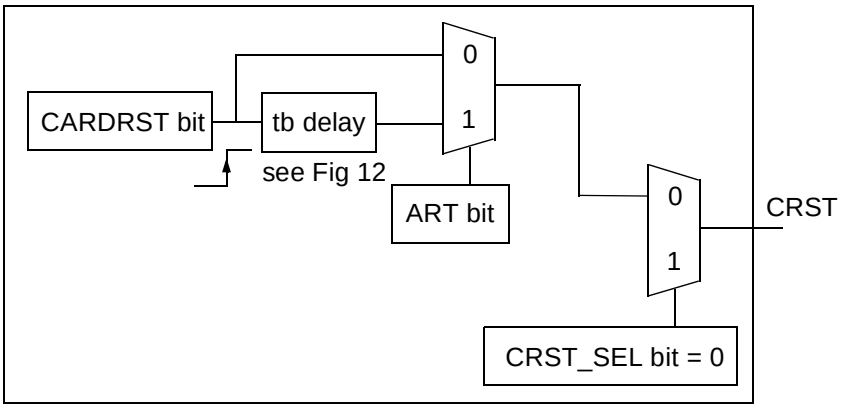
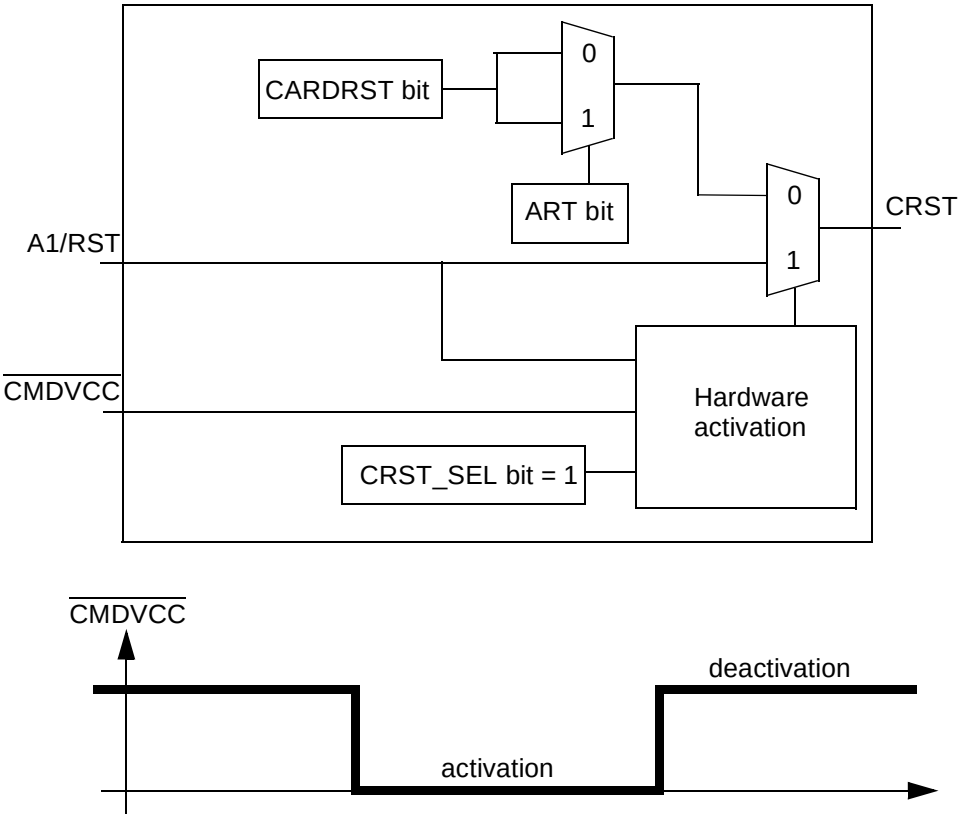


Figure 9. CRST Block Diagram with Hardware Activation ($\overline{\text{CMDVCC}}$ pin used)



Activation Sequence

Hardware Activation (DC/DC started with $\overline{\text{CMDVCC}}$)

Initial conditions:

CARDDET bit must be configured in accordance to the smart card connector polarity.

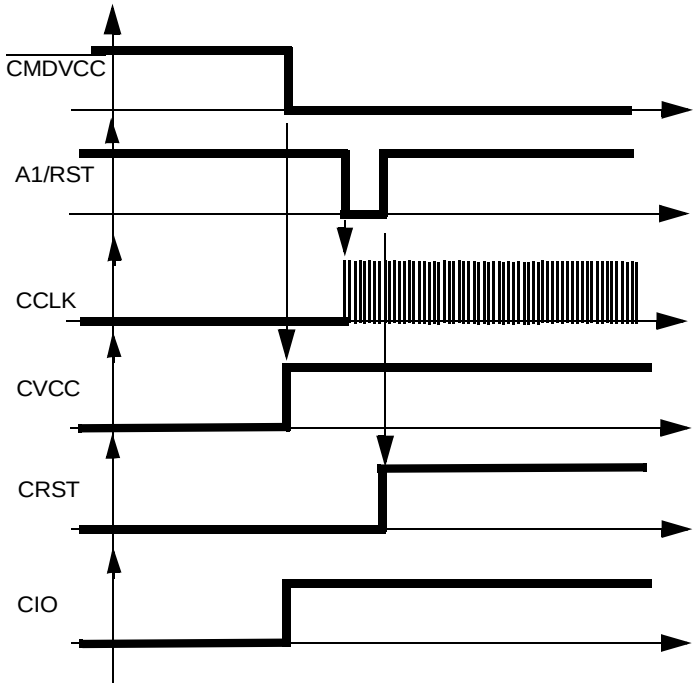
IT_SEL bit, CRST_SEL bit (see CONFIG4 register) must be set and CARDRST bit (see INTERFACE register) must be cleared. A smart card must be detected to enable to start the DC/DC (CVCC= 3V or 5V).

The hardware activation sequence is started by hardware with $\overline{\text{CMDVCC}}$ pin going high to low. It follows this **automatic** sequence:

- CIO / CC4 / CC8 and IO / C4 / C8 are respectively linked together (IODIS bit is cleared).
- The DC/DC is started and CVCC is set according to the A0/3V pin: 5V (Class A) if A0/3V is High and 3V (Class B) is A0/3V is Low.
- CCLK signal is enabled (CKSTOP bit cleared) when CVCC has settled to the programmed voltage (see Electrical Characteristics) and the level on A1/RST is 0. The CCLK source can be DCCLK signal, CLK signal , A2/CK signals or CARDCK bit (see Figures 5).
- CRST signal is linked with A1/RST pin as soon as A1/RST pin level is 0. A rising edge on A1/RST pin set the CRST pin.

Note: 1. The card must be deactivated to change the voltage.

Figure 10. Activation sequence with $\overline{\text{CMDVCC}}$



Note: For NDS applications, the host usually starts activation with A1/RST = 0.

Software Activation (DC/DC Started With Writing in VCARD[1:0] bits) and ART bit = 1

Initial conditions: CARDRST bit = 0, CKSTOP bit =1, IODIS bit = 1.

The following sequence can be applied:

1. Card Voltage is set by software to the required value (VCARD[1:0] bits in CONFIG0 register). This writing starts the DC/DC.
2. Wait the end of the DC/DC init with a polling on VCARDOK bit (STATUS register) or wait for PRES/INT to go Low if enabled (if IT_SEL bit = 0 in CONFIG4 register). When VCARDOK bit is set (by hardware), CARDIO bit should be set by software.
3. CKSTOP, IODIS are programmed by software. CKSTOP bit is reset to have the clock running. IODIS is reset to drive the I/O, C4, C8 pins and the CIO,CC4, CC8 pins according to each other.
4. CARDRST bit (see INTERFACE register) is set by software.

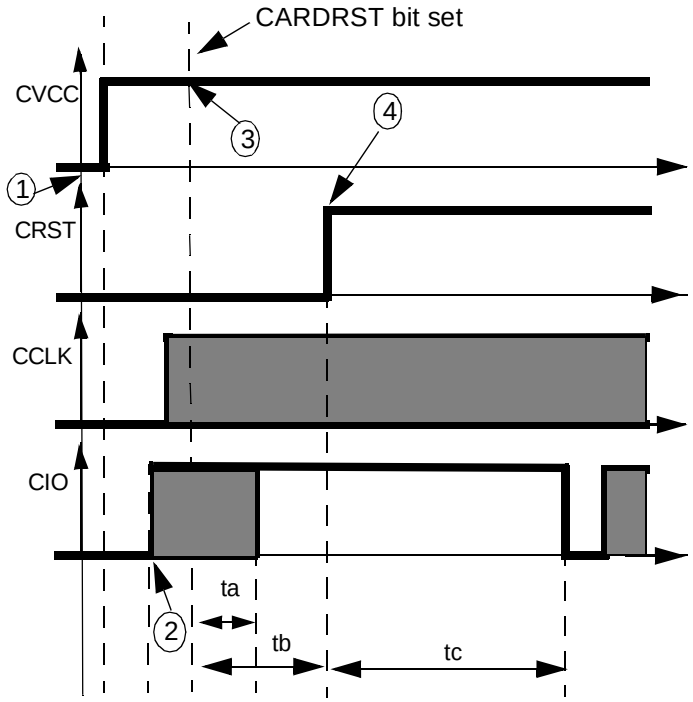
Automatic Reset Transition description:

A 16-bit counter starts when CARDRST bit is set. It counts card clock cycles. The CRST signal is set when the counter reaches the TIMER[1-0] value which corresponds to the “tb” time (Figure 11).The counter is reseted when the CRST pin is released and it is stopped at the first start bit of the Answer To Request (ATR) on CIO pin.

The CIO pin is not checked during the first 200 clock cycles (ta on Figure 11). If the ATR arrives before the counter reaches Timer[1-0] value, the activation sequence fails, the CRST signal is not set and the Capture[1-0] register contains the value of the counter at the arrival of the ATR.

If the ATR arrives after the rising edge on CRST pin and before the card clock counter overflows (65535 clock cycles), the activation sequence completes. The Capture[1-0] register contains the value of the counter at the arrival of the ATR (tc time on Figure 11).

Figure 11. Software activation with ART bit = 1



ISO 7816 constraints: ta = 200 card clock cycles

400 card clock cycles< = tb

400 card clock cycles< = tc < = 40000 card clock cycles

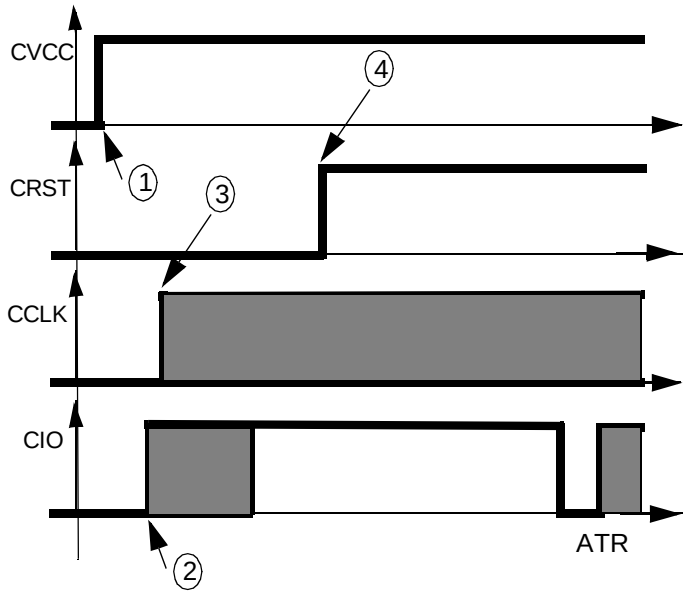
Note: Timer[1-0] reset value is 400.

Software Activation (DC/DC Started by Writing in VCARD[1:0] bits) and ART bit = 0

The activation sequence is controlled by software using TWI commands, depending on the cards to support. For ISO 7816 cards, the following sequence can be applied:

1. Card Voltage is set by software to the required value (VCARD[1:0] bits in CONFIG0 register). This writing starts the DC/DC.
2. Wait of the end of the DC/DC init with a polling on VCARDOK bit (STATUS register) or wait for PRES/INT to go Low if enabled (if IT_SEL bit = 0 in CONFIG4 register). When VCARDOK bit is set (by hardware), CARDIO bit should be set by software.
3. CKSTOP, IODIS are programmed by software. CKSTOP bit is reset to have the clock running. IODIS is reset to drive the I/O, C4, C8 pins and the CIO,CC4, CC8 pins according to each other.
4. CRST pin is controlled by software using CARDRST bit (see INTERFACE register).

Figure 12. Software activation without automatic control (ART bit = 0)



Note: It is assumed that initially VCARD[1:0], CARDCK, CARDIO and CARDRST bits are cleared, CKSTOP and IODIS are set (those bits are further explained in the registers description)

Note: The user should check the AT83C24 status and possibly resume the activation sequence if one TWI transfer is not acknowledged during the activation sequence.

Deactivation Sequence

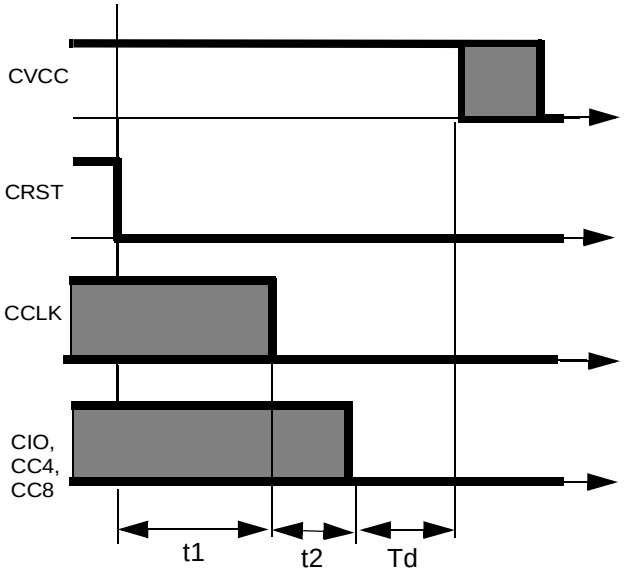
The card automatic deactivation is triggered when one the following condition occurs:

- ICARDERR bit is set by hardware
- VCARDERR bit is set by hardware (or by software)
- INSERT is set and CARDIN is cleared (card extraction)
- SHUTDOWN is set by software
- $\overline{\text{CMDVCC}}$ goes from Low to High
- Power fail on VCC (see POWERMON bit in CONFIG4 register)
- Reset pin going low

It is a self-timed sequence which cannot be interrupted when started (see Figure 13). Each step is separated by a delay based on Td equal to 8 periods of the DC/DC clock, typically 2 µs:

1. T0: CARDRST is cleared, SHUTDOWN bit set.
2. T0 + 5 x Td:CARDCK is cleared, CKSTOP, CARDIO and IODIS are set.
3. T0 + 6 x Td: CARDIO is cleared.
4. T0 + 7 x Td: VCARD[1-0] = 00.

Figure 13. Deactivation Sequence



Notes: 1. Setting ICARDERR by software does not trigger a deactivation. VCARDERR can be used to deactivate the card by software.
2. t1=5 to 5.5*Td, and t2=0.5*Td to Td.

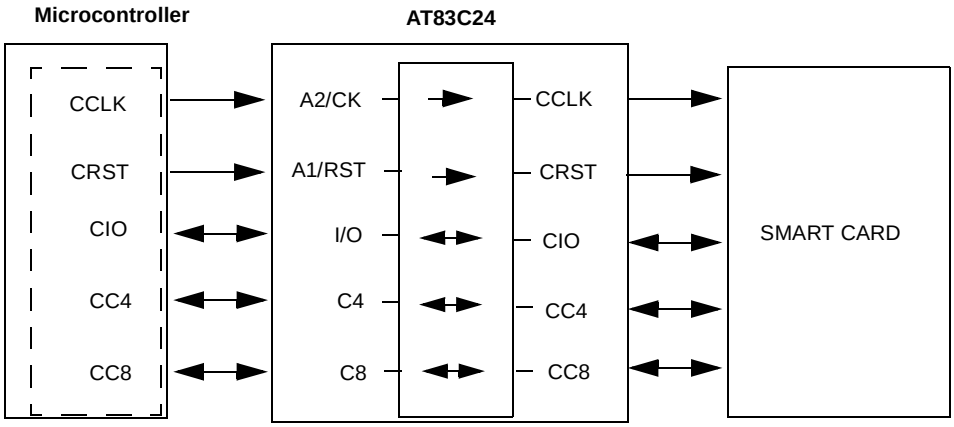
Transparent Mode

If the microcontroller outputs ISO 7816 signals, a transparent mode allows to connect RST/CLK and I/O/C4/C8 signals after an electrical level control. The AT83C24 level shifters adapt the card signals to the smart card voltage selection.

The CRST and CCLK microcontroller signals can be respectively connected to the A1/RST and A2/CK pins.

The CRST_SEL bit (in CONFIG4 register) selects standard or transparent configuration for the CRST pin. CKS in CONFIG2 allows to select standard or transparent configuration for the CCLK pin. So CCLK and CRST are independent. A2/CK to A0/3V inputs always give the TWI address at reset. The A0/3V pin can be used for TWI addressing and easily connect two AT83C24 devices on the same TWI bus.

Figure 14. Transparent Mode Description



Power Modes

Two power-down modes are available to reduce the AT83C24 power consumption (see STUTDOWN bit in CONFIG1 register and LP bits in CONFIG3 register).

To enter in the mode number 4 (see Table 5), the sequence is the following:

- First select the Low-power mode by setting the LP bit
- The activation of the SHUTDOWN bit can then be done.

The AT83C24 exits Power-down if a software/hardware reset is done or if SHUTDOWN bit is cleared. The AT83C24 is then active immediately.

Either a hardware reset or a TWI command clearing the SHUTDOWN bit can cause an exit from Power-down. The internal registers retain their value during the shutdown mode.

In Power-down mode, the device is sleeping and waiting for a wake up condition.

To reduce power consumption, the User should stop the clock on the CLK input after setting the SHUTDOWN bit. The clock can be enabled again just before exiting SHUTDOWN (at least 10 µs before a START bit on SDA).

Table 5. Power Modes Description

Mode Number	Shutdown Bit	LP Bit	STEPREG	VCARD[1:0]	Typical Supply Current	Description
1	0	X	0	11	160 mA 30 mA	Step up mode: VCC = 3V, CVCC = 5V, Icard = 65mA Icard = 0
2	0	X	1	11	70 mA	Regulator mode: VCC = 5.25V, CVCC = 5V, Icvcc = 65mA
3	0	X	X	00	3 mA	DC/DC off, CLK = 10MHz, VCC=3V to 5V
4	1	0	X	00	90 µA	The TWI interface of the AT83C24 is active but its analog blocs are switched off to reduce the consumption
5	1	1	X	00	30 µA	Pulsed mode of the internal 3V logic regulator

Power Monitoring

The AT83C24 needs only one power supply to run: VCC.

If the microcontroller outputs signals with a different electrical level, the host positive supply is connected to EVCC.

EVCC and VCC pins can be connected together if they have the same voltage.

- If EVCC and VCC have different electrical levels:

  The EVCC pin and RESET pin should be connected with a resistor bridge. RESET pin high level must be higher than VIH (see Table 19). When EVCC drops, RESET pin level drops too. A deactivation sequence starts if a card was active.

Then the AT83C24 resets if RESET pin stays low.

- If EVCC and VCC have the same value, then they should be connected:

  The AT83C24 integrates an internal 3V regulator to feed its logic from the VCC supply. The bit powermon allows the user to select if the internal PFD monitors VCC or the internal regulated 3V. If the PFD monitors VCC (POWERMON bit=0), a deactivation is performed if VCC falls below VPFDP (see VPFDP value in the datasheet). Same deactivation is performed if the internal 3V falls below VPFDP and POWERMON bit = 1.

Registers

Table 6. CONFIG0 (Config Byte 0)

7	6	5	4	3	2	1	0
1	0	ATRERR	INSERT	ICARDERR	VCARDERR	VCARD1	VCARD0

Bit Number	Bit Mnemonic	Description
7-6	1-0	These bits cannot be programmed and are read as 1-0.
5	ATRERR	**Answer to Reset Interrupt** This bit is set when the card clock counter overflows (no falling edge on CIO is received before the overflow of the card clock counter). This bit is cleared by hardware when this register is read. It can be set by software for test purpose. The reset value is 0.
4	INSERT	**Card Insertion Interrupt** This bit is set when a card is inserted or extracted: a change in CARDIN value filtered according to CDS[2-0]. After power up, if the level on CPRES pin is 0, then INSERT bit is set. It can be set by software for test purpose. This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
3	ICARDERR	**Card Over Current Interrupt** This bit is set when an over current is detected on CVCC. It can be set by software for test purpose (no card deactivation is performed, no IT is performed). This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
2	VCARDERR	**Card Out of Range Voltage Interrupt** This bit is set when the output voltage goes out of the voltage range specified by VCARD field. It can be set by software for test purpose and deactivate the card. This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
1-0	VCARD[1:0]	**Card Voltage Selection** VCARD[1:0] = 00: 0V VCARD[1:0] = 01: 1.8V (see STEPREG bit) VCARD[1:0] = 10: 3V VCARD[1:0] = 11: 5V VCARD[1:0] writing to 1.8V, 3V, 5V starts the DC/DC if a card is detected. VCARD[1:0] writing to 0 stops the DC/DC. No card deactivation is performed when the voltage is changed between 1.8V, 3V or 5V. The microcontroller should deactivate the card before changing the voltage. The reset value is 00.

Table 7. CONFIG 1 (Config Byte 1)

7	6	5	4	3	2	1	0
X	ART	SHUTDOWN	CARDDET	PULLUP	CDS2	CDS1	CDS0

Bit Number	Bit Mnemonic	Description
7	X	This bit should not be set.
6	ART	**Automatic Reset Transition** Set this bit to have the CRST pin changed according to activation sequence. Clear this bit to have the CRST pin immediately following the value programmed in CARDRST. The reset value is 0.
5	SHUTDOWN	**Shutdown** Set this bit to reduce the power consumption. An automatic de-activation sequence will be done. Clear this bit to enable VCARD[1:0] selection. The reset value is 0.
4	CARDDET	**Card Presence Detection Polarity** Set this bit to indicate the card presence detector is closed when no card is inserted (CPRES is low). Clear this bit to indicate the card presence detector is open when no card is inserted (CPRES is high).Changing CARDDET will set INSERT bit (see CONFIG0) even if no card is inserted or extracted. The reset value is 0.
3	PULLUP	**Pull-up Enable** Set this bit to enable the internal pull-up on the CPRES pin. This allows to minimize the number of external components. Clear this bit to disable the internal pull-up and minimize the power consumption when the card detection contact is on. Then an external pull-up must be connected to V_{CC} (typically a 1 MΩ resistor). The reset value is 1.
2-0	CDS[2:0]	**Card Detection filtering** CPRES is sampled by the master clock provided on CLK input. A change on CPRES is detected after: CDS[2-0] = 0: 0 sample(1) CDS[2-0] = 1: 4 identical samples CDS [2-0] = 2: 8 identical samples (reset value) CDS[2-0] = 3: 16 identical samples CDS[2-0] = 4: 32 identical samples CDS[2-0] = 5: 64 identical samples CDS[2-0] = 6: 128 identical samples CDS[2-0] = 7: 256 identical samples The reset value is 2. Note: When CDS[2-0] = 0 and IT_SEL = 0, PRES/INT = 1 when no card is present and PRES/INT = 0 when a card is inserted even if CLK is STOPPED. This can be used to wake up the external microcontroller and restart CLK when a card is inserted in the AT83C24. If CDS[2-0] = 0, IT_SEL = 1 and CLK is stopped, a card insertion or extraction has no effect on PRES/INT pin.

Table 8. CONFIG2 (Config Byte 2)

7	6	5	4	3	2	1	0
X	DCK2	DCK1	DCK0	X	CKS2	CKS1	CKS0

Bit Number	Bit Mnemonic	Description
7	X	This bit should not be set.
6-4	DCK[2:0]	**DC/DC Clock prescaler factor** DCCLK is the DC/DC clock. It is the division of CLK input by DCK prescaler. DCK = 0: prescaler factor equals 1 (CLK = 4 to 4.61MHz) DCK [2:0] = 1: prescaler factor equals 2 (CLK = 7 to 9.25MHz) DCK [2:0] = 2: prescaler factor equals 4 (CLK = 14 to 18.5 MHz) DCK [2:0] = 3: prescaler factor equals 6 (CLK = 21 to 27.6 MHz) DCK [2:0] = 4: prescaler factor equals 8 (CLK = 28 to 34.8 MHz) DCK [2:0] = 5: prescaler factor equals 10 (CLK = 35 to 43 MHz) DCK [2:0] = 6: prescaler factor equals 12 (CLK = 43.1 to 48 MHz) DCK [2:0] = 7: reserved The reset value is 1. DCCLK must be as close as possible to 4 MHz with a duty cycle of 50%. DCK must be programmed before starting the DC/DC. The other values of CLK are not allowed. DCK has to be properly configured before resetting the STEPREG bit.
3	X	This bit should not be set.
2-0	CKS[2:0]	**Card Clock prescaler factor** CKS [2:0] = 0: CCLK = CLK (then the maximum frequency on CLK is 24 MHz) CKS [2:0] = 1: CCLK = DCCLK (DC/DC clock) CKS [2:0] = 2: CCLK = DCCLK / 2 CKS [2:0] = 3: CCLK = DCCLK / 4 CKS [2:0] = 4: CCLK = A2 CKS [2:0] = 5: CCLK = A2 / 2 CKS [2:0] = 6: CCLK = CLK / 2 CKS [2:0] = 7: CCLK = CLK / 4 The reset value is 0.

Notes:
1. When this register is changed, a special logic insures no glitch occurs on the CCLK pin and actual configuration changes can be delayed by half a period to two periods of CCLK.
2. CCLK must be stopped with CKSTOP bit before switching from CKS = (0, 1, 2, 3, 6, 7) to CKS = (4, 5) or vice versa.
3. When DCK = 0, only CKS=4 and CKS=5 are allowed.
4. The user can't directly select A2 or A2/2 after a reset or when switching from CKS = (0, 1, 2, 3, 6, 7) to CKS = (4, 5). To select A2, the user should select A2/2 first and after A2. To select A2/2, the user should select A2 first and after A2/2.

Table 9. CONFIG3 (Config Byte 3)

7	6	5	4	3	2	1	0
EAUTO	**VEXT1**	**VEXT0**	**ICCADJ**	**LP**	**X**	**X**	**X**

Bit Number	Bit Mnemonic	Description
7-5	EAUTO VEXT1 VEXT0	**EVCC voltage configuration:** EAUTO VEXT1 VEXT0 0 0 0 EVCC = 0 the regulator is switched off. 0 0 1EVCC = 2.3V 0 1 0 EVCC = 1.8V 0 1 1 EVCC = 2.7V 1 X X EVCC voltage is the level detected on I/O input pin. if EVCC is supplied from the external EVCC pin, the user can switch off the internal EVCC regulator to decrease the consumption. If EVCC is switched off, and no external EVCC is supplied, the AT83C24 is inactive until a hardware reset is done. The reset value is 100.
4	ICCADJ	**CI_{CC} overflow adjust** This bit controls the DC/DC sensitivity to any overflow current . Set this bit to decrease the DC/DC sensitivity (CI_{CC_ovf} is increased by about 20%, see Electrical Characteristics). The start of the DC/DC with a high current load is easier. Clear this bit to have a normal configuration. The reset value is 0.
3	LP	**Low-power Mode** Set this bit to enable low-power mode during shutdown mode (pulsed mode activated). Clear this bit to disable low-power mode during shutdown mode. The activation reference is the following: • First select the Low-power mode by setting LP bit. • The activation of SHUTDOWN bit can then be done. This bit as no effect when SHUTDOWN bit is cleared. The reset value is 0.
2	X	This bit should not be set.
1	X	This bit should not be set.
0	X	This bit should not be set.

Table 10. CONFIG4 (Config Byte 4)

7	6	5	4	3	2	1	0
X	X	X	STEPREG	INT_PULLUP	POWERMON	IT_SEL	CRST_SEL

Bit Number	Bit Mnemonic	Description
7-5	X-X-X	These bits should not be set.
4	STEPREG	**Step Regulator mode** Clear this bit to enable the automatic step-up converter (CVCC is stable even if VCC is not higher than CVCC). Set this bit to permanently disable the step-up converter (CVCC is stable only if VCC is sufficiently higher than CVCC). This bit must be set before activating the DC/DC converter if no external coil is present. The reset value is 0. This bit must always be set if no external coil is used
3	INT_PULLUP	**Internal pull-up** Set this bit to activate the internal pull-up (connected internally to EVCC) on PRES/$\overline{\text{INT}}$ pin. Clear this bit to deactivate the internal pull-up. PRES/$\overline{\text{INT}}$ is an open drain output with a programmable internal pull up. The reset value is 0.
2	POWERMON	**Power monitor** Set this bit to monitor any glitch on the Digital Supply Voltage (DVCC) of the AT83C24. Clear this bit to monitor any glitch on VCC. The reset value is 0.
1	IT_SEL	**Interrupt Select** Set this bit to disable INSERT and VCARD_INT interrupts. Then PRES/$\overline{\text{INT}}$ is pulled up when a card is present and no error is detected. Clear this bit to have all the interrupt sources enabled and active Low. **IT_SEL must be set to enable a hardware activation with $\overline{\text{CMDVCC}}$.** The reset value is 0.
0	CRST_SEL	**Card Reset Selection** Set this bit to have the CRST pin driven by hardware through the A1 pin (only with hardware activation). Clear this bit to have the CRST pin driven by software through the CARDRST bit. **CRST_SEL must be set when $\overline{\text{CMDVCC}}$ is used (hardware activation).** The reset value is 0.

Table 11. INTERFACE (Interface Byte)

7	6	5	4	3	2	1	0
0	IODIS	CKSTOP	CARDRST	CARDC8	CARDC4	CARDCK	CARDIO

Bit Number	Bit Mnemonic	Description
7	0	This bit should not be set.
6	IODIS	**Card I/O isolation** Set this bit to drive the CIO, CC4, CC8 pins according to CARDIO, CARDC4, CARDC8 respectively and to put I/O, C4, C8 in Hi-Z. This can be used to have the I/O, and C4 and C8 pins of the host communicating with another AT83C24 interface, while CIO, CC4 and CC8 are driven by software (or if the card is in standby or power-down modes). Clear this bit to drive the I/O/CIO, C4/CC4 and C8/CC8 pins according to each other. This can be used to activate asynchronous cards. The reset value is 1.
5	CKSTOP	**CARD Clock Stop** Set this bit to stop CCLK according to CARDCK. This can be used to set asynchronous cards in power-down mode (GSM) or to drive CCLK by software. Clear this bit to have CCLK running according to CKS. This can be used to activate asynchronous cards. Note: 1. When this bit is changed a special logic ensures that no glitch occurs on the CCLK pin and actual configuration changes can be delayed by half a period to two periods of CCLK. 2. CKSTOP must be set before switching on the DC/DC with VCARD[1:0]. The reset value is 1.
4	CARDRST	**Card Reset** Set this bit to enter a reset sequence according to ART bit value. Clear this bit to drive a low level on the CRST pin. The reset value is 0.
3	CARDC8	**Card C8** Set this bit to drive the CC8 pin High with the on-chip pull-up (according to IODIS bit value). The pin can then be an input (read in STATUS register). Clear this bit to drive a low level on the CC8 pin (according to IODIS bit value). The reset value is 0.
2	CARDC4	**Card C4** Set this bit to drive the CC4 pin High with the on-chip pull-up (according to IODIS bit value). The pin can then be an input (read in STATUS register). Clear this bit to drive a low level on the CC4 pin (according to IODIS bit value). The reset value is 0.
1	CARDCK	**Card Clock** Set this bit to set a high level on the CCLK pin (according to CKSTOP bit value). Clear this bit to drive a low level on the CCLK pin. The reset value is 0.
0	CARDIO	**Card I/O** Set this bit to drive the CIO pin High with the on-chip pull-up (according to IODIS bit value). The pin can then be an input (read in STATUS register). Clear this bit to drive a low level on the CIO pin (according to IODIS bit value). The reset value is 0.

Table 12. STATUS (Status Byte)

7	6	5	4	3	2	1	0
CC8	CC4	CARDIN	VCARDOK	X	VCARD_INT	CRST	CIO

Bit Number	Bit Mnemonic	Description
7	CC8	**Card CC8** This bit provides the actual level on the CC8 pin when read. The reset value is 0.
6	CC4	**Card CC4** This bit provides the actual level on the CC4 pin when read. The reset value is 0.
5	CARDIN	**Card Presence Status** This bit is set when a card is detected. It is cleared otherwise.
4	VCARD_OK	**Card Voltage Status** This bit is set by the DCDC when the output voltage remains within the voltage range specified by VCARD[1:0] bits. It is cleared otherwise. The reset value is 0.
3	X	This bit should not be set.
2	VCARD_INT	Card voltage interrupt This bit is set when VCARD_OK bit is set. This bit is cleared when read by the microcontroller. The reset value is 0.
1	CRST	**Card RST** This bit provides the actual level on the CRST pin when read. The reset value is 0.
0	CIO	**Card I/O** This bit provides the actual level on the CIO pin when read. The reset value is 0.

Table 13. TIMER 1 (Timer MSB)

7	6	5	4	3	2	1	0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Bit Number	Bit Mnemonic	Description
7 - 0	Bits 15 - 8	Timer MSB (bits 15 to 8)

Reset value = 0x00000001

Table 14. TIMER 0 (Timer LSB)

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Number	Bit Mnemonic	Description
7 - 0	bits 7 - 0	Timer LSB (bits 7to 0)

Reset value = 0x10010000

Table 15. CAPTURE 1 (Capture MSB)

7	6	5	4	3	2	1	0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

Bit Number	Bit Mnemonic	Description
7 - 0	bits 15 - 8	See “software activation with ART = 1”, page 15.

Reset value = 0x00000000

Table 16. CAPTURE 0 (Capture LSB)

7	6	5	4	3	2	1	0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit Number	Bit Mnemonic	Description
7 - 0	bits 7 - 0	See “software activation with ART = 1”, page 15.

Reset value = 0x00000000

Electrical Characteristics

Absolute Maximum Ratings *

Ambient Temperature Under Bias:	-40°C to 85°C
Storage Temperature:	-65°C to +150°C
Voltage on VCC:	V_{SS} -0.5V to +6.0V
Voltage on SCIB pins (***):	CVSS -0.5V to CVCC + 0.5V
Voltage on host interface pins:	VSS -0.5V to EVCC + 0.5V
Voltage on other pins:	VSS -0.5V to VCC + 0.5V
Power Dissipation:	1.5W
Thermal resistor of QFN package..(**):	35°C/W
Thermal resistor of SO package:	48°C/W

*NOTICE: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
Power Dissipation value is based on the maximum allowable die temperature and the thermal resistance of the package.

(**) Exposed die attached pad must be soldered to ground

Thermal resistor are measured on multilayer PCB with 0 m/s air flow.

(***) including shortages between any groups of smart card pins.

AC/DC Parameters

EVCC connected to host power supply: from 1.6V to 5.5V.

T_A = -40°C to +85°C; V_{SS} = 0V; V_{CC} = 3V to 5.5V.

CLASS A card supplied with CVCC = 4.75 to 5.25V for AT83C24NDS

CLASS A card supplied with CVCC = 4.6 to 5.25V for AT83C24

CLASS B card supplied with CVCC = 2.8V to 3.2V

CLASS C card supplied with CVCC = 1.68V to 1.92V

Table 17. Core (VCC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{PFDP}	Power fail high level threshold	2.4	2.5	2.6	V	
V_{PFDM}	Power fail low level threshold	2.25	2.35	2.45	V	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1 µs		600s		Not tested.

Table 18. Host Interface (I/O, C4, C8, CLK, A2, A1, A0, $\overline{\text{CMDVCC}}$, PRES/$\overline{\text{INT}}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low-voltage	-0.5		0.3 x EVCC 0.25 x EVCC	V	EVCC from 2.7V to VCC EVCC from 1.6 to 2.7V
V_{IH}	Input High Voltage	0.7 x EVCC		EVCC + 0.5	V	EAUTO=0 EAUTO=1 EVCC from 1.6V to VCC

Table 18. Host Interface (I/O, C4, C8, CLK, A2, A1, A0, $\overline{\text{CMDVCC}}$, PRES/$\overline{\text{INT}}$) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low-voltage (I/O, C4, C8, PRES/$\overline{\text{INT}}$)			0.05 0.4	V V	I_{OL} = -100 µA I_{OL} = -1.2 mA
V_{OH}	Output High Voltage (C4, C8, PRES/$\overline{\text{INT}}$) V_{OH} on I/O depends on external pull up value	0.8 x EVCC		EVCC	V	EVCC from 1.6V to VCC I_{OH} = 100 µA
EI_{CC}	Extra Supply Current			+3	mA	C_L = 100 nF
$R_{PRES/INT}$	PRES/$\overline{\text{INT}}$ weak pull-up output current	300	330	360	kΩ	Short to VSS INT_PULLUP = 0: Internal pull-up active.
EVCC	EVCC pin not connected to a power supply	Vpeak - 10 mV	Vpeak	Vpeak + 25 mV	V	C_L = 100 nF, EIcc = +3 mA Vpeak on I/O from 1.6V to VCC EAUTO = 1: min duration 1µs, min frequency 0.1Hz, spikes <50ns are filtered.
EVCC	EVCC pin connected to a power supply	Vpeak - 200mV				EAUTO = 1
CLK	Clock signal for AT83C24	4		48	MHz	If DCK[2:0] =0 (CLK=4MHz to 4.61MHz), a duty cycle of 50% is needed.
CLK	Clock signal for AT83C24NDS	18		48	MHz	no constrainst on duty cycle

Table 19. Host Interface (SCL, SDA, RESET)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low-voltage	-0.5		1.9 0.3 x VCC	V	VCC > 4.5V VCC <= 4.5V
V_{IH}	Input High Voltage	3 0.7 x VCC		VCC + 0.5	V	VCC > 4.5V VCC <= 4.5V
V_{OL}	Output Low-voltage			0.4	V	I_{OL} = -3 mA
V_{HIST}	Input trigger hysteresis	0.1 x VCC				

Table 20. Smart Card Class A

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current Capability	65 65			mA	VCC=3V to 5.5V, STEPREG=0 VCC > 5.35V, STEPREG = 1
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJ = 0 (reset value) ICCADJ = 1	 66 66	 120 130	 130 150	mA	VCC from 3 to 5.5V

Table 20. Smart Card Class A

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	Ripple on CVCC		60 150	200 350	mV	0 < Icard < 60mA C_L =10µF for AT83C24 0 < Icard < 65mA C_L = 3.3µF for AT83C24NDS
	Spikes on CVCC	4.6		5.3	V	Max. charge 40 nA.s Max. duration 400 ns Max. Icard variation 200 mA
Vcardok up	Vcardok high level threshold	4.8	4.9		V	
Vcardok down	Vcardok low level threshold	4.6 4.75	4.8 4.8		V	AT83C24 AT83C24NDS
T_{VHL}	CVCC valid to 0		180 500	250 750	µs	Icard = 0, VCC > V_{PFDP} C_L = 3.3 µF Icard = 0 C_L = 10 µF Icard = 0 (see note 1)
T_{VLH}	CVCC 0 to Valid		180 110 240 170	250 250 300 250	µs	VCC = 3V, C_L = 3.3µF Icard = 65mA Icard = 0mA VCC = 3V, C_L = 10µF Icard = 65mA Icard = 0mA

Notes: 1. Capacitor: X7R type or X5R type, max ESR value is 30mΩ (100kHz-100MHz),
Replacing 3.3µF by 2.2µF in parrallel with 1µF is better for ESR and noise reduction.

Table 21. Smart Card Class B

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current Capability	65 65			mA	VCC=3V to 5.5V, STEPREG=0 VCC > 5.35V, STEPREG = 1
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJ = 0 (reset value) ICCADJ = 1	 66 66	 130 140	 140 150	mA	VCC from 3.0 to 5.5V
	Ripple on CVCC		60	200 350	mV	0 < Icard < 65mA C_L =10µF 0 < Icard < 65mA C_L = 3.3µF
	Spikes on CVCC	2.76		3.24	V	Maxi. charge 40 nA.s Max. duration 400 ns Max. variation Icard 200mA
Vcardok up	Vcardok high level threshold	2.8	3		V	
Vcardok down	Vcardok low level threshold	2.76	2.9		V	
T_{VHL}	CVCC valid to 0		130 400	250 500	µs	Icard = 0, VCC > V_{PFDP} C_L = 3.3 µF Icard = 0 (see note 1) C_L = 10 µF Icard = 0

Table 21. Smart Card Class B

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{VLH}	CVCC 0 to Valid		140 110 130 100	250 250 250 250	µs	VCC = 3V, C_L = 3.3µF Icard = 65mA Icard = 0mA VCC = 3V, C_L = 10µF Icard = 60mA Icard = 0mA

Notes: 1. Capacitor: X7R type or X5R type, max ESR value is 30mΩ (100kHz-100MHz),
Replacing 3.3µF by 2.2µF in parrallel with 1µF is better for ESR and noise reduction.

Table 22. Smart Card Class C

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current Capability	40			mA	VCC = 3V
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJ = 0 (reset value) ICCADJ = 1		45		mA	
	Spikes on CVCC	1.68		1.92	V	
Vcardok up	Vcardok high level threshold	1.75	1.8		V	
Vcardok down	Vcardok low level threshold	1.7	1.75		V	
T_{VHL}	CVCC valid to 0		180	300	µs	Icard = 0, C_L = 10 µF(1) CVCC = 1.8V to 0.4V
T_{VLH}	CVCC 0 to valid		200 100 50 60	300 150 80 100	µs	Icard = 40mA, C_L = 10 µF(1) Icard = 0, C_L = 10 µF(1) Icard = 40mA, C_L = 3.3 µF(1) Icard = 0, C_L = 3.3 µF(1) CVCC = 0.4 to VCARDOK

Notes: 1. Capacitor: X7R type or X5R type, max ESR value is 30mΩ (100kHz-100MHz),
Replacing 3.3µF by 2.2µF in parrallel with 1µF is better for ESR and noise reduction.

Table 23. Smart Card Clock (CCLK pin)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low-voltage	0		0.4	V	I_{OL} = -200 µA CLASS A&B&C
V_{OH}	Output High Voltage	CVCC - 0.45 0.7CVCC		CVCC CVCC	V	I_{OH} = +200 µA CLASS A&B CLASS C
I_{OS}	Short Circuit Current	-30		30	mA	Short to GND or CVCC
t_R t_F	Rise and Fall time			16 22.5 50	ns	C_L = 30 pF CLASS A C_L = 30 pF CLASS B C_L = 30 pF CLASS C measurement between 10% and 90% of CVCC

Table 23. Smart Card Clock (CCLK pin) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	Rise and Fall Slew rate	0.2 0.12			V/ns	CLASS A CCLK from 0.5 to 4.2V CLASS B CCLK from 0.5 to 0.85 x CVCC
	Low level voltage stability (taking into account PCB design)	-0.25		0.5	V	CLASS A&B&C
	High level voltage stability (taking into account PCB design)	4.2 2.35 CVCC-0.4		CVCC+0.25 CVCC+0.25 CVCC+0.25	V	CVCC = CLASS A CVCC = CLASS B CLASS C
CCLK	Smart card clock frequency			24	MHz	C_L = 30pF, CLK=48MHz

Table 24. Smart Card I/O (CIO, CC4, CC8 pins)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low-voltage	-0.3V		0.8	V	I_{IL} = 500 µA
I_{IL}	Input Low Current			700	µA	CVCC = CLASS A&B&C
V_{IH}	Input High Voltage	0.6 x CVCC 0.7 x CVCC		CVCC CVCC	V	CVCC = CLASS A CVCC = CLASS B & C
I_{IH}	Input High Current	-20		+20	µA	
V_{OL}	Output Low-voltage	0		0.45 0.3 0.3	V	I_{OL} = -1 mA CLASS A I_{OL} = -1 mA CLASS B I_{OL} = -1 mA CLASS C
V_{OH}	Output High Voltage	0.75 x CVCC 0.9 x CVCC		CVCC CVCC	V	I_{OH} = 40 µA CLASS A&B&C I_{OH} = 0µA, CLASS A&B
I_{OS}	Output Short Circuit Current	-15		+15	mA	Short to GND or CVCC
	Low level voltage stability (taking into account PCB design)	-0.25 -0.25 -0.25		0.6 0.4 0.4	V	CLASS A CLASS B CLASS C
	High level voltage stability (taking into account PCB design)	CVCC-0.5		CVCC+0.25	V	CVCC = CLASS A&B&C
t_R t_F	Output rise and fall time			0.1	µs	C_L = 65 pF CLASS A: measurement between 0.6V and 70% of CVCC CLASS B & C: measurement between 0.4V and 70% of CVCC
t_R t_F	Input rise and fall time			1	µs	C_L = 65 pF

Table 25. Smart Card RST (CRST pin)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low-voltage	0 0		0.12 x CVCC 0.4 0.2	V	I_{OL} = -20 µA CLASS A&B&C I_{OL} = -200 µA CLASS A I_{OL} = -200 µA CLASS B&C
V_{OH}	Output High Voltage	0.9*CVCC		CVCC	V	I_{OH} = 200 µA CLASS A&B&C
I_{OS}	Output High Current	-15		+15	mA	Short to GND or CVCC
t_R t_F	Rise and Fall time			0.1	µs	C_L = 30pF measurement between 10% and 90% of CVCC
	Low level voltage stability (taking into account PCB design)	-0.25		0.50V 0.30V 0.30V	V	CLASS A CLASS B CLASS C
	High level voltage stability (taking into account PCB design)	4.2 2.35 CVCC-0.4		CVCC+0.25	V	CLASS A CLASS B CLASS C

Table 26. Card Presence

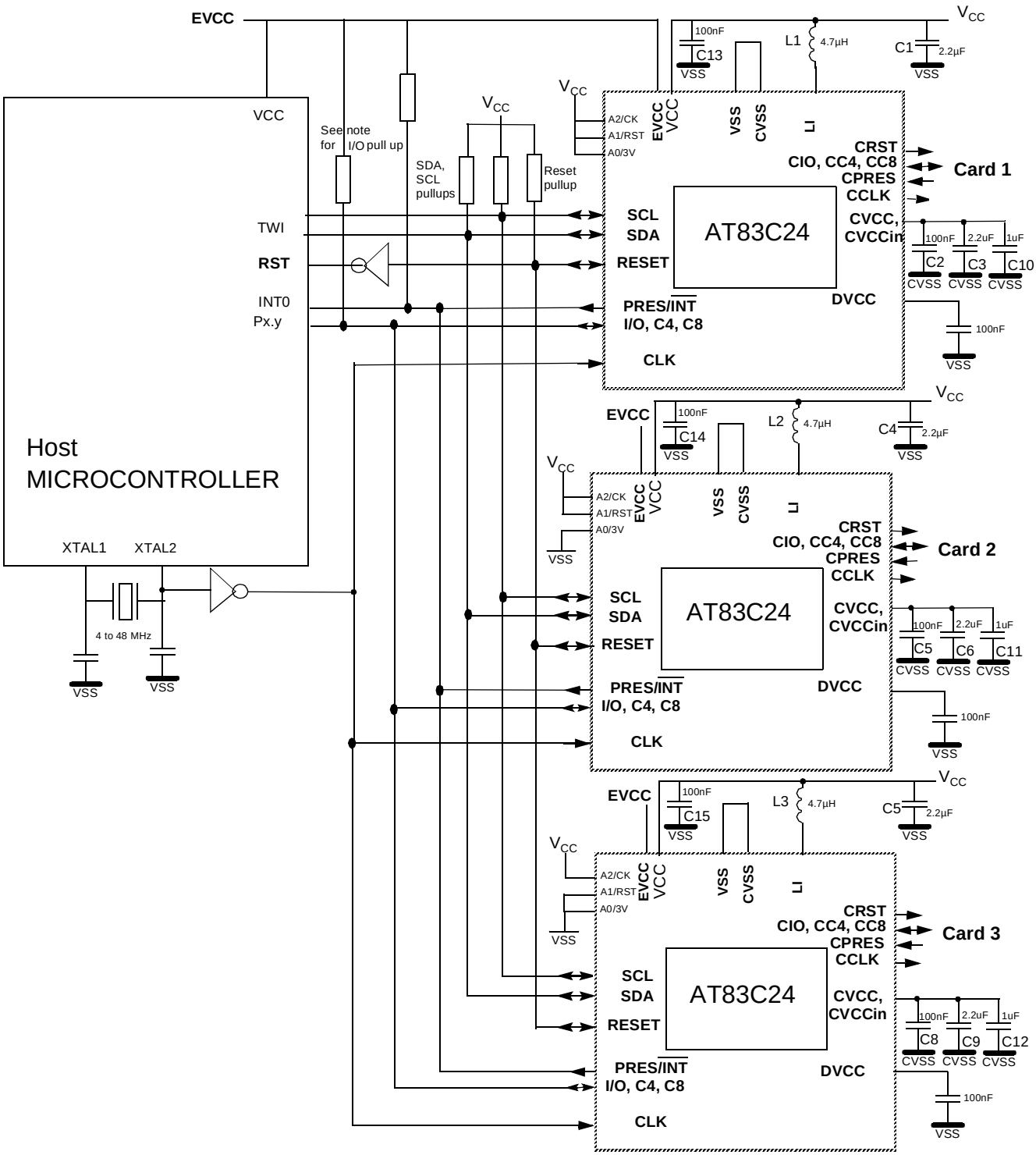
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{CPRES}	CPRES weak pull-up output current	300	330	360	κΩ	Short to VSS PULLUP = 1: Internal pull-up active

Table 27. TWI (SDA, SCL pins)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{SU;DAT}$	Data set-up time	20	10		ns	Not tested
$t_{HD;DAT}$	Data hold time	10	0		ns	Not tested
t_{fDA}	Fall time on SDA signal			50	ns	Not tested

Typical Application

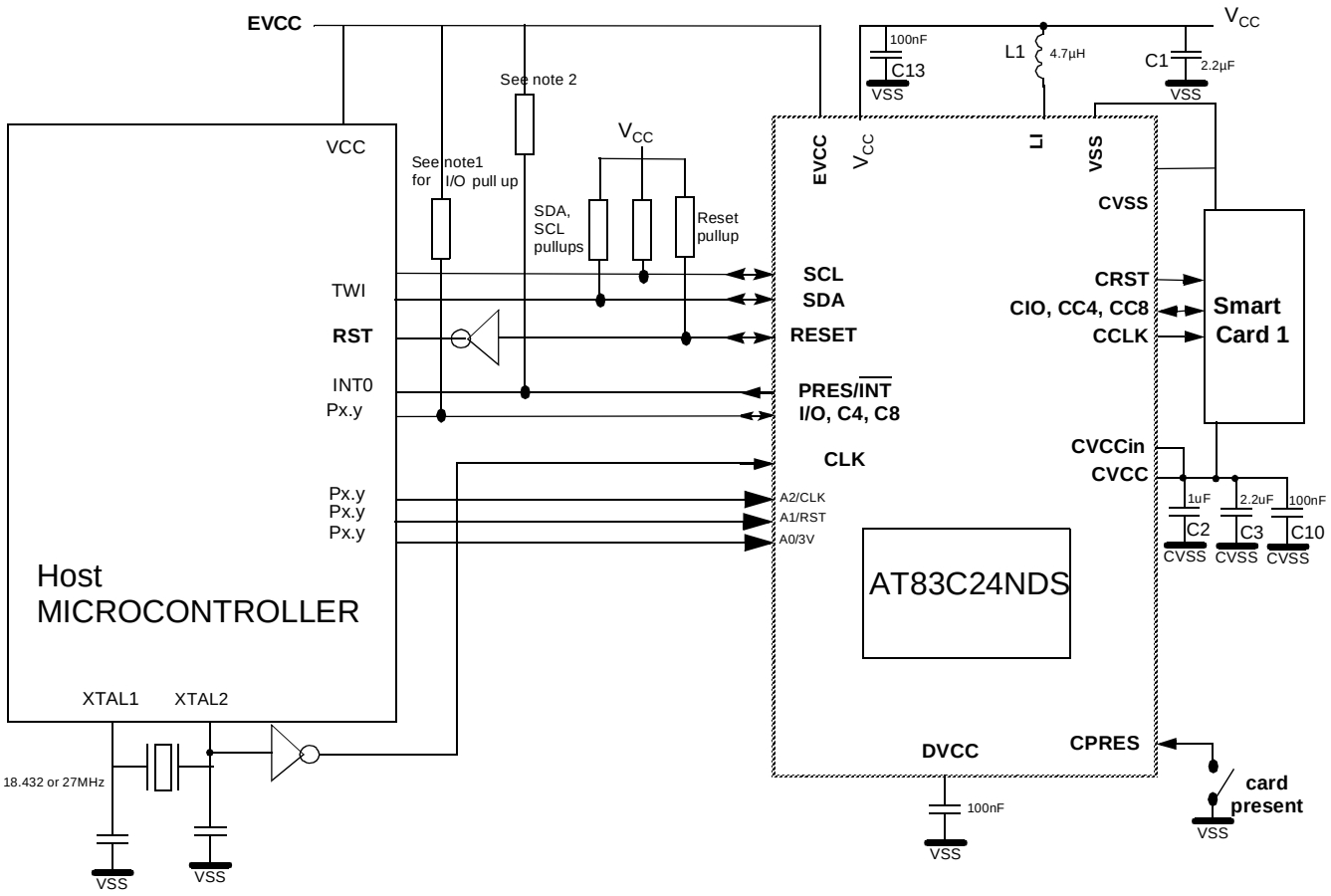
Figure 1. Typical Standard Mode Application Diagram for 3 AT83C24 (up to 8 AT83C24 if needed)



Note: 1. The external resistor on I/O can be removed if the host pin has an internal resistor.

Typical NDS Application

Figure 2. Typical NDS Standard Mode Application Diagram for 1 AT83C24NDS.



Note:
1. The external resistor on I/O can be removed if the host pin has an internal resistor.
2. The internal pull up on PRES/INT is disabled during reset (recommended external 20kOhms pull up).
3. Refer to application note for AT83C24NDS software configuration.

Ordering Information

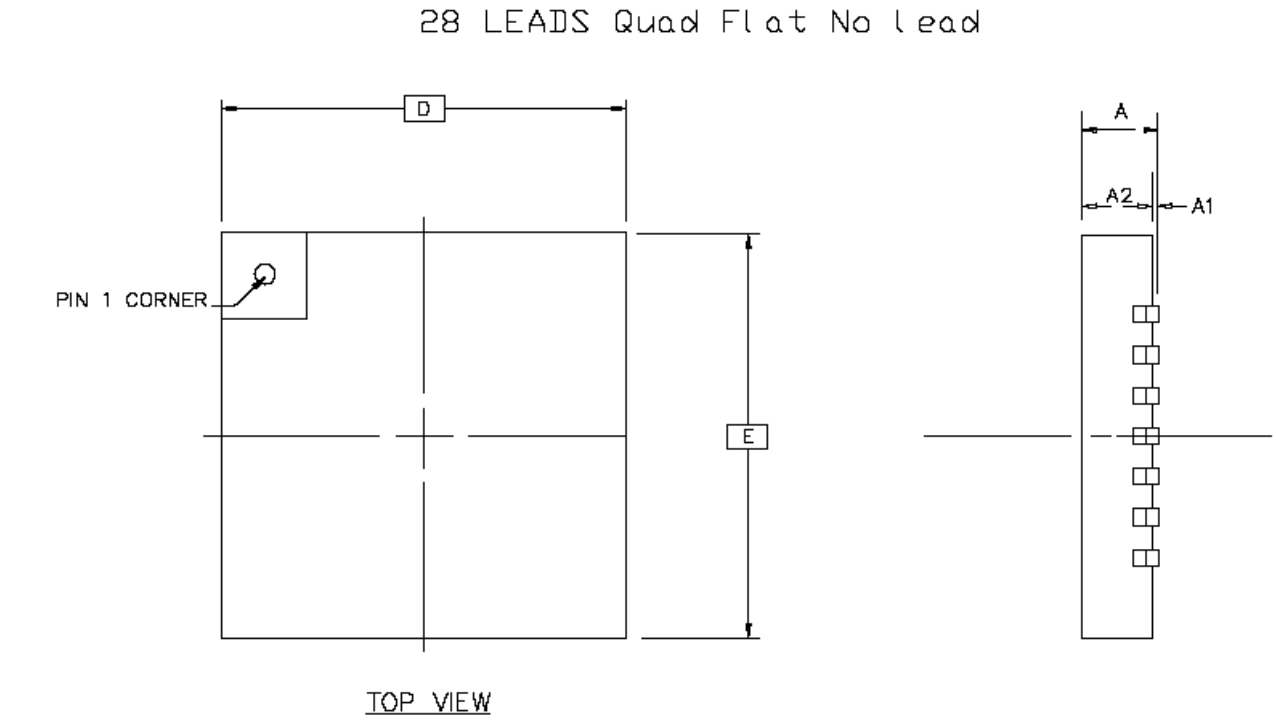
Part Number	Supply Voltage	Temperature Range	Package	Packing
AT83C24-PRTIL[2]	3V to 5.5V	Industrial	QFN28	Tray
AT83C24-PRRIL[2]	3V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24-PRTIM[2]	4.00V to 5.5V	Industrial	QFN28	Tray
AT83C24-PRRIM[2]	4.00V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24-TISIL	3V to 5.5V	Industrial	SO28	Stick
AT83C24-TIRIL	3V to 5.5V	Industrial	SO28	Tape&Reel
AT83C24-TISIM	4.00V to 5.5V	Industrial	SO28	Stick
AT83C24-TIRIM	4.00V to 5.5V	Industrial	SO28	Tape&Reel
AT83C24NDS-PRTIL [1][2]	3V to 5.5V	Industrial	QFN28	Tray
AT83C24NDS-PRRIL [1][2]	3V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24NDS-PRTIM [1][2]	4.00V to 5.5V	Industrial	QFN28	Tray
AT83C24NDS-PRRIM [1][2]	4.00V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24NDS-TISIL [1]	3V to 5.5V	Industrial	SO28	Stick
AT83C24NDS-TIRIL [1]	3V to 5.5V	Industrial	SO28	Tape&Reel
AT83C24NDS-TISIM [1]	4.00V to 5.5V	Industrial	SO28	Stick
AT83C24NDS-TIRIM [1]	4.00V to 5.5V	Industrial	SO28	Tape&Reel
LEAD FREE/ HALOGEN FREE:				
AT83C24-PRTUL[2]	3V to 5.5V	Industrial	QFN28	Tray
AT83C24-PRRUL[2]	3V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24-PRTUM[2]	4.00V to 5.5V	Industrial	QFN28	Tray
AT83C24-PRRUM[2]	4.00V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24-TISUL	3V to 5.5V	Industrial	SO28	Stick
AT83C24-TIRUL	3V to 5.5V	Industrial	SO28	Tape&Reel
AT83C24-TISUM	4.00V to 5.5V	Industrial	SO28	Stick
AT83C24-TIRUM	4.00V to 5.5V	Industrial	SO28	Tape&Reel
AT83C24NDS-PRTUL [1][2]	3V to 5.5V	Industrial	QFN28	Tray
AT83C24NDS-PRRUL [1][2]	3V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24NDS-PRTUM[1][2]	4.00V to 5.5V	Industrial	QFN28	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
AT83C24NDS-PRRUM (1)(2)	4.00V to 5.5V	Industrial	QFN28	Tape&Reel
AT83C24NDS-TISUL (1)	3V to 5.5V	Industrial	SO28	Stick
AT83C24NDS-TIRUL (1)	3V to 5.5V	Industrial	SO28	Tape&Reel
AT83C24NDS-TISUM (1)	4.00V to 5.5V	Industrial	SO28	Stick
AT83C24NDS-TIRUM (1)	4.00V to 5.5V	Industrial	SO28	Tape&Reel

Note: 1. Enhanced AC/DC parameters, see first page for differences between AT83C24 and AT83C24NDS.
2. Refer to index mark for proper placement.

Package Drawings

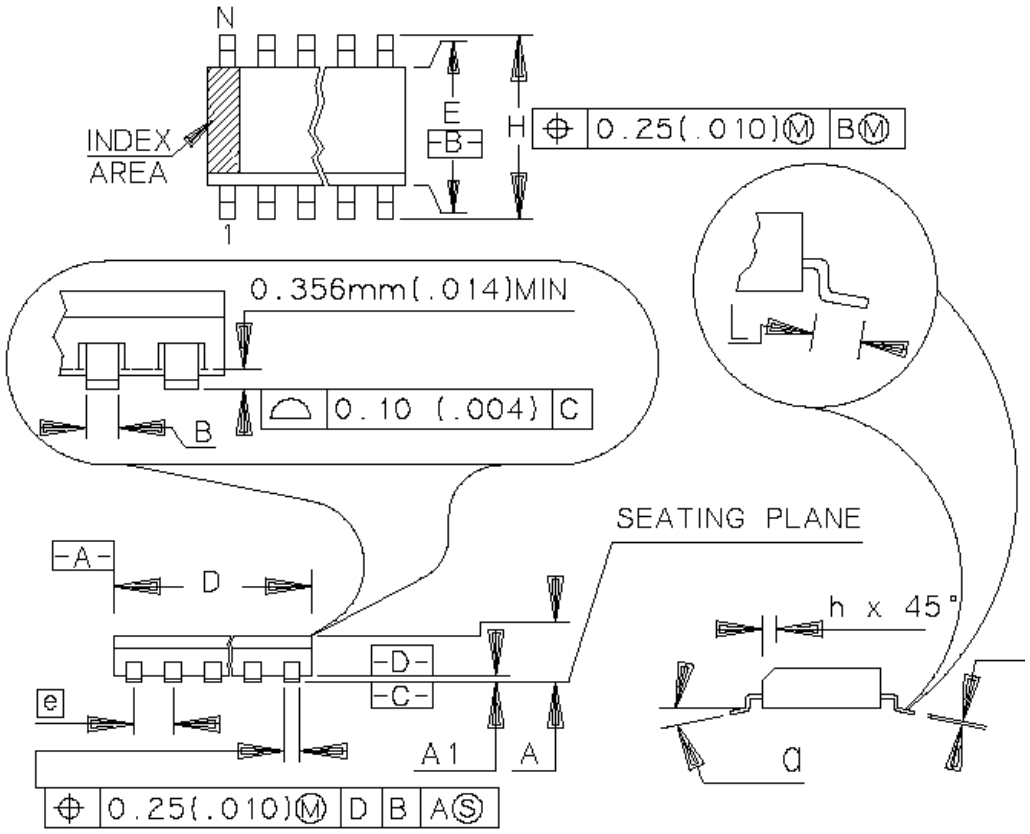
QFN28



	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80		1.00	.031		.039
J/K	3.47	3.57	3.67	.137	.140	.144
D/E		5.00 BSC			.197 BSC	
A1	0.00		0.05	.000		.002
N		28				
A2	0.75		1.00	.029		.039
e		0.50 BSC			.020 BSC	
L	0.35	0.40	0.45	.014	.016	.018
L1	-	-	0.15	-	-	.006
b	0.18	0.25	0.30	.007	.010	.012

SO28

28 PINS SO . 300



	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	17.70	18.10	.697	.713
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	28		28	
α	0°		8°	

Datasheet Change Log

Changes from 4234A-05/03 to 4234B-02/04

1. Addition of CRST, CIO, CCLK controllers descriptions, page 10.
2. Update of Hardware\Software activation description, page 14.
3. Suppression of low voltage regulator mode for power down modes, page 19.
4. Modification of clock values in CONFIG2 regsiter, page 22.
5. Addition of a point on QFN pinout view, page2.
6. Update of electrical characteristics, page 29.

Changes from 4234B-02/04 to 4234C - 04/04

1. Addition of references in ordering information
2. Update of EVCC description
3. Update of CARDDET bit and INSERT bit description

Changes from 4234C-04/04 to 4234D - 07/04

1. Update for Rev 4 silicon version (index 4 on component).
2. Software workaround for A2 or A2/2 selection in CKS register.
3. Max speed on IO/CIO transfer
4. New conditions for hardware activation (see IT_SEL).
5. SO28 drawing package (error with SO32).
6. Adjusted electrical parameters for NDS compliance, pages 28, 29, 30.

Changes from 4234D-04/04 to 4234E - 09/04

1. QFN28 new package drawing.
2. Clock input parameters for AT83C24 and AT83C24NDS.

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