Am29118

Eight-Bit Am29116 I/O Support

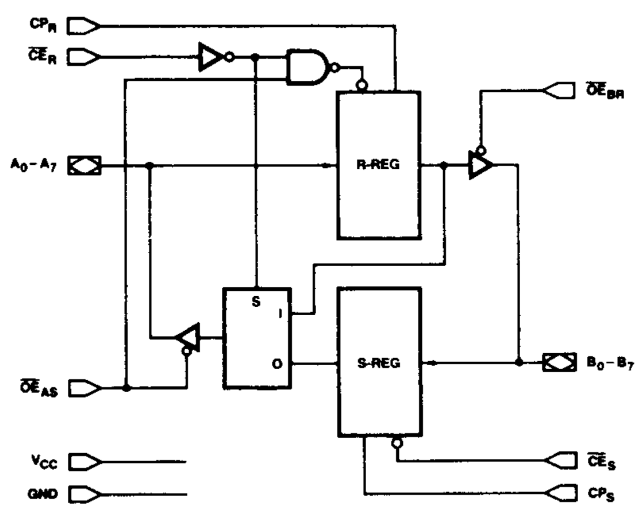
DISTINCTIVE CHARACTERISTICS

- Eight-bit bidirectional I/O port
- Reads both registers on A-port
- Separate clock, clock enable and three-state output enable to synchronize data between two bidirectional buses
- 24 mA output current sink capability
- 24-pin 0.3-inch slim package
- Additional accumulator to support certain Am29116 applications.

GENERAL DESCRIPTION

The Am29118 is an eight-bit wide bidirectional parallel data input/output port designed to provide an additional accumulator when used with the Am29116 or with any microprocessor with single bidirectional data port. In addition, it can be used as a parallel data input/output port, like the Am2952.

BLOCK DIAGRAM



BD002182

Figure 1

RELATED AMD PRODUCTS

Part No.	Description
Am29116 Family	High Performance 16-Bit Bipolar Microprocessor Family
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2925	System Clock Generator and Driver
Am2940/2	DMA Address Generator
Am2950-3	8-Bit Bidirectional I/O Ports
Am29800 Family	High Performance Bus Interface

S-3 Orig

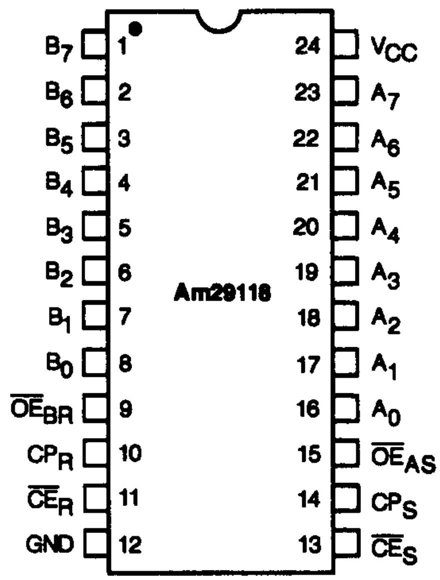
002136

Publication # 05182 Rev. C Amendment /0
Issue Date: November 1986

T-2136

CONNECTION DIAGRAM
Top View

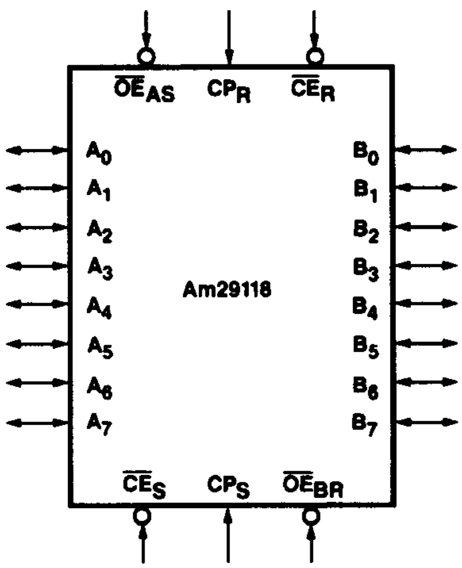
SLIM (CD3024)



CD010210

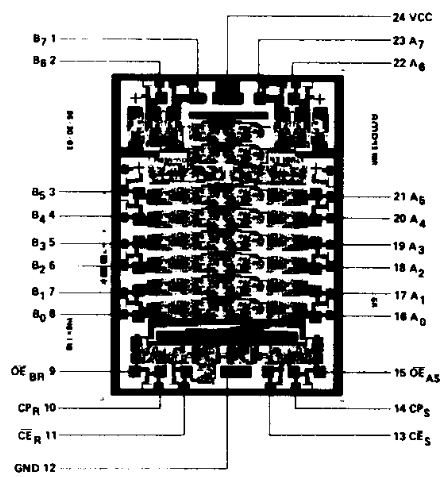
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS000932

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.148" x 0.110"
Approximate Gate Count = 109

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM29118 — D C B

E. OPTIONAL PROCESSING
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD3024)

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29118
8-Bit Am29116 I/O Support

Valid Combinations	
AM29118	DC, DCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_7$ Register I/O Ports (Input/Output)
Eight bidirectional lines carrying the R Register inputs or outputs or S Register outputs.

$B_0 - B_7$ Register I/O Ports (Input/Output)
Eight bidirectional lines carrying the S Register inputs or R Register outputs.

CP_R Clock Pulse, R-Register (Input)
The clock for the R Register. When $\overline{CE}_R$ is LOW and $\overline{OE}_{AS}$ is HIGH, data is entered into the R Register on the LOW-to-HIGH transition of the CP_R signal.

$\overline{CE}_R$ Register Enable, R Register (Input, Active LOW)
The Clock Enable for the R Register, when $\overline{CE}_R$ is LOW and $\overline{OE}_{AS}$ is HIGH, data is entered into the R Register on the LOW-to-HIGH transition of the CP_R signal. When $\overline{CE}_R$ is HIGH, the R Register holds its contents, regardless of CP_R signal transitions.

$\overline{OE}_{BR}$ Output Enable, B Port (Input, Active LOW)
The Output Enable for the R Register. When $\overline{OE}_{BR}$ is LOW, the R Register three-state outputs are enabled onto the $B_0 - B_7$ lines. When $\overline{OE}_{BR}$ is HIGH, the R Register outputs are in the high-impedance state.

CP_S Clock Pulse, S Register (Input)
The clock for the S Register. When $\overline{CE}_S$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CP_S signal.

$\overline{CE}_S$ Register Enable, S Register (Input, Active LOW)
The clock enable for the S Register. When $\overline{CE}_S$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CP_S signal. When $\overline{CE}_S$ is HIGH, the S Register holds its contents, regardless of CP_S signal transitions.

$\overline{OE}_{AS}$ Output Enable, A Port (Input, Active LOW)
The output enable for the S Register. When $\overline{OE}_{AS}$ is LOW, the R or S Register three-state outputs are enabled onto the $A_0 - A_7$ lines. When $\overline{OE}_{AS}$ is high, the S Register outputs are in the high-impedance state.

FUNCTIONAL DESCRIPTION

The Am29118 has two eight-bit wide registers (R-Register and S-Register) connected back to back for moving data in both directions between two buses. The R-Register serves the dual purpose of transmitting data from one bus (device's internal bus) to another (system bus), and serving as an additional accumulator for the Am29116.

The accumulator function is implemented by allowing the A-port to provide read and write data from the R-Register and read data from the S-Register; the B-port provides read data for the R-Register and write data for the S-Register (similar to the Am2952). This additional function in the Am29118 is implemented with a two-input multiplexer, as shown in Figure 1. Each register has an individual clock (CP_R and CP_S), a Clock Enable, ($\overline{CE}_R$ and $\overline{CE}_S$), and a three-state Output Enable ($\overline{OE}_{AS}$ and $\overline{OE}_{BR}$). The clock enable signal for the R-Register ($\overline{CE}_R$) and the Output Enable Signal for the S-Register ($\overline{OE}_{AS}$) are encoded to make the R-Register an accumulator, in addition to all the Am2952 functions as shown in Table 1. Because of this encoding, transferring data from the S-Register to the R-Register is not permissible.

TABLE 1.

$\overline{OE}_{AS}$	$\overline{CE}_R$	Function
L	L	Read R, Disable CP_R
L	H	Read S, Disable CP_R
H	L	Enable CP_R
H	H	Disable CP_R

APPLICATIONS

In the Am29116 system, there is only one I/O port available for data communication with the ALU. In such a system, the Am29118 acts as an additional accumulator (temporary storage) to increase performance, and also provides capability of a bidirectional I/O port (like the Am2952).

Figure 2 shows the connections necessary for the Am29118 to be used as an accumulator as well as a bidirectional I/O port. The A-port is connected to the Y-bus (internal bus) of the Am29116, and B-port is connected to the system data bus. Four microcode bits are used for source and destination control for the Y-bus and the system data bus. Figure 3 shows the timing waveforms to modify an accumulator (R-Register) in two microcycles. During the first cycle, data is read from the R-Register, modified in the Am29116 and stored in one of the internal registers. A two-address architecture is required if the second operand to modify the R-Register is in one of the RAM registers, and the result has to be stored in another RAM register. For stable operation, data from the R-Register is latched in the D-Latch halfway through the clock during the first cycle. The instruction is executed and the result stored into a scratchpad register. In the second cycle, data is moved from the internal result register to the R-Register of the Am29118.

Figure 4 shows the timing waveforms to modify an accumulator (R-Register) in a single microcycle. In the first half of the cycle the source register is enabled on the Y-bus into the D-Latch of the Am29116. The D-Latch is transparent during the first half of the cycle. In the second half of the cycle, data is latched in the D-Latch and the bus source is disabled. During the second half of the cycle, the output buffer of the Am29116 is enabled to bring the result on the Y-bus to be loaded into the destination. These two techniques provide different advantages and disadvantages to modify the external accumulator using the Am29116. The first technique (Figure 3) takes two microcycles but allows a shorter microcycle time. The second technique (Figure 4) takes only one microcycle but needs a longer microcycle time.

There is also a requirement for the system bus to transfer data as input to the Am29116. The S-Register is used in this case to receive data from the system bus (like the Am2952).

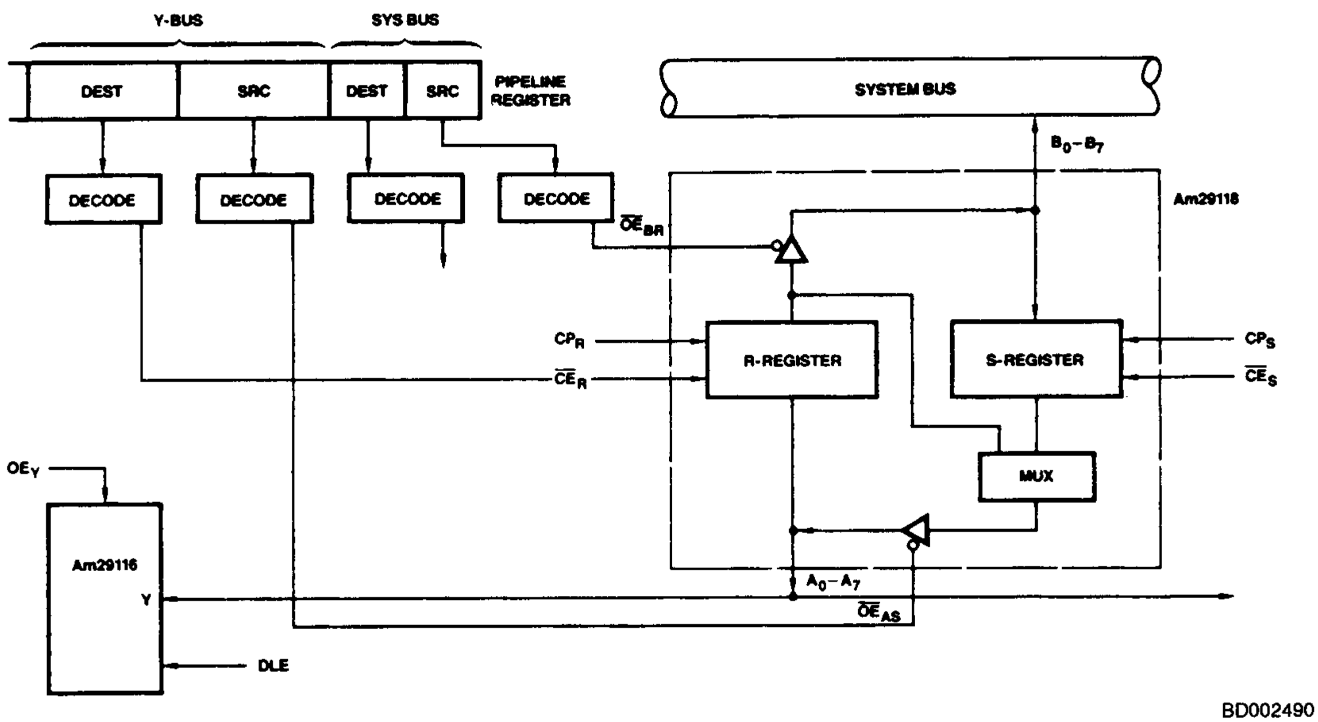


Figure 2. System Configuration.

SWITCHING WAVEFORMS

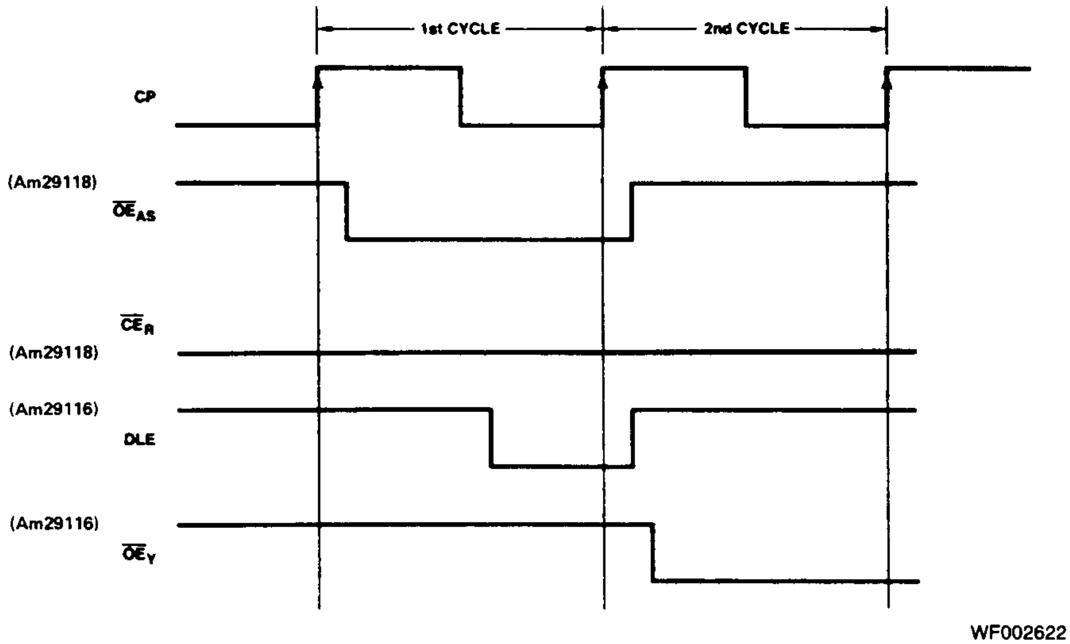


Figure 3. Timing Waveforms for Modifying R-Register in Two Microcycles using the Am29116.

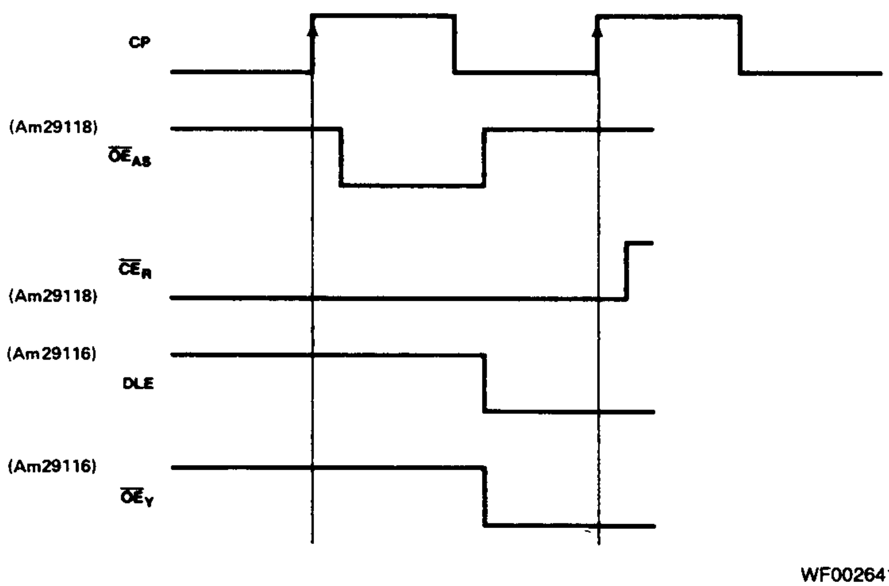


Figure 4. Timing Waveforms for Modifying R-Register using the Am29116.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
(Ambient) Temperature under Bias........ −55°C to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs For
High Output State .... −0.5 V to $+V_{CC}$ max
DC Input Voltage .... −0.5 V to +5.5 V
DC Output Current, into Outputs .... 30 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature .... 0°C to +70°C
Supply Voltage .... +4.75 V to +5.25 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	A_0-A_7, B_0-B_7	COM'L, I_{OL} = −6.5 mA	2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	A_0-A_7, B_0-B_7	COM'L, I_{OL} = 24 mA		0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA				−115	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5 V		A_0-A_7, B_0-B_7		−250	μA
				$\overline{CE}_R$		−720	μA
				Others		−360	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN}=2.7 V		A_0-A_7, B_0-B_7		70	μA
				Others		20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN}=5.5 V				1.0	mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_0-A_7, B_0-B_7	V_O = 2.4 V		70	μA
				V_O = 0.4 V		−250	
I_{SC}	Output Short Circuit Current (Note 2)	V_{CC} = MAX			−30	−85	mA
I_{CC}	Power Supply Current (Notes 3, 4)	V_{CC} = MAX	COM'L	T_A = 0 to +70°C		190	mA
				T_A = +70°C		180	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. I_{CC} is measured with all inputs at 4.5 V and all outputs open.
4. Worst case I_{CC} is at minimum temperature.

SWITCHING CHARACTERISTICS

The tables below define the Am29118 switching characteristics. Table A is setup and hold times relative to a clock LOW-to-HIGH transition. Table B is propagational delays. Table C is pulse-width requirements. Table D is enable/disable times. All measurements are made at 1.5 V with input levels at 0 or 3 V. All values are in ns with R_L on A_i and B_i = 220Ω and R_L on FS and FR = 300Ω. C_L = 50 pF except output disable times which are specified at C_L = 5 pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, C_L = 50 pF)

A. Setup and Hold Times

Input	With Respect to	t_s	t_h
$A_0 - A_7$	CP_R ↑	11	3
$B_0 - B_7$	CP_S ↑	11	3
$\overline{CE}_S$	CP_S ↑	9	2
$\overline{CE}_R$	CP_R ↑	9	2

B. Propagation Delays

Input	$A_0 - A_7$	$B_0 - B_7$
CP_S ↑	20	–
CP_R ↑	–	20

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CP_S	20	20
CP_R	20	20

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}_{AS}$	$A_0 - A_7$	20	20
$\overline{OE}_{BR}$	$B_0 - B_7$	20	20

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic testing environment. The specifics of what philosophies are applied to which test are shown in the data sheet and the data-sheet reconciliation that follow.

Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" that measure the propagation delays in to and out of the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impractical to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench setup and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data-sheet loads, may be used during production testing.

Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of bipolar devices frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels.

AC Testing

AC parameters are specified that cannot be measured accurately on automatic testers because of tester limitations. Data-input hold times fall into this category. In these cases, the parameter in question is tested by correlating the tester to bench data or oscilloscope measurements made on the tester by engineering (supporting data on file).

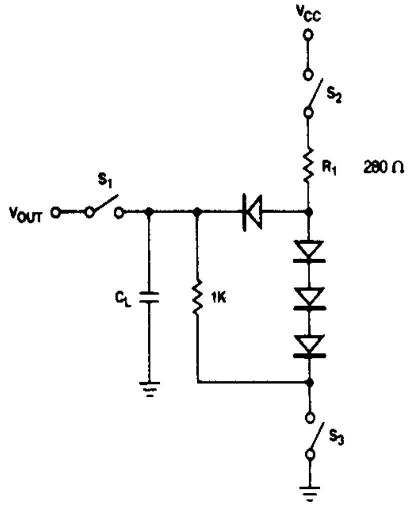
Certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

Output Short-Circuit Current Testing

When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the V_{OUT} = 0, V_{CC} = Max. case.

SWITCHING TEST CIRCUIT

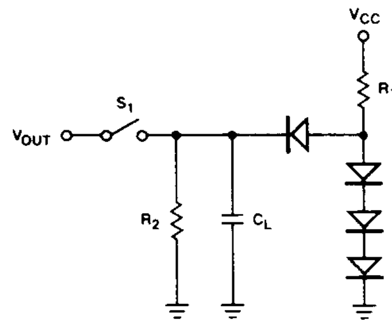
A. THREE-STATE OUTPUTS



TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}}$$

B. NORMAL OUTPUTS



TC001081

$$R_2 = \frac{2.4\ V}{I_{OH}}$$

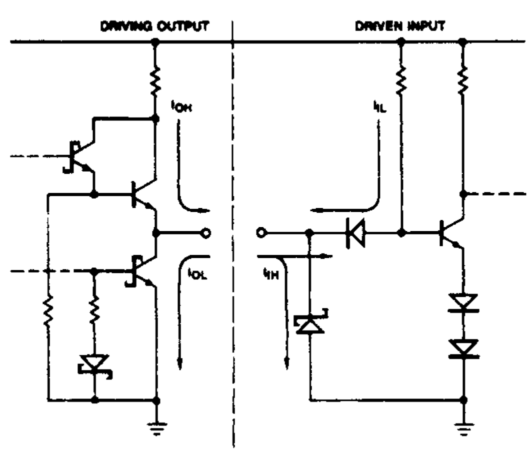
$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}}$$

Notes: 1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

TEST OUTPUT LOADS FOR Am29118

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
16–23	$A_0 - A_7$	A	220	1K
1–8	$B_0 - B_7$	A	220	1K

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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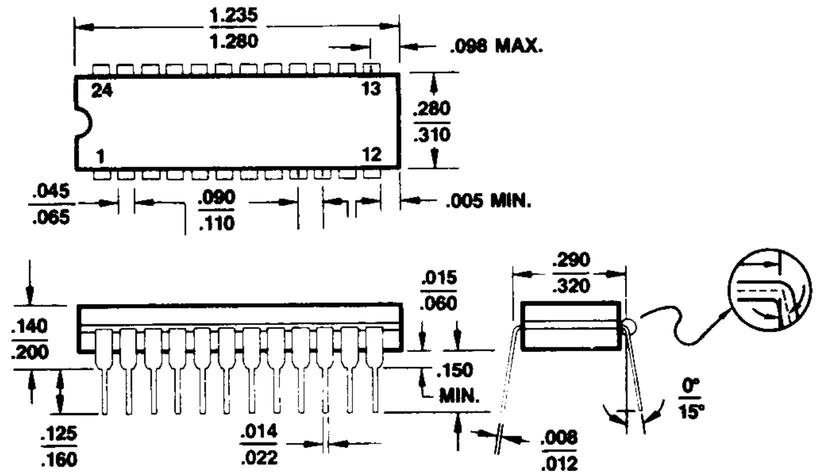
PHYSICAL DIMENSIONS

CD3024



PID # 06850B

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Printed in U.S.A. AIS-RRD-15M-11/86-0