

HN58V65A Series

HN58V66A Series

64 k EEPROM (8-kword × 8-bit)

Ready/Busy Function, $\overline{\text{RES}}$ Function (HN58V66A)

REJ03C0149-0300Z
(Previous ADE-203-539B (Z) Rev. 2.0)
Rev. 3.00
Dec. 04. 2003

Description

Renesas Technology's HN58V65A series and HN58V66A series are a electrically erasable and programmable EEPROM's organized as 8192-word × 8-bit. They have realized high speed, low power consumption and high relisbility by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single supply: 2.7 to 5.5 V
- Access time:
 - 100 ns (max) at $2.7 \text{ V} \leq V_{\text{cc}} < 4.5 \text{ V}$
 - 70 ns (max) at $4.5 \text{ V} \leq V_{\text{cc}} \leq 5.5 \text{ V}$
- Power dissipation:
 - Active: 20 mW/MHz (typ)
 - Standby: 110 μW (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 10 ms (max)
- Automatic page write (64 bytes): 10 ms (max)
- Ready/ $\overline{\text{Busy}}$
- $\overline{\text{Data}}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology

HN58V65A Series, HN58V66A Series

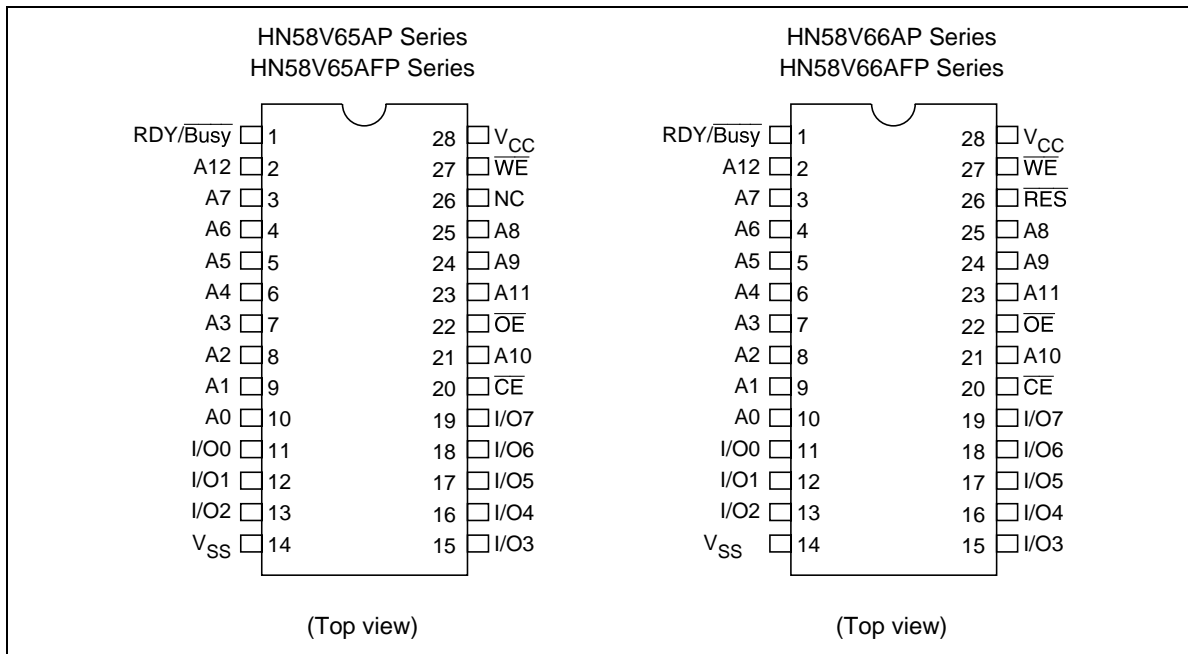
Features (cont)

- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin (only the HN58V66A series)
- Industrial versions (Temperature range: -20 to 85°C and -40 to 85°C) are also available.
- There are also lead free products.

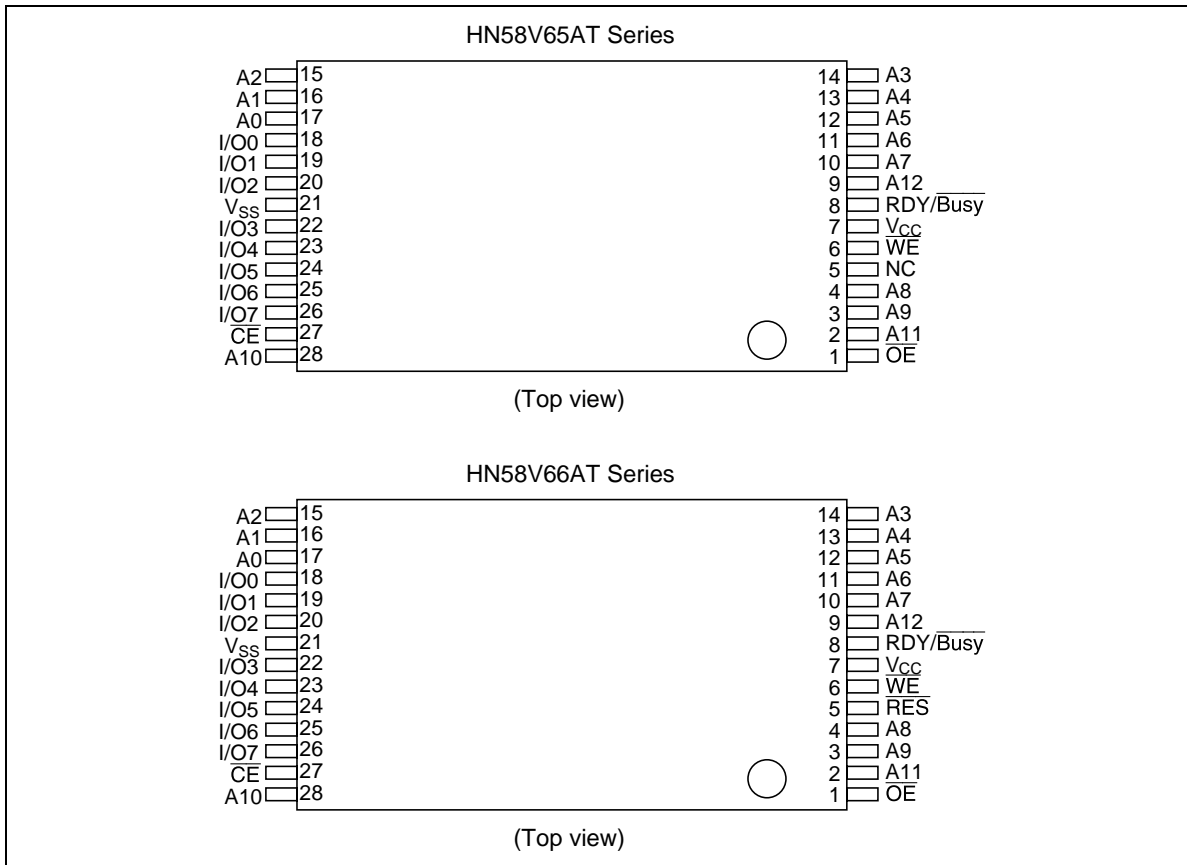
Ordering Information

Type No.	Access time		Package
	$2.7\text{ V} \leq V_{\text{CC}} < 4.5\text{ V}$	$4.5\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$	
HN58V65AP-10	100 ns	70 ns	600 mil 28-pin plastic DIP (DP-28)
HN58V66AP-10	100 ns	70 ns	
HN58V65AFP-10	100 ns	70 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58V66AFP-10	100 ns	70 ns	
HN58V65AT-10	100 ns	70 ns	28-pin plastic TSOP(TFP-28DB)
HN58V66AT-10	100 ns	70 ns	
HN58V65AP-10E	100 ns	70 ns	600 mil 28-pin plastic DIP (DP-28V)
HN58V66AP-10E	100 ns	70 ns	Lead free
HN58V65AFP-10E	100 ns	70 ns	400 mil 28-pin plastic SOP (FP-28DV)
HN58V66AFP-10E	100 ns	70 ns	Lead free
HN58V65AT-10E	100 ns	70 ns	28-pin plastic TSOP(TFP-28DBV)
HN58V66AT-10E	100 ns	70 ns	Lead free

Pin Arrangement



Pin Arrangement (cont)



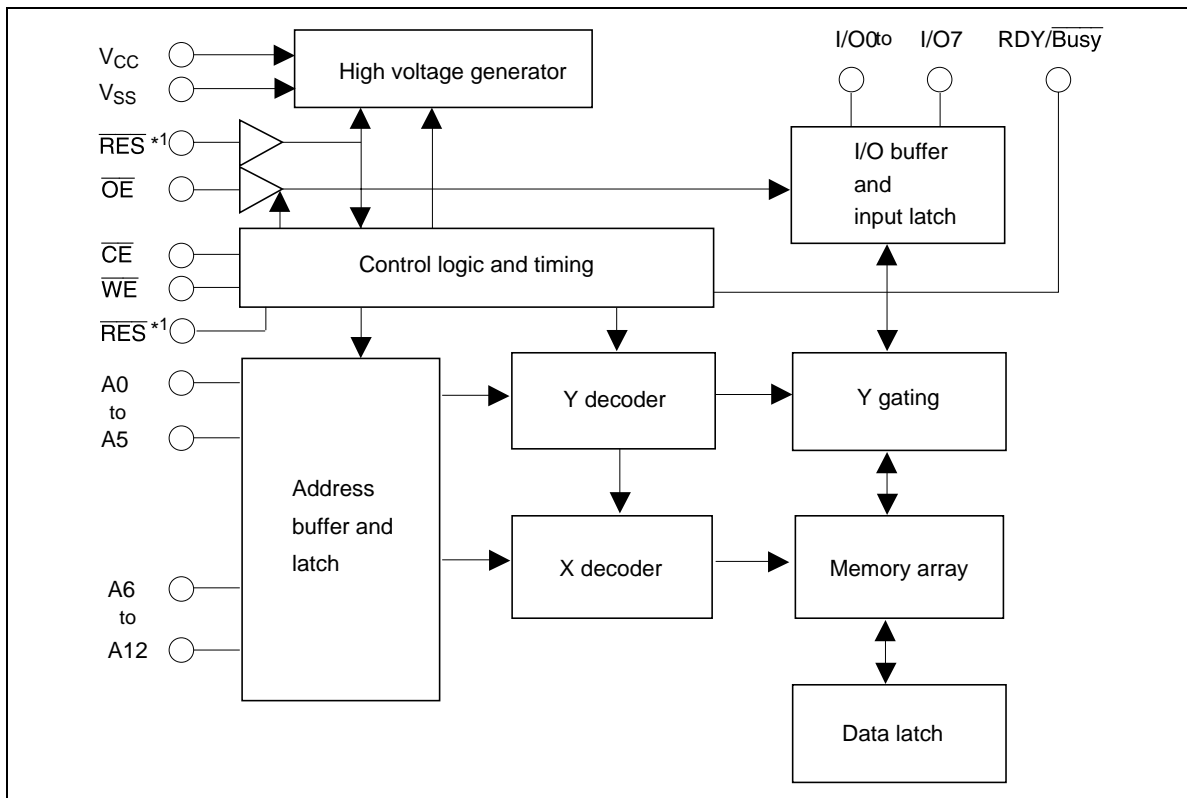
Pin Description

Pin name	Function
A0 to A12	Address input
I/O0 to I/O7	Data input/output
\overline{OE}	Output enable
\overline{CE}	Chip enable
\overline{WE}	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/Busy	Ready busy
\overline{RES}^{*1}	Reset
NC	No connection

Note: 1. This function is supported by only the HN58V66A series.

Block Diagram

Note: 1. This function is supported by only the HN58V66A series.



Operation Table

Operation	\overline{CE}	\overline{OE}	\overline{WE}	\overline{RES}^{*3}	RDY/Busy	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H^{*1}	High-Z	Dout
Standby	V_{IH}	\times^{*2}	\times	\times	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	\times	\times	V_{IH}	\times	—	—
	\times	V_{IL}	\times	\times	—	—
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Dout (I/O7)
Program reset	\times	\times	\times	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.
 2. \times : Don't care
 3. This function supported by only the HN58V66A series.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.6 to +7.0	V
Input voltage relative to V_{SS}	V_{in}	-0.5 ^{*1} to +7.0 ^{*3}	V
Operating temperature range ^{*2}	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Notes: 1. V_{in} min : -3.0 V for pulse width \leq 50 ns.
 2. Including electrical characteristics and data retention.
 3. Should not exceed $V_{CC} + 1$ V.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	—	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	-0.3 ^{*1}	—	0.6 ^{*5}	V
	V_{IH}	1.9 ^{*2}	—	$V_{CC} + 0.3^{*3}$	V
	V_H^{*4}	$V_{CC} - 0.5$	—	$V_{CC} + 1.0$	V
Operating temperature	T_{opr}	0	—	+70	°C

Notes: 1. V_{IL} min: -1.0 V for pulse width \leq 50 ns.
 2. $V_{IH} = 2.2$ V for $V_{CC} = 3.6$ to 5.5 V.
 3. V_{IH} max: $V_{CC} + 1.0$ V for pulse width \leq 50 ns.
 4. This function is supported by only the HN58V66A series.
 5. $V_{IL} = 0.8$ V for $V_{CC} = 3.6$ V to 5.5 V

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	2* ¹	μA	V _{in} = 0 V to V _{CC}
Output leakage current	I _{LO}	—	—	2	μA	V _{out} = 0 V to V _{CC}
Standby V _{CC} current	I _{CC1}	—	1 to 2	5	μA	$\overline{CE} = V_{CC} - 0.3 \text{ V to } V_{CC} + 1.0 \text{ V}$
	I _{CC2}	—	—	1	mA	$\overline{CE} = V_{IH}$
Operating V _{CC} current	I _{CC3}	—	—	6	mA	I _{out} = 0 mA, Duty = 100%, Cycle = 1 μs, V _{CC} = 3.6 V
				8	mA	I _{out} = 0 mA, Duty = 100%, Cycle = 1 μs, V _{CC} = 5.5 V
				12	mA	I _{out} = 0 mA, Duty = 100%, Cycle = 100 ns, V _{CC} = 3.6 V
				25	mA	I _{out} = 0 mA, Duty = 100%, Cycle = 70 ns, V _{CC} = 5.5 V
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	V _{CC} × 0.8	—	—	V	I _{OH} = -400 μA

Note: 1. I_{LI} on RES : 100 μA max (only the HN58V66A series)

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C _{in} * ¹	—	—	6	pF	V _{in} = 0 V
Output capacitance	C _{out} * ¹	—	—	12	pF	V _{out} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Test Conditions

- Input pulse levels : 0.4 V to 2.4 V (V_{CC} = 2.7 to 3.6 V), 0.4 V to 3.0 V (V_{CC} = 3.6 to 5.5 V)
0 V to V_{CC} ($\overline{\text{RES}}$ pin^{*2})
- Input rise and fall time : ≤ 5 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle 1 (2.7 V ≤ V_{CC} < 4.5 V)

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Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t _{ACC}	—	100	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{CE}}$ to output delay	t _{CE}	—	100	ns	$\overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{OE}}$ to output delay	t _{OE}	10	50	ns	$\overline{\text{CE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$
Address to output hold	t _{OH}	0	—	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{OE}}$ ($\overline{\text{CE}}$) high to output float ^{*1}	t _{DF}	0	40	ns	$\overline{\text{CE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{RES}}$ low to output float ^{*1,2}	t _{DFR}	0	350	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{RES}}$ to output delay ^{*2}	t _{RR}	0	450	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$

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Write Cycle 1 ($2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$)

Parameter	Symbol	Min ^{*3}	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
\overline{CE} to write setup time (\overline{WE} controlled)	t_{CS}	0	—	—	ns	
\overline{CE} hold time (\overline{WE} controlled)	t_{CH}	0	—	—	ns	
\overline{WE} to write setup time (\overline{CE} controlled)	t_{WS}	0	—	—	ns	
\overline{WE} hold time (\overline{CE} controlled)	t_{WH}	0	—	—	ns	
\overline{OE} to write setup time	t_{OES}	0	—	—	ns	
\overline{OE} hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
\overline{WE} pulse width (\overline{WE} controlled)	t_{Wp}	200	—	—	ns	
\overline{CE} pulse width (\overline{CE} controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.3	—	30	μs	
Byte load window	t_{BL}	100	—	—	μs	
Write cycle time	t_{WC}	—	—	10^{*4}	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0^{*5}	—	—	ns	
Reset protect time ^{*2}	t_{RP}	100	—	—	μs	
Reset high time ^{*2,6}	t_{RES}	1	—	—	μs	

- Notes:
- t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
 - This function is supported by only the HN58V66A series.
 - Use this device in longer cycle than this value.
 - t_{WC} must be longer than this value unless polling techniques or $\overline{RDY}/\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
 - Next read or write operation can be initiated after t_{DW} if polling techniques or $\overline{RDY}/\overline{Busy}$ are used.
 - This parameter is sampled and not 100% tested.
 - A6 through A12 are page addresses and these addresses are latched at the first falling edge of \overline{WE} .
 - A6 through A12 are page addresses and these addresses are latched at the first falling edge of \overline{CE} .
 - See AC read characteristics.

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Read Cycle 2 ($4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)

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-10					
Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	70	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
\overline{CE} to output delay	t_{CE}	—	70	ns	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
\overline{OE} to output delay	t_{OE}	10	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
\overline{OE} (\overline{CE}) high to output float* ¹	t_{DF}	0	30	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
\overline{RES} low to output float* ^{1,2}	t_{DFR}	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$
\overline{RES} to output delay* ²	t_{RR}	0	450	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$

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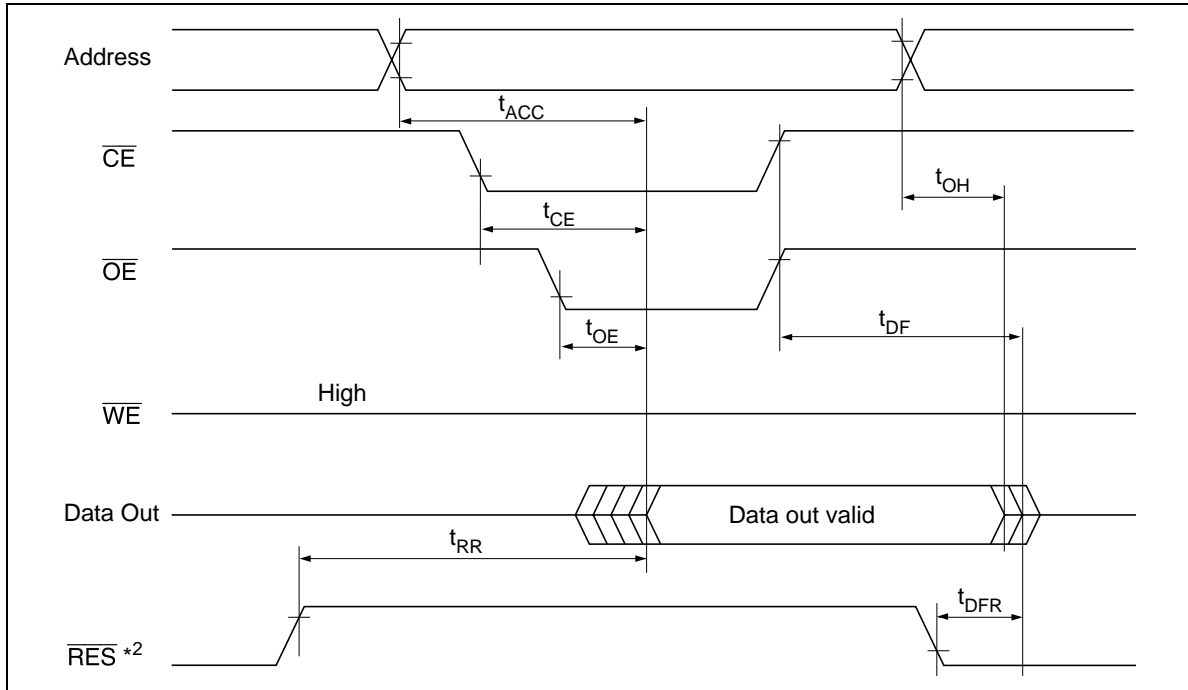
Write Cycle 2 ($4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)

Parameter	Symbol	Min ^{*3}	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
\overline{CE} to write setup time (\overline{WE} controlled)	t_{CS}	0	—	—	ns	
\overline{CE} hold time (\overline{WE} controlled)	t_{CH}	0	—	—	ns	
\overline{WE} to write setup time (\overline{CE} controlled)	t_{WS}	0	—	—	ns	
\overline{WE} hold time (\overline{CE} controlled)	t_{WH}	0	—	—	ns	
\overline{OE} to write setup time	t_{OES}	0	—	—	ns	
\overline{OE} hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
\overline{WE} pulse width (\overline{WE} controlled)	t_{Wp}	100	—	—	ns	
\overline{CE} pulse width (\overline{CE} controlled)	t_{CW}	100	—	—	ns	
Data latch time	t_{DL}	50	—	—	ns	
Byte load cycle	t_{BLC}	0.2	—	30	μs	
Byte load window	t_{BL}	100	—	—	μs	
Write cycle time	t_{WC}	—	—	10^{*4}	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0^{*5}	—	—	ns	
Reset protect time ^{*2}	t_{RP}	100	—	—	μs	
Reset high time ^{*2,6}	t_{RES}	1	—	—	μs	

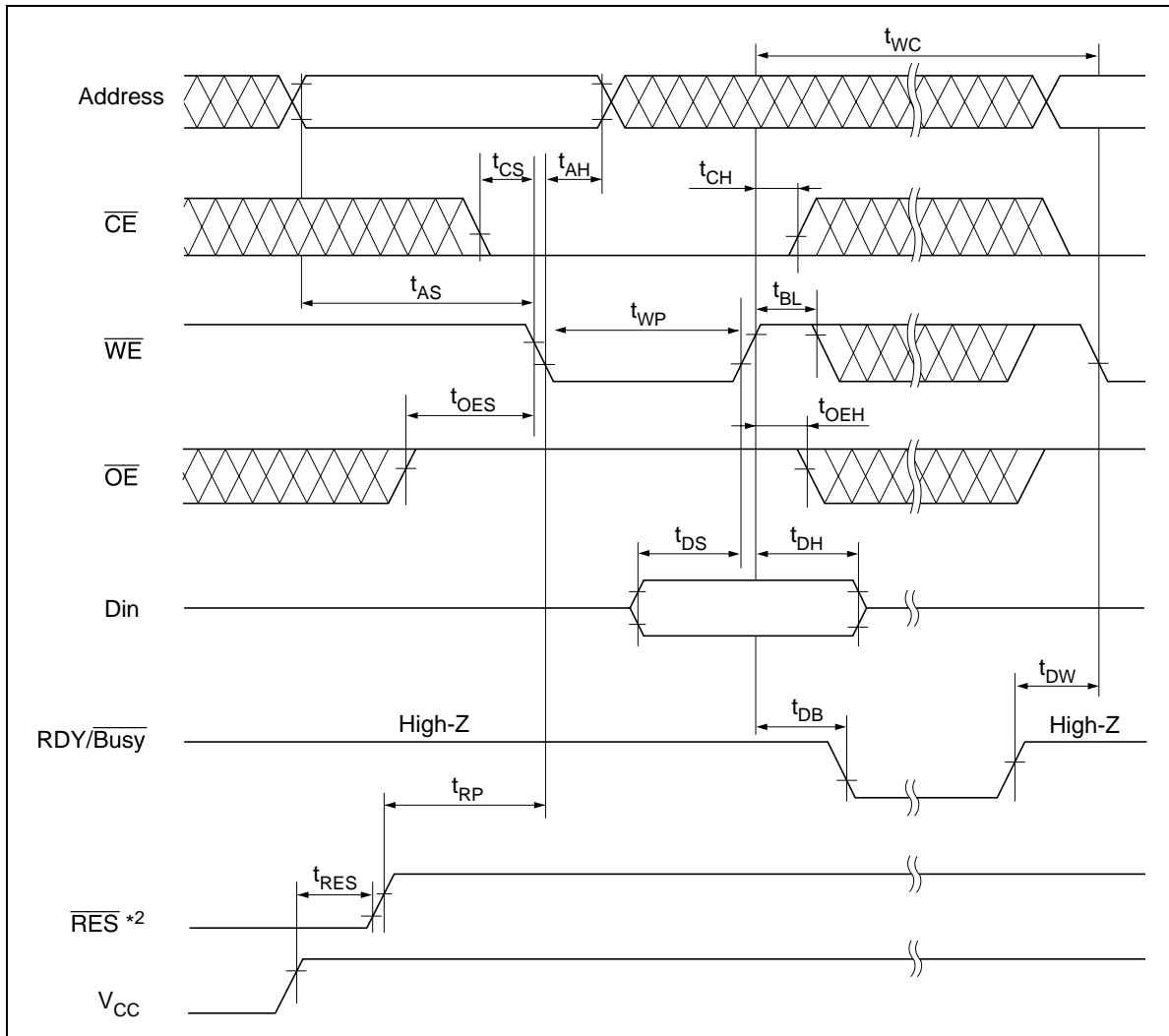
- Notes:
- t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
 - This function is supported by only the HN58V66A series.
 - Use this device in longer cycle than this value.
 - t_{WC} must be longer than this value unless polling techniques or $\overline{RDY}/\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
 - Next read or write operation can be initiated after t_{DW} if polling techniques or $\overline{RDY}/\overline{Busy}$ are used.
 - This parameter is sampled and not 100% tested.
 - A6 through A12 are page addresses and these addresses are latched at the first falling edge of \overline{WE} .
 - A6 through A12 are page addresses and these addresses are latched at the first falling edge of \overline{CE} .
 - See AC read characteristics.

Timing Waveforms

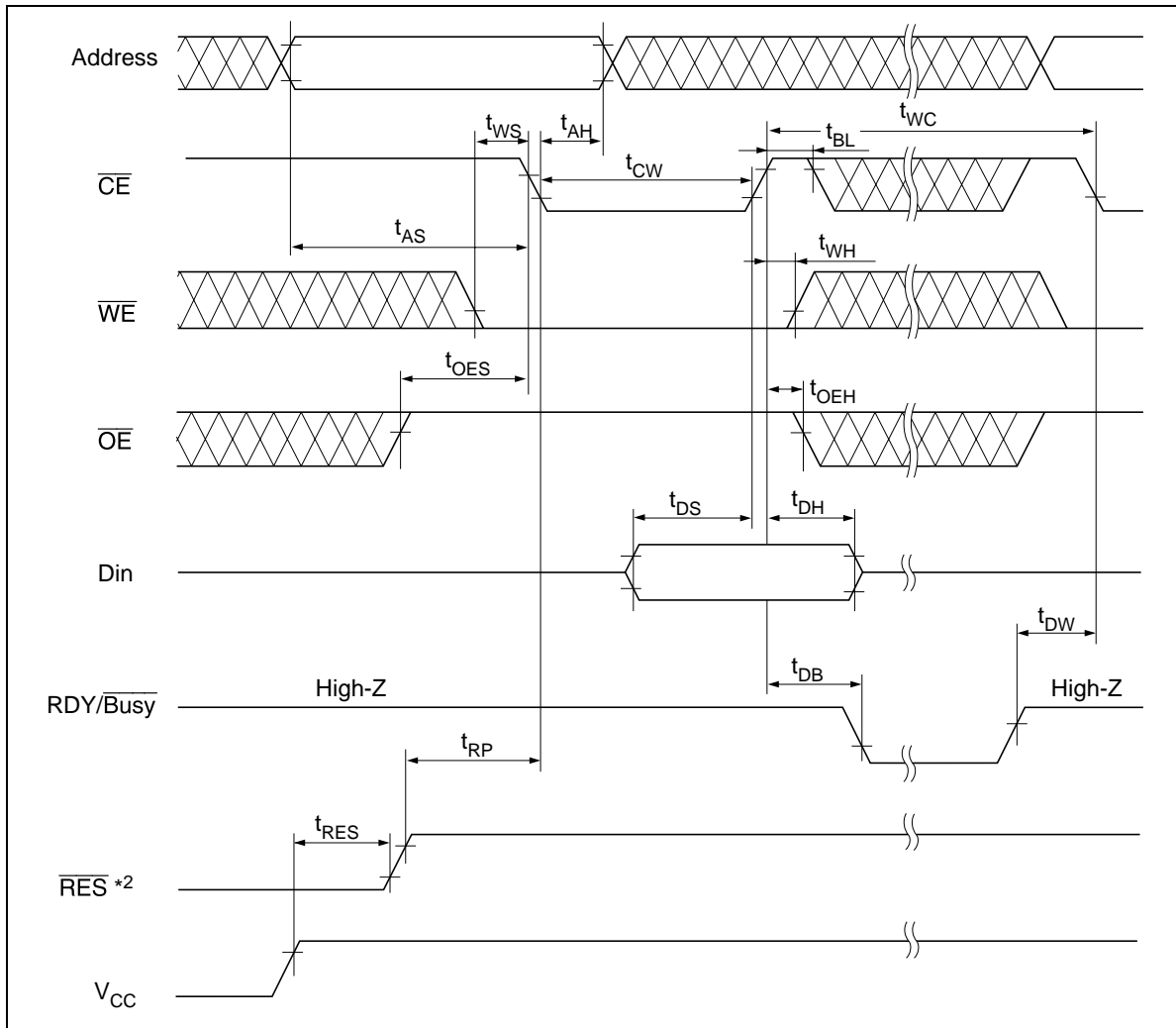
Read Timing Waveform



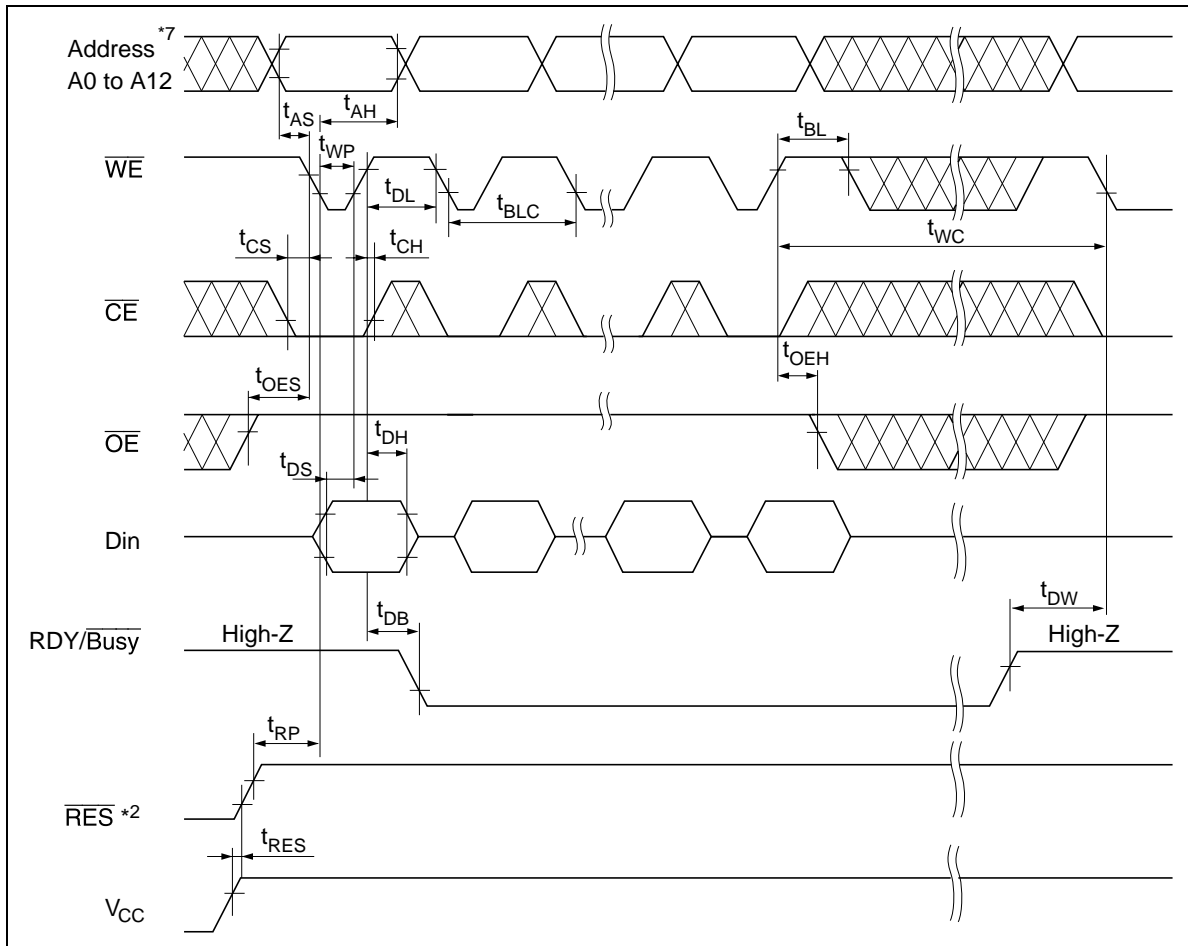
Byte Write Timing Waveform(1) (\overline{WE} Controlled)



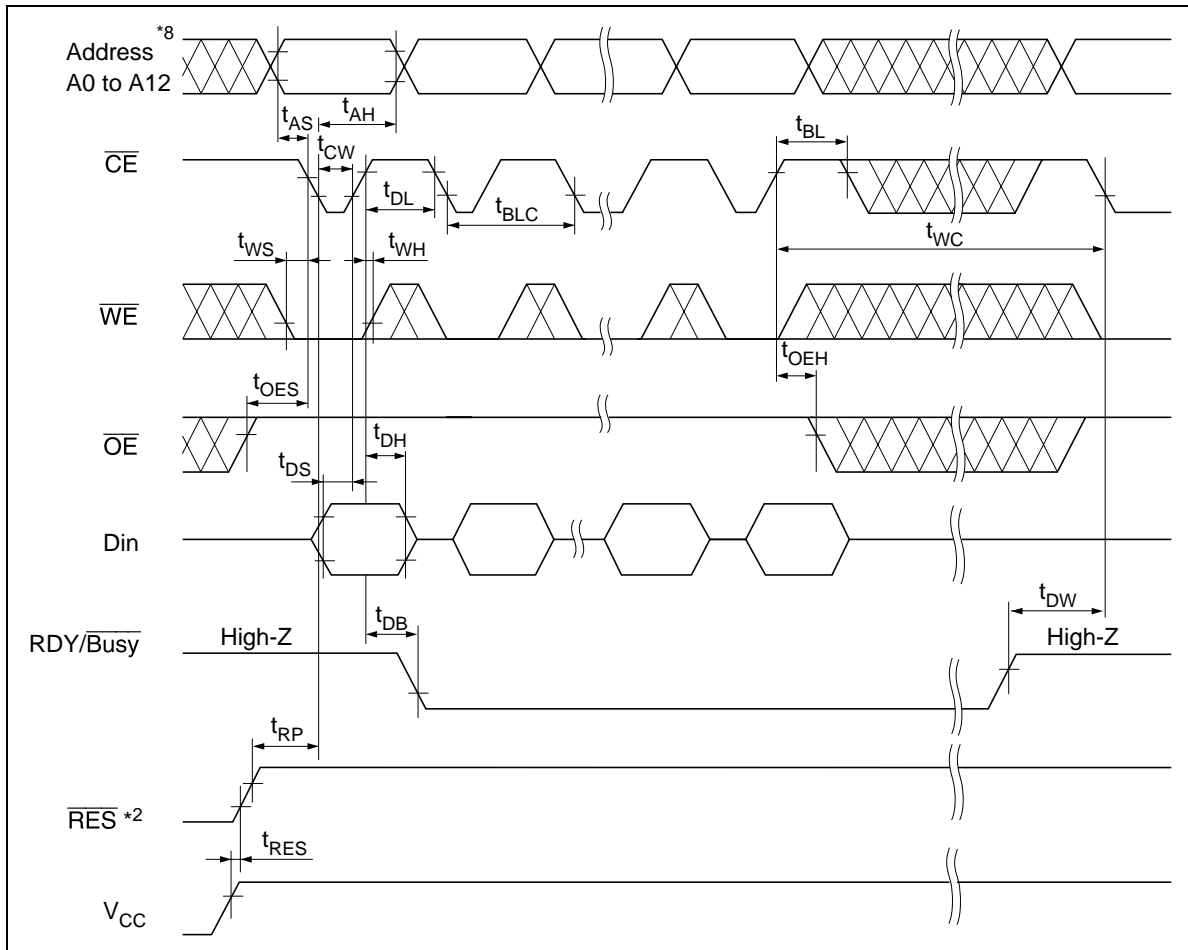
Byte Write Timing Waveform(2) ($\overline{\text{CE}}$ Controlled)



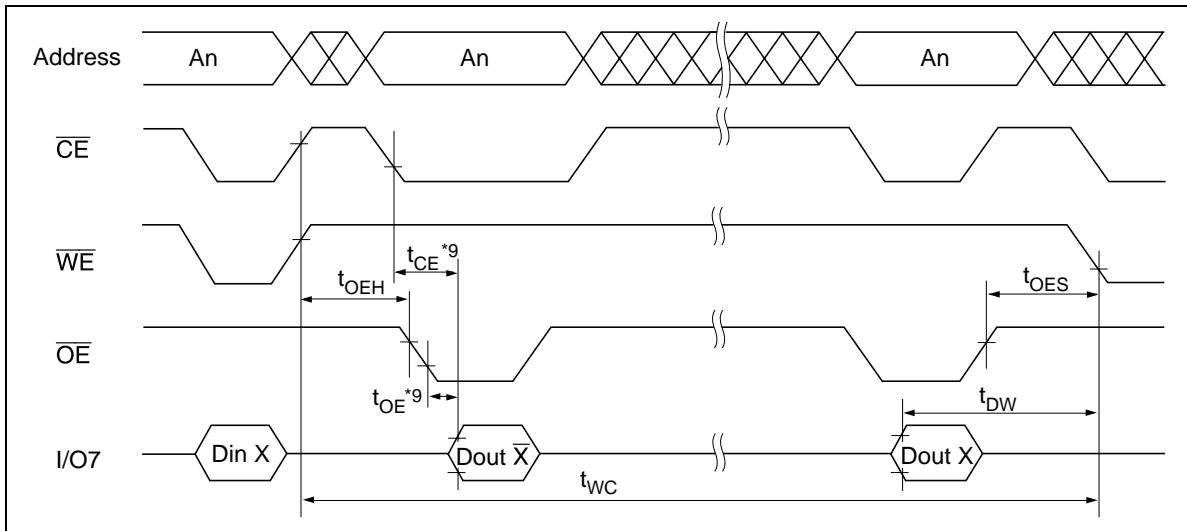
Page Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



Page Write Timing Waveform(2) (\overline{CE} Controlled)



Data Polling Timing Waveform

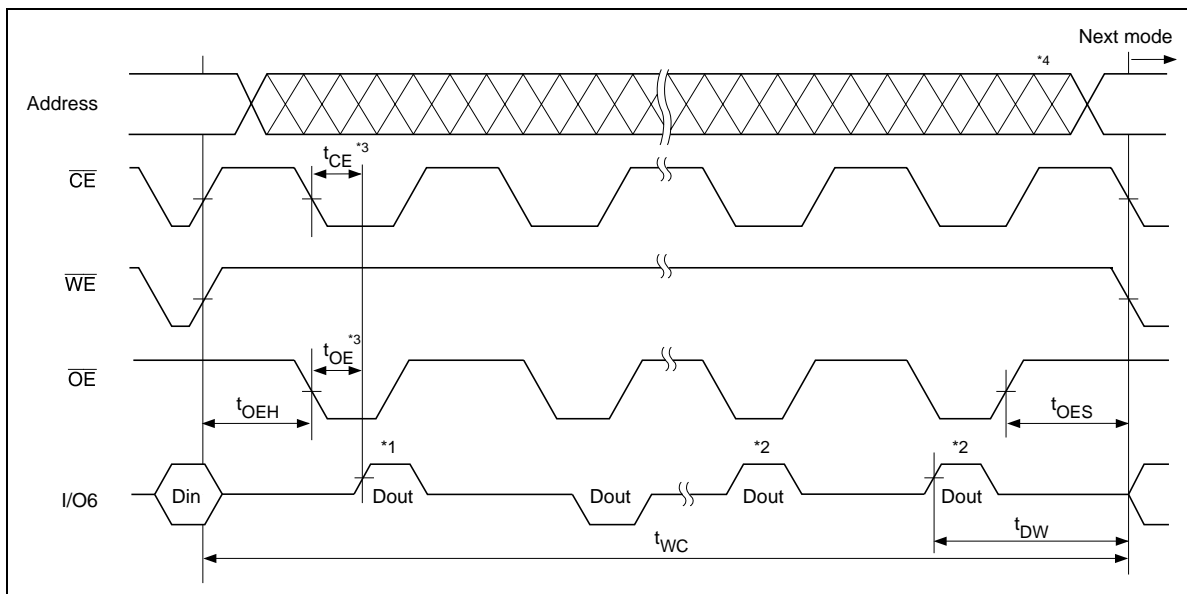


Toggle Bit

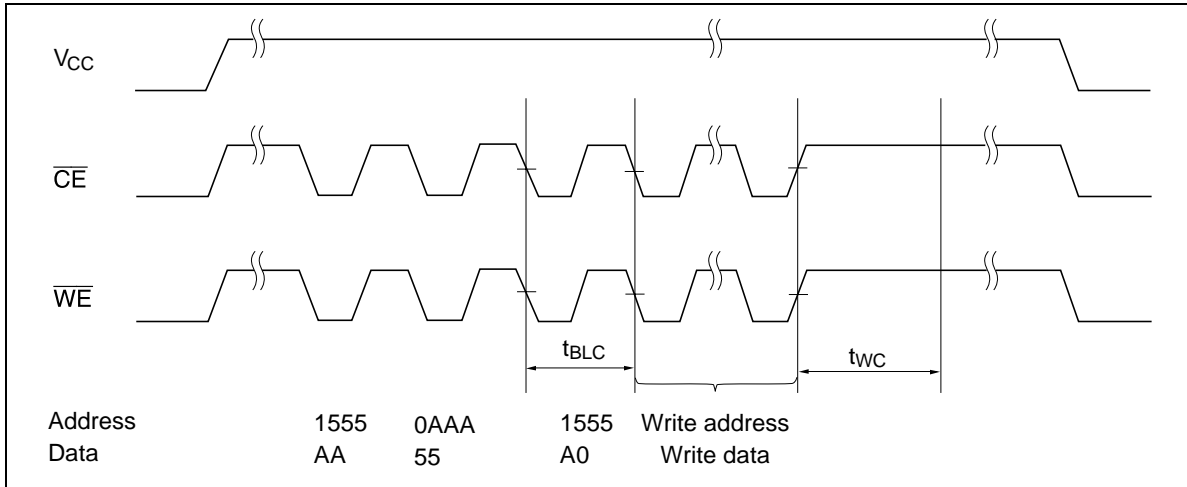
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

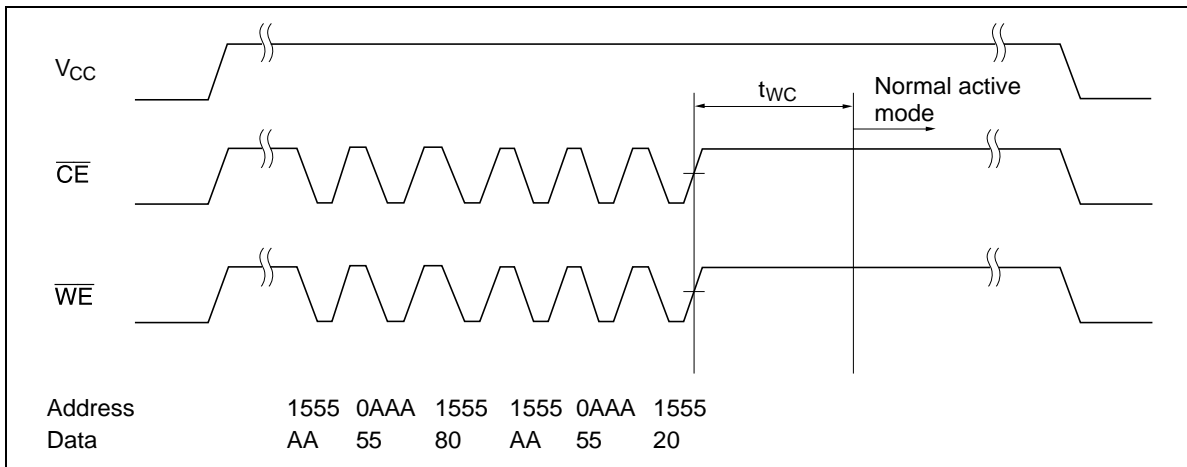
- Notes:
1. I/O6 beginning state is “1”.
 2. I/O6 ending state will vary.
 3. See AC read characteristics.
 4. Any address location can be used, but the address must be fixed.



Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μ s from the preceding falling edge of \overline{WE} or \overline{CE} . When \overline{CE} or \overline{WE} is kept high for 100 μ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

Data Polling

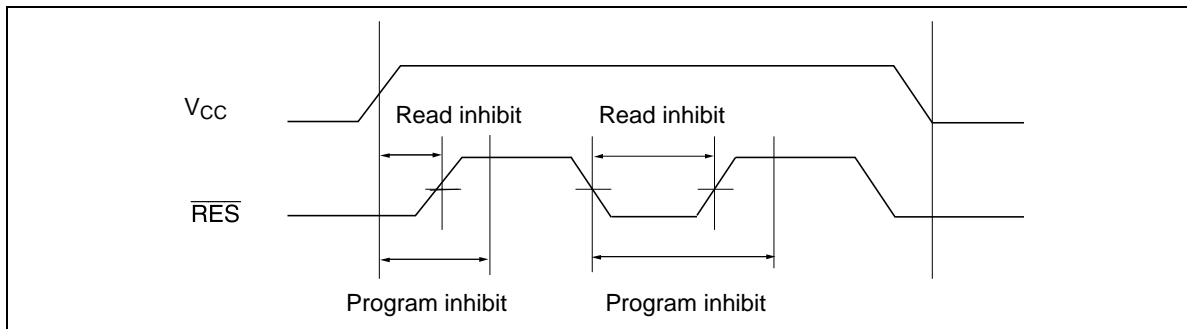
Data polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/ \overline{Busy} Signal

RDY/ \overline{Busy} signal also allows status of the EEPROM to be determined. The RDY/ \overline{Busy} signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/ \overline{Busy} signal changes state to high impedance.

\overline{RES} Signal (only the HN58V66A series)

When \overline{RES} is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping \overline{RES} low when V_{CC} is switched. \overline{RES} should be high during read and programming because it doesn't provide a latch function.



$\overline{\text{WE}}$, $\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, and data is latched by the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

Write/Erase Endurance and Data Retention Time

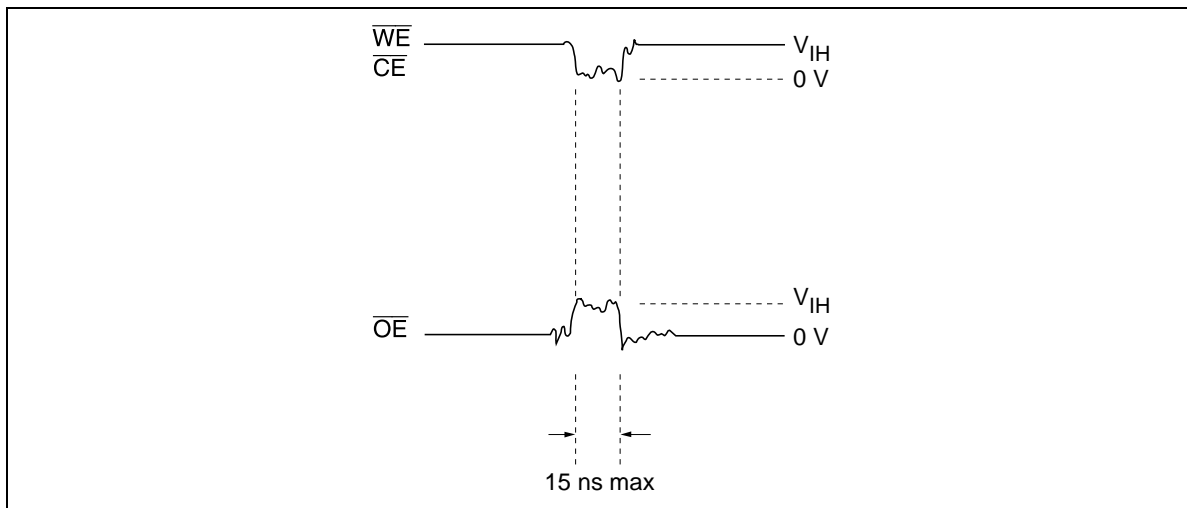
The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 15 ns or less.

1. Data Protection against Noise on Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 15 ns on the control pins.

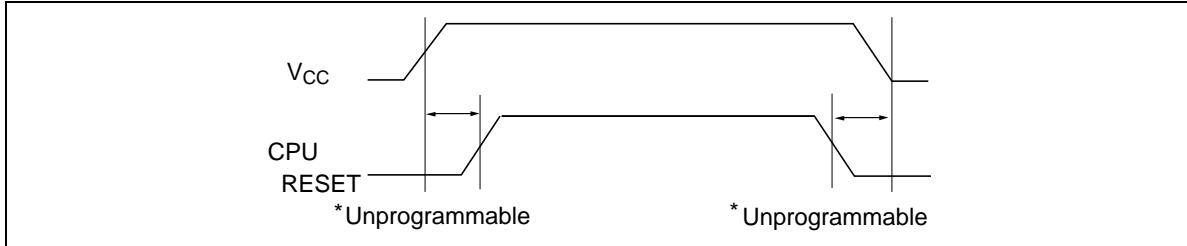


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2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



2.1 Protection by \overline{CE} , \overline{OE} , \overline{WE}

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

\overline{CE}	V_{CC}	×	×
\overline{OE}	×	V_{SS}	×
\overline{WE}	×	×	V_{CC}

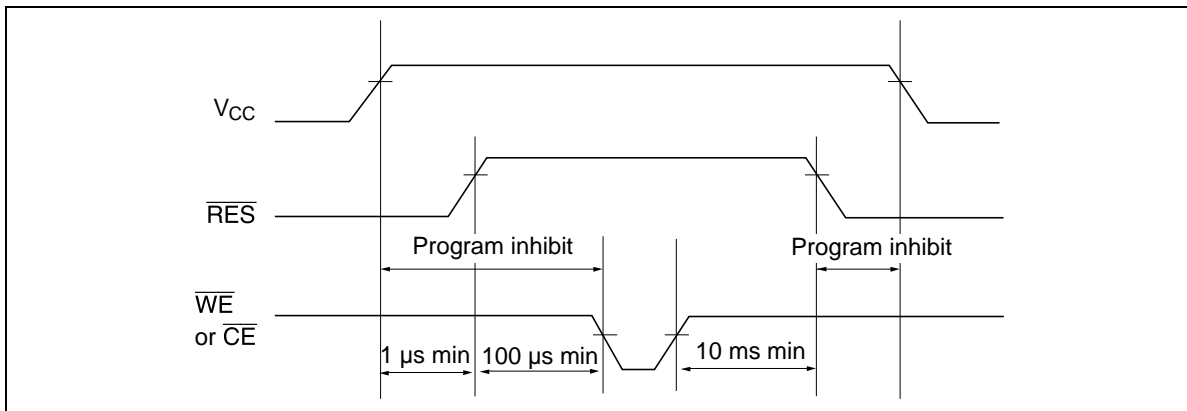
×: Don't care.

V_{CC} : Pull-up to V_{CC} level.

V_{SS} : Pull-down to V_{SS} level.

2.2 Protection by \overline{RES} (only the HN58V66A series)

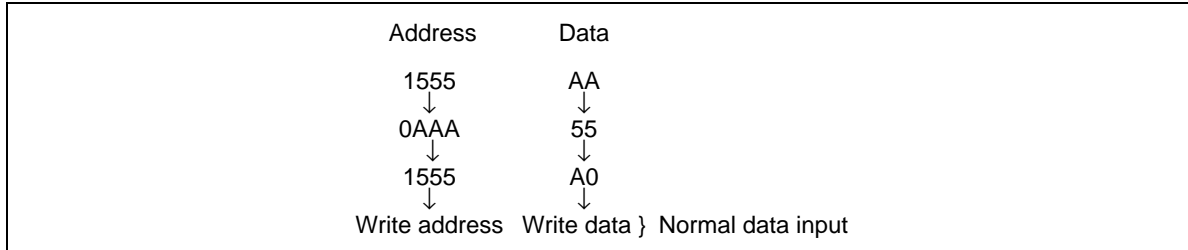
The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's \overline{RES} pin. \overline{RES} should be kept V_{SS} level during V_{CC} on/off. The EEPROM breaks off programming operation when \overline{RES} becomes low, programming operation doesn't finish correctly in case that \overline{RES} falls low during programming operation. \overline{RES} should be kept high for 10 ms after the last data input.



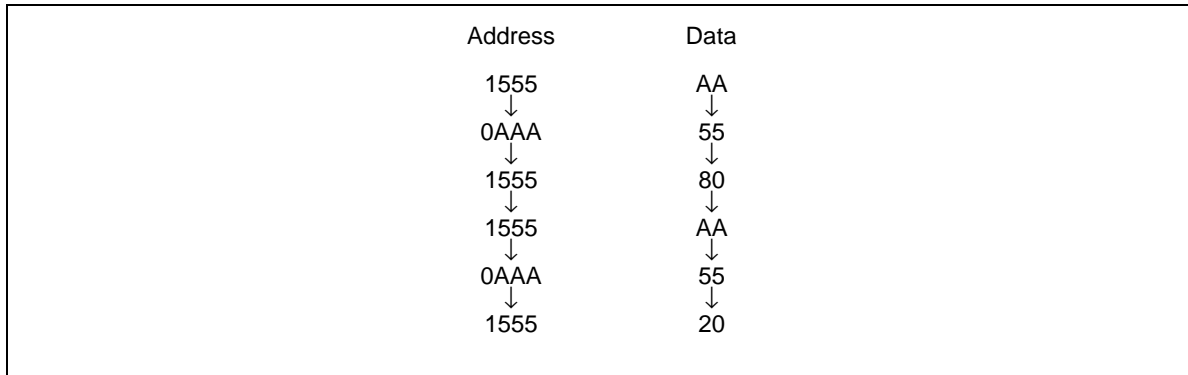
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3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, this device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode. SDP is enabled if only the 3 bytes code is input.



Software data protection mode can be cancelled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the cancelling cycle, the data cannot be written.



The software data protection is not enabled at the shipment.

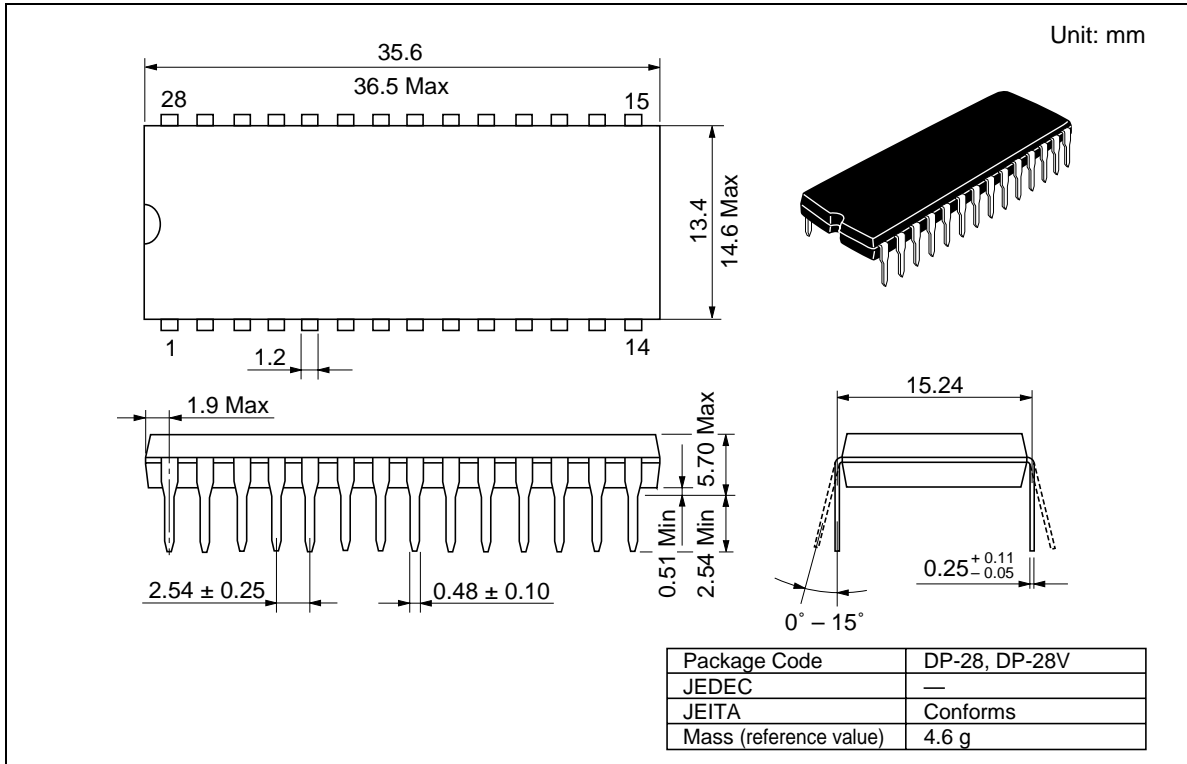
Note: There are some differences between Renesas Technology's and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Renesas Technology's sales offices.

HN58V65A Series, HN58V66A Series

Package Dimensions

HN58V65AP Series

HN58V66AP Series (DP-28, DP-28V)

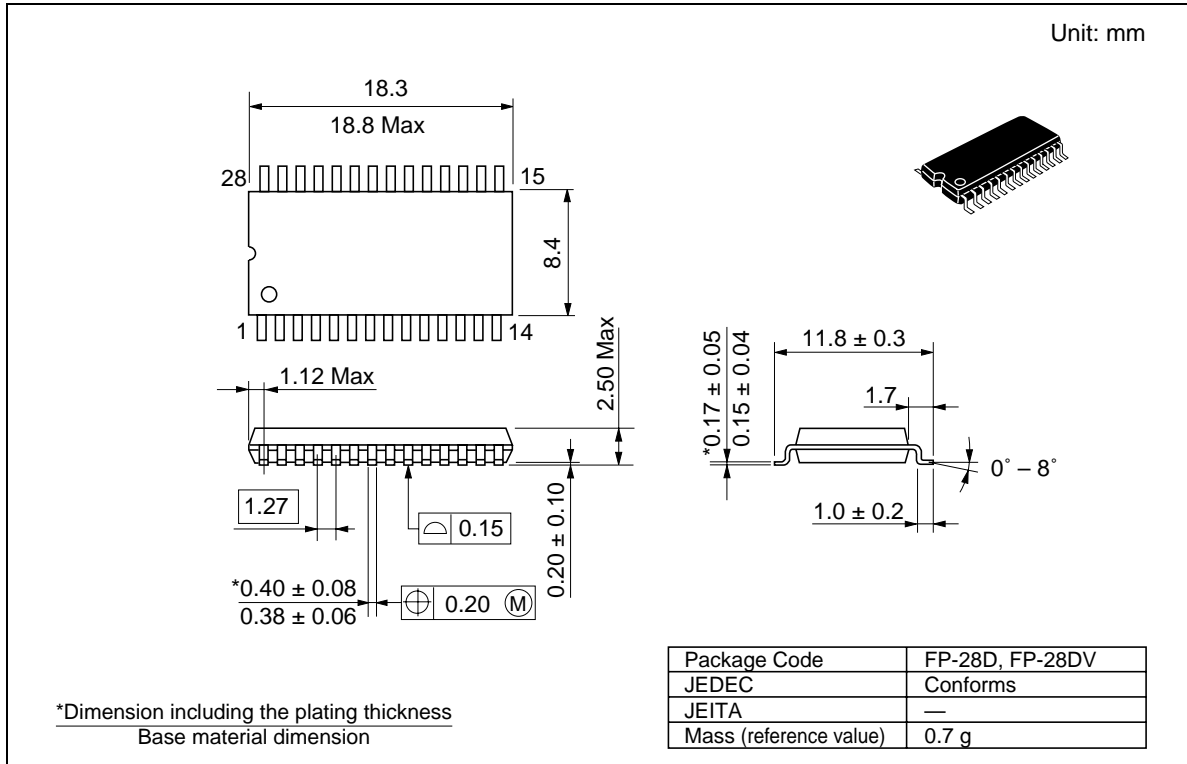


HN58V65A Series, HN58V66A Series

Package Dimensions (cont)

HN58V65AFP Series

HN58V66AFP Series (FP-28D, FP-28DV)

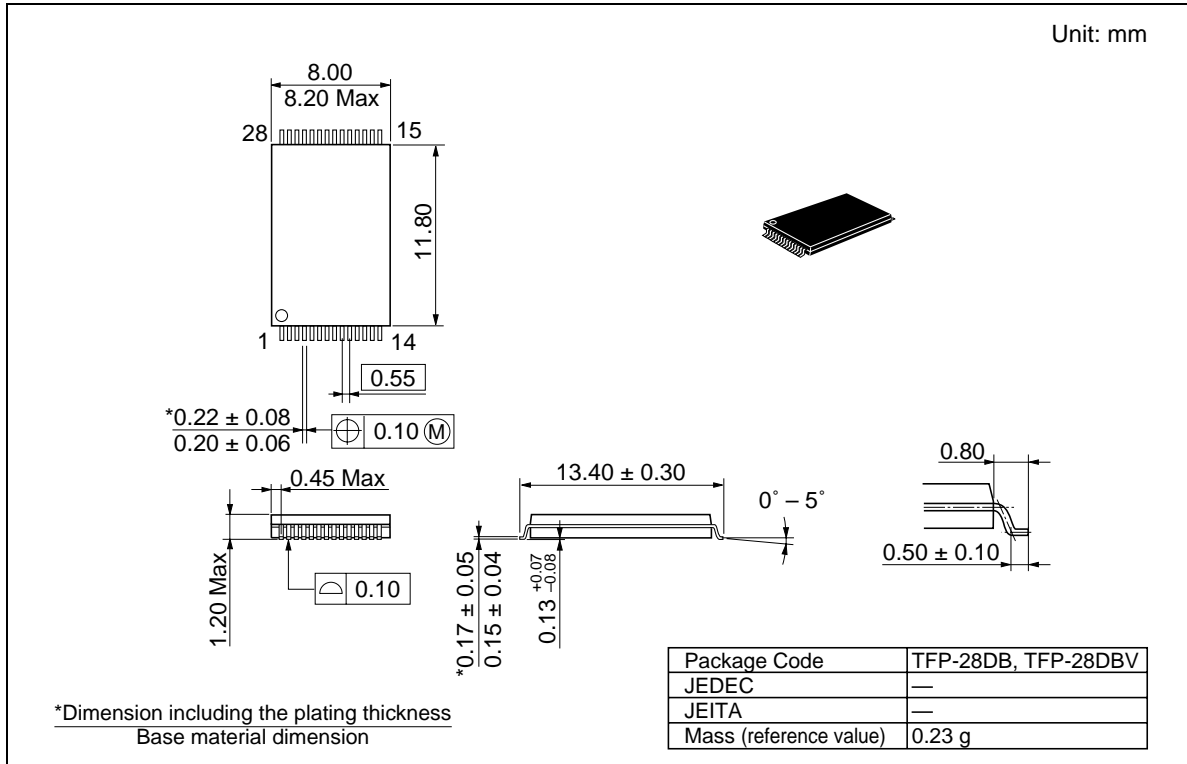


HN58V65A Series, HN58V66A Series

Package Dimensions (cont)

HN58V65AT Series

HN58V66AT Series (TFP-28DB, TFP-28DBV)



Revision History

HN58V65A/HN58V66A Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.0	Mar. 18. 1996	—	Initial issue
0.1	Nov. 12. 1996	— —	Change of FP-28DA to DP-28 Addition of 5 V specification
0.2	Mar. 7. 1997	— 6 7	Change of page size: 32 byte to 64 byte Recommended DC Operating Conditions V_{CC} (typ) : 0.3 V to — Addition of note 5 Change of note 2 ($V_{IH} = 2.4$ V to $V_{IH} = 2.2$ V) DC Characteristics I_{CC1} (min/typ/max): —/—/20 μ A to —/1 to 2/5 μ A Change of Test conditions I_{L1} : $V_{CC} = 5.5$ V, $V_{in} = 5.5$ V to $V_{in} = 0$ V to V_{CC} I_{L0} : $V_{CC} = 5.5$ V, $V_{out} = 5.5/0.4$ V to $V_{out} = 0$ V to V_{CC} I_{CC1} : $\overline{CE} = V_{CC}$ to $\overline{CE} = V_{CC} - 0.3$ V to $V_{CC} + 1$ V
1.0	Aug. 28. 1997	7 8 12 20	DC Characteristics ICC_3 : —/—/10 μ A to —/—/8 μ A AC Characteristic Input pules level: 0.4 V to V_{SS} to 0 V to V_{SS} Timing Waveform Read Timing Waveform: Correct error Functional Description Data Protection: Addition of description
2.0	Jan. 22.1998	—	Change of Subtitle
3.00	Dec. 04. 2003	— 2 24-26	Change format issued by Renesas Technology Corp. Ordering Information Addition of HN58V65AP-10E, HN58V66AP-10E, HN58V65AFP-10E, HN58V66AFP-10E, HN58V65AT-10E, HN58V66AT-10E Package Dimensions DP-28 to DP-28, DP-28V FP-28D to FP-28D, FP-28DV TFP-28DB to TFP-28DB, TFP-28DBV

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