Dual-Channel Isolators with Integrated DC/DC Converter

Preliminary Technical Data

ADuM5200/5201/5202

FEATURES

***iso*Power™ integrated isolated DC/DC converter**
Regulated 3V or 5V output
500mW output power
Dual dc-to-25 Mbps (NRZ) signal isolation channels
Schmitt Trigger Inputs
SOIC 16-lead package with > 8mm creepage
High temperature operation: 105°C
High common-mode transient immunity: > 25 kV/µs
Safety and regulatory approvals (pending)
- **UL recognition**
  - **2500 V rms for 1 minute per UL 1577**
- **CSA component acceptance notice #5A**
- **VDE certificate of conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
  - **V_{IORM} = 560 V peak**

APPLICATIONS

RS-232/RS-422/RS-485 transceiver
Industrial field bus isolation
Power Supply start up and Gate Drive
Isolated Sensor Interface
Industrial PLC

GENERAL DESCRIPTION

The ADuM520x[1] are dual-channel digital isolators with isoPower, an integrated, isolated DC/DC converter. Based on Analog Devices' *i*Coupler® technology, the DC/DC converter provides up to 500 mW of regulated, isolated power at either 5.0V from a 5.0V input supply or 3.3V from a 3.3V or 5.0V supply. This eliminates the need for a separate isolated DC/DC converter in low-power isolated designs. Analog Devices' chip-scale transformer *i*Coupler technology is used both for the isolation of the logic signals as well as for the DC/DC converter. The result is a small form-factor total-isolation solution.

ADuM520x units may be used in combination with ADuM540x and ADuM5000 with *iso*Power to achieve higher output power levels and greater channel counts.

The ADuM520x isolators provide two independent isolation channels in a variety of channel configurations and data rates (see Ordering Guide).

FUNCTIONAL BLOCK DIAGRAMS

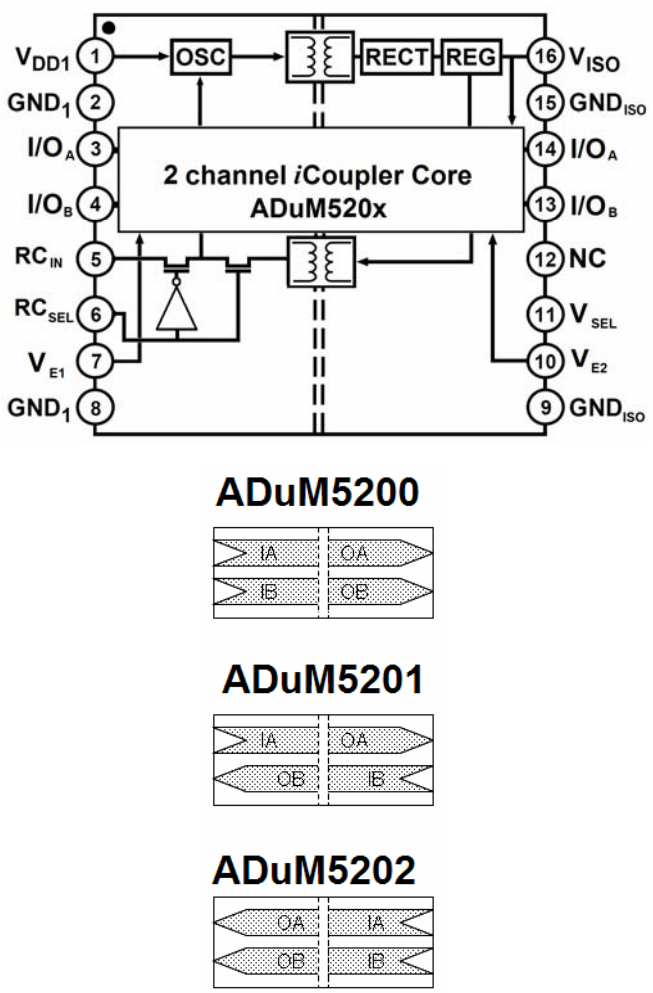

Figure 1ADuM520x Functional Diagrams

[1] Protected by U.S. Patents 5,952,849, 6,873,065. and 7075 329 B2, Other patents pending.

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS – 5V PRIMARY INPUT SUPPLY / 5V SECONDARY ISOLATED SUPPLY[1]

4.5 V ≤ V_{DD1} ≤ 5.5 V, V_{SEL}=V_{ISO}; all voltages are relative to their respective ground. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD} = 5.0 V, V_{ISO} = 5.0 V, V_{SEL}= V_{ISO}.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Setpoint	V_{ISO}	4.7	5.0	5.4	V	I_{ISO}=0mA
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	I_{ISO}=50mA, V_{DD1}=4.5V to 5.5V
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	I_{ISO} = 10mA to 90mA
Output Ripple	$V_{ISO(RIP)}$		75		mV_{P-P}	20MHz Bandwidth, C_{BO}=0.1µF ‖ 10µF, I_{ISO} = 100mA
Output Noise	$V_{ISO(N)}$		200		mV_{P-P}	20MHz Bandwidth, C_{BO}=0.1µF ‖ 10µF, I_{ISO} = 100mA
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
DC to 2 Mbps Data Rate[2]						
Maximum Output Supply Current[3]	$I_{ISO(max)}$	100			mA	f ≤ 1 MHz, V_{ISO}=5V
Efficiency At Max. Output Supply Current[4]			34		%	I_{ISO} = $I_{ISO(2,max)}$, f ≤ 1 MHz
I_{DD1} Supply Current, No V_{ISO} load[5]	$I_{DD1(Q)}$		19	30	mA	I_{ISO} = 0mA, f ≤ 1 MHz
25 Mbps Data Rate (CRWZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load[6]						
ADuM5200	$I_{DD1(D)}$		34		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
ADuM5201	$I_{DD1(D)}$		38		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
ADuM5202	$I_{DD1(D)}$		41		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
Available V_{ISO} Supply Current[7]						
ADuM5200	$I_{ISO(LOAD)}$		94		mA	C_L=15pF, f = 12.5 MHz
ADuM5201	$I_{ISO(LOAD)}$		92		mA	C_L=15pF, f = 12.5 MHz
ADuM5202	$I_{ISO(LOAD)}$		90		mA	C_L=15pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} load[8]	$I_{DD1(Max)}$		290		mA	C_L=0pF, f = 0 MHz, V_{DD} = 5V I_{ISO}=100mA
I/O Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}	0.7 V_{ISO}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD1} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
	V_{OAH}, V_{OBH}	V_{DD1} − 0.3, V_{ISO} − 0.3	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
	V_{OAL}, V_{OBL}		0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
ADuM520xARWZ						
Minimum Pulse Width[9]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[10]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[11]	t_{PHL}, t_{PLH}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[11]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[12]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[13]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels
ADuM520xCRWZ						
Minimum Pulse Width[9]	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[14]		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[15]	t_{PHL}, t_{PLH}		45	60	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[11]	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[16]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[17]	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[17]	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD}$ or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] All voltages are relative to their respective ground.
[2] The contributions of supply current values for all four channels are combined at identical data rates.
[3] V_{ISO} supply current available for external use when all data rates are below 2Mbps. At data rates above 2Mbps data I/O channels will draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and be included in the V_{ISO} power budget.
[4] The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of its internal power consumption.
[5] $I_{DD1(Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2Mbps, requiring no additional dynamic supply current. It reflects the minimum current operating condition.
[6] $I_{DD1(D)}$ is the typical input supply current with all channels simultaneously driven at maximum data rate of 25Mbps with full capacitive load representing the maximum dynamic load conditions. Resistive loads on the outputs should be treated separately from the dynamic load.
[7] This current is available for driving external loads at the V_{ISO} pin. All channels are simultaneously driven at maximum data rate of 25Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to Power Consumption section for calculation of available current at less than maximum data rate.
[8] $I_{DD1(MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.
[9] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[10] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[11] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[12] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[13] Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

ELECTRICAL CHARACTERISTICS – 3.3V PRIMARY INPUT SUPPLY / 3.3V SECONDARY ISOLATED SUPPLY[1]

3.0 V ≤ V_{DD1} ≤ 3.6 V, V_{SEL}=GND_{ISO}; all voltages are relative to their respective ground. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD} = 3.3 V, V_{ISO} = 3.3 V, V_{SEL}= GND_{ISO}.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Setpoint	V_{ISO}	3.13	3.3	3.37	V	I_{ISO}=0mA
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	I_{ISO}=37.5 mA, V_{DD1}=3.0V to 3.6V
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	I_{ISO} = 6mA to 54mA
Output Ripple	$V_{ISO(RIP)}$		50		mV_{P-P}	20MHz Bandwidth, C_{BO}=0.1μF ‖ 10μF, I_{ISO} = 90mA
Output Noise	$V_{ISO(N)}$		130		mV_{P-P}	20MHz Bandwidth, C_{BO}=0.1μF ‖ 10μF, I_{ISO} = 90mA
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
DC to 2 Mbps Data Rate[2]						
Maximum Output Supply Current[3]	$I_{ISO(max)}$	60			mA	f ≤ 1 MHz, V_{ISO}=3.15V
Efficiency At Max. Output Supply Current[4]			36		%	I_{ISO} = $I_{ISO(2,max)}$, f ≤ 1 MHz
I_{DD1} Supply Current, No V_{ISO} load[5]	$I_{DD1(Q)}$		10	20	mA	I_{ISO} = 0mA, f ≤ 1 MHz
25 Mbps Data Rate (CRWZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load[6]						
ADuM5200	$I_{DD1(D)}$		23		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
ADuM5201	$I_{DD1(D)}$		25		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
ADuM5202	$I_{DD1(D)}$		28		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
Available V_{ISO} Supply Current[7]						
ADuM5200	$I_{ISO(LOAD)}$		106		mA	C_L=15pF, f = 12.5 MHz
ADuM5201	$I_{ISO(LOAD)}$		105		mA	C_L=15pF, f = 12.5 MHz
ADuM5202	$I_{ISO(LOAD)}$		103		mA	C_L=15pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} load[8]	$I_{DD1(Max)}$		175		mA	C_L=0pF, f = 0 MHz, V_{DD} = 3.3V, I_{ISO}=60mA
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	μA	
Logic High Input Threshold	V_{IH}	0.7 × V_{ISO}, 0.7 × V_{IDD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{ISO}, 0.3 × V_{IDD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD1} − 0.2, V_{ISO} − 0.2	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
	V_{OAH}, V_{OBH}	V_{DD1} − 0.5, V_{1SO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
	V_{OAL}, V_{OBL}		0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
ADuM520xARWZ						
Minimum Pulse Width[9]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[10]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[11]	t_{PHL}, t_{PLH}		60	100	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[11]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[12]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[13]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels
ADuM520xCRWZ						

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Minimum Pulse Width[13]	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[14]		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[15]	t_{PHL}, t_{PLH}		45	60	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[11]	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[16]	t_{PSK}			45	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[17]	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[17]	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD}$ or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] All voltages are relative to their respective ground.
[2] The contributions of supply current values for all four channels are combined at identical data rates.
[3] V_{ISO} supply current available for external use when all data rates are below 2Mbps. At data rates above 2Mbps data I/O channels will draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and be included in the V_{ISO} power budget.
[4] The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of its internal power consumption.
[5] $I_{DD1(Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2Mbps, requiring no additional dynamic supply current. It reflects the minimum current operating condition.
[6] $I_{DD1(D)}$ is the typical input supply current with all channels simultaneously driven at maximum data rate of 25Mbps with full capacitive load representing the maximum dynamic load conditions. Resistive loads on the outputs should be treated separately from the dynamic load.
[7] This current is available for driving external loads at the V_{ISO} pin. All channels are simultaneously driven at maximum data rate of 25Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to Power Consumption section for calculation of available current at less than maximum data rate.
[8] $I_{DD1(MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.
[9] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[10] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[11] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[12] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[13] Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

ELECTRICAL CHARACTERISTICS – 5V PRIMARY INPUT SUPPLY / 3.3V SECONDARY ISOLATED SUPPLY[1]

4.5 V ≤ V_{DD1} ≤ 5.5 V, V_{SEL}= GND_{ISO}, all voltages are relative to their respective ground. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD} = 5.0 V, V_{ISO} = 3.3 V, V_{SEL}= GND_{ISO}.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Setpoint	V_{ISO}	3.0	3.3	3.6	V	I_{ISO}=0mA
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	I_{ISO}=50mA, V_{DD1}=4.5V to 5.5V
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	I_{ISO} = 10mA to 100mA
Output Ripple	$V_{ISO(RIP)}$		50		mV_{P-P}	20MHz Bandwidth, C_{BO}=0.1μF ‖ 10μF, I_{ISO} = 90mA
Output Noise	$V_{ISO(N)}$		130		mV_{P-P}	20MHz Bandwidth, C_{BO}=0.1μF ‖ 10μF, I_{ISO} = 90mA
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
DC to 2 Mbps Data Rate[2]						
Maximum Output Supply Current[3]	$I_{ISO(max)}$	100			mA	f ≤ 1 MHz, V_{ISO}=3.0V
Efficiency At Max. Output Supply Current[4]			30		%	I_{ISO} = $I_{ISO(2,max)}$, f ≤ 1 MHz
I_{DD1} Supply Current, No V_{ISO} load[5]	$I_{DD1(Q)}$		9	13	mA	I_{ISO} = 0mA, f ≤ 1 MHz
25 Mbps Data Rate (CRWZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load[6]						
ADuM5200	$I_{DD1(D)}$		22		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
ADuM5201	$I_{DD1(D)}$		25		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
ADuM5202	$I_{DD1(D)}$		27		mA	I_{ISO} = 0mA, C_L=15pF, f = 12.5 MHz
Available V_{ISO} Supply Current[7]						
ADuM5200	$I_{ISO(LOAD)}$		96		mA	C_L=15pF, f = 12.5 MHz
ADuM5201	$I_{ISO(LOAD)}$		95		mA	C_L=15pF, f = 12.5 MHz
ADuM5202	$I_{ISO(LOAD)}$		93		mA	C_L=15pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} load[8]	$I_{DD1(Max)}$		230		mA	C_L=0pF, f = 0 MHz, V_{DD} = 5V, I_{ISO}=100mA
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	μA	
Logic High Input Threshold	V_{IH}	0.7 V_{ISO}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD1} − 0.2, V_{ISO} − 0.2	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
	V_{OAH}, V_{OBH}	V_{DD1} − 0.5, V_{1SO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
	V_{OAL}, V_{OBL}		0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
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Minimum Pulse Width[9]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[10]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[11]	t_{PHL}, t_{PLH}		60	100	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[11]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[12]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[13]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels
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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[11]	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[16]	t_{PSK}			45	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[17]	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[17]	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD}$ or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

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[4] The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of its internal power consumption.
[5] $I_{DD1(Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2Mbps, requiring no additional dynamic supply current. It reflects the minimum current operating condition.
[6] $I_{DD1(D)}$ is the typical input supply current with all channels simultaneously driven at maximum data rate of 25Mbps with full capacitive load representing the maximum dynamic load conditions. Resistive loads on the outputs should be treated separately from the dynamic load.
[7] This current is available for driving external loads at the V_{ISO} pin. All channels are simultaneously driven at maximum data rate of 25Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to Power Consumption section for calculation of available current at less than maximum data rate.
[8] $I_{DD1(MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.
[9] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[10] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[11] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[12] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[13] Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{CA}		45		°C/W	Thermocouple located at center of package underside, test conducted on 4 layer board with thin traces[3].
Thermal Shutdown						
Thermal Shutdown Threshold	TS_{SD}		150		°C	T_J Rising
Thermal Shutdown Hysteresis	TS_{SD-HYS}		20		°C	

[1] Device considered a 2-terminal device; Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] Refer to the Power Considerations section for thermal model definitions

Table 5.

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Reinforced insulation, 2500 V rms isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 300 V rms (424 V peak)maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL1577, each ADuM520x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 µA).
2 In accordance with DIN V VDE V 0884-10, each ADuM520x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

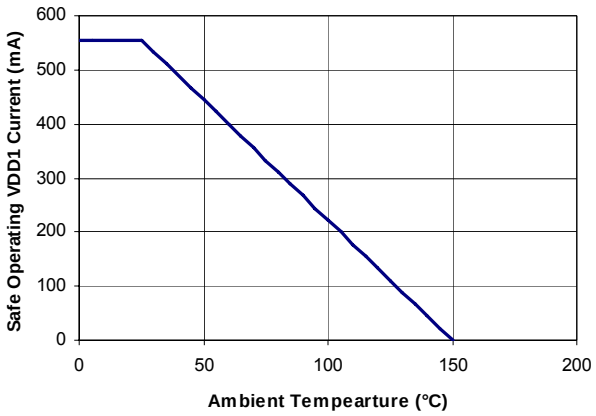


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]				
V_{DD} @ V_{SEL}=0V	V_{DD}	3.0	5.5	V
V_{DD} @ V_{SEL}=5V	V_{DD}	4.5	5.5	V
Minimum Load	$I_{ISO(MIN)}$	10		mA

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD}, V_{ISO})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB}, V_{E1}, V_{E2},RC_{SEL}, V_{SEL})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−18 mA to +18 mA
Side 2(I_{OISO})	−22 mA to +22 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 2 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	424	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	600	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Basic Insulation	600	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 11. Truth Table (Positive Logic)

RC_{IN} Input	RC_{SEL} Output	V_{SEL} Input[1]	V_{DDI} Input	V_{ISO} Output	V_{IX} Input	V_{OX} Output	Notes
X	H	H	5.0V	5.0V	X	X	Master mode operation, Self Regulating
X	H	L	5.0V	3.3V	X	X	Master mode operation, Self Regulating
X	H	H	3.3V	5.0V	X	X	Master mode operation, Self Regulating
X	H	L	3.3V	3.3V	X	X	Master mode operation, Self Regulating
EXT-PWM	L	X	X	X	X	X	Slave mode operation, Regulation from another *iso*Power part.
L	L	L	X	0V	X	X	Low power mode, Converter disabled
X	X	X	X	X	H	H	Data outputs valid for any active power configuration.
X	X	X	X	X	L	L	Data outputs valid for any active power configuration
H	L	X	X	X	X	X	**WARNING!** This combination of RC_{IN} and RC_{SEL} is prohibited. Damage will occur on the secondary due to exess output voltage at V_{ISO}. RCin must be either Low or a PWM signal from a master *iso*Power part..

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

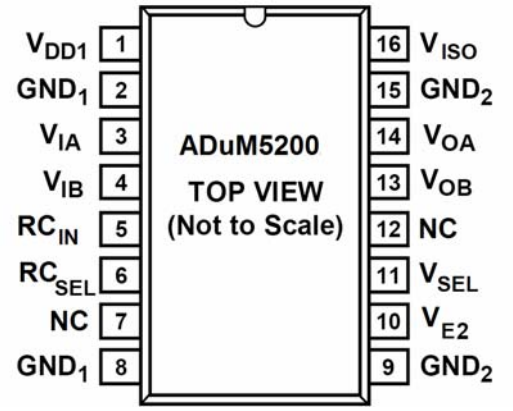


Figure 3. ADuM5200 Pin Configuration

Table 12. ADuM5200 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage 3.0V to 5.5 V.
2,8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	RC_{IN}	Regulation Control Input, In slave power configuration (RC_{SEL}=Low), this pin is connected to the RC_{OUT} of a master isoPower device, or tied low to disable the converter. In Master/Stand alone mode(RC_{SEL}=High) this pin has no function. This pin is weakly pulled to low. In Noisy environments it should be tied to low or to a PWM control source. **Warning** -This pin must not be tied high if RC_{SEL} is low, this combination will cause excessive volatge on the secondary, damaging the ADuM5000 and possibly devices that it powers.
6	RC_{SEL}	Control input, Determines self regulation (CTL High) mode or Slave mode(CTL Low)allowing external regulation. This pin is weakly pulled to high. In noisy environments it should be tied either high or low.
7	NC	No Internal Connection
9,15	GND_{ISO}	Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and it is recommended that both pins be connected to a common ground.
10	V_{E2}	Data Enable Input, When High or NC the Secondary outputs are active, when Low the outputs are in a high Z state..
11	V_{SEL}	Output Voltage Selection: When V_{SEL} = V_{ISO} then the Viso set point is 5.0V, When V_{SEL} = GND_{ISO} Then the VISO setpoint is 3.3V. In Slave regulation mode, this pin has no function.
12	NC	No Internal Connection.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage Output for Secondary Isolaton electronics and External Loads, 3.3V (VSEL Low) or 5.0V (V_{SEL} High), 5.0V output Functioanlity not guaranteed for a 3.3V primary supply input.

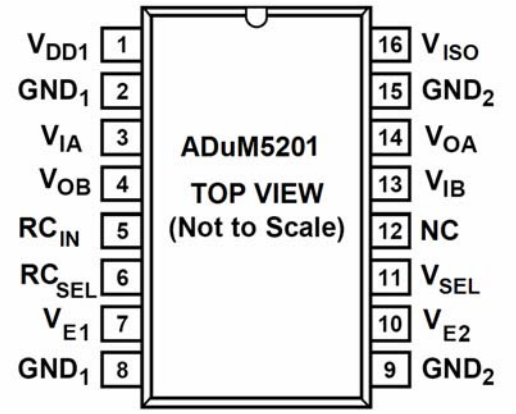


Figure 4. ADuM5201 Pin Configuration

Table 13. ADuM5201 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage 3.0V to 5.5 V.
2,8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{OB}	Logic Output B.
5	RC_{IN}	Regulation Control Input, In slave power configuration (RC_{SEL}=Low), this pin is connected to the RC_{OUT} of a master isoPower device, or tied low to disable the converter. In Master/Stand alone mode(RC_{SEL}=High) this pin has no function. This pin is weakly pulled to low. In Noisy environments it should be tied to low or to a PWM control source. **Warning** -This pin must not be tied high if RC_{SEL} is low, this combination will cause excessive volatge on the secondary, damaging the ADuM5000 and possibly devices that it powers.
6	RC_{SEL}	Control input, Determines self regulation (CTL High) mode or Slave mode(CTL Low)allowing external regulation. This pin is weakly pulled to high. In noisy environments it should be tied either high or low.
7	V_{E1}	Data Enable Input, When High or NC the Primary output is active, when Low the outputs are in a high Z state..
9,15	GND_{ISO}	Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and it is recommended that both pins be connected to a common ground.
10	V_{E2}	Data Enable Input, When High or NC the Secondary output is active, when Low the outputs are in a high Z state..
11	V_{SEL}	Output Voltage Selection: When $V_{SEL} = V_{ISO}$ then the Viso set point is 5.0V, When $V_{SEL} = GND_{ISO}$ Then the VISO setpoint is 3.3V. In Slave regulation mode, this pin has no function.
12	NC	No Internal Connection.
13	V_{IB}	Logic Input B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage Output for Secondary Isolaton electronics and External Loads, 3.3V (VSEL Low) or 5.0V (V_{SEL} High), 5.0V output Functioanlity not guaranteed for a 3.3V primary supply input.

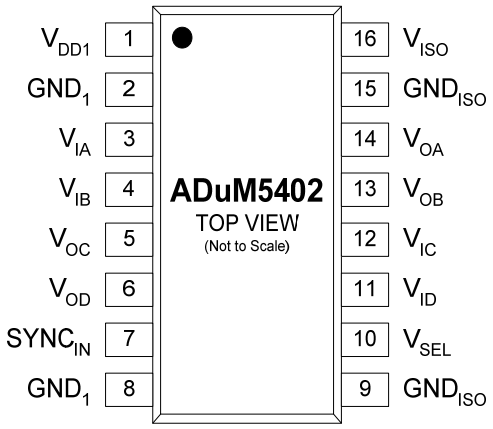


Figure 5. ADuM5202 Pin Configuration

Table 14. ADuM5202 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage 3.0V to 5.5 V.
2,8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected, and it is recommended that both pins be connected to a common ground.
3	V_{OA}	Logic Output A.
4	V_{OB}	Logic Output B.
5	RC_{IN}	Regulation Control Input, In slave power configuration (RC_{SEL}=Low), this pin is connected to the RC_{OUT} of a master isoPower device, or tied low to disable the converter. In Master/Stand alone mode(RC_{SEL}=High) this pin has no function. This pin is weakly pulled to low. In Noisy environments it should be tied to low or to a PWM control source. **Warning** -This pin must not be tied high if RC_{SEL} is low, this combination will cause excessive volatge on the secondary, damaging the ADuM5000 and possibly devices that it powers.
6	RC_{SEL}	Control input, Determines self regulation (CTL High) mode or Slave mode(CTL Low)allowing external regulation. This pin is weakly pulled to high. In noisy environments it should be tied either high or low.
7	V_{E1}	Data Enable Input, When High or NC the Primary output is active, when Low the outputs are in a high Z state..
9,15	GND_{ISO}	Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and it is recommended that both pins be connected to a common ground.
10	NC	No Internal Connection
11	V_{SEL}	Output Voltage Selection: When V_{SEL} = V_{ISO} then the Viso set point is 5.0V, When V_{SEL} = GND_{ISO} Then the VISO setpoint is 3.3V..
12	NC	No Internal Connection.
13	V_{IB}	Logic Input B.
14	V_{OA}	Logic Input A.
16	V_{ISO}	Secondary Supply Voltage Output for Secondary Isolaton electronics and External Loads, 3.3V (VSEL Low) or 5.0V (V_{SEL} High), 5.0V output Functioanlity not guaranteed for a 3.3V primary supply input.

TYPICAL PERFORMANCE CHARACTERISTICS

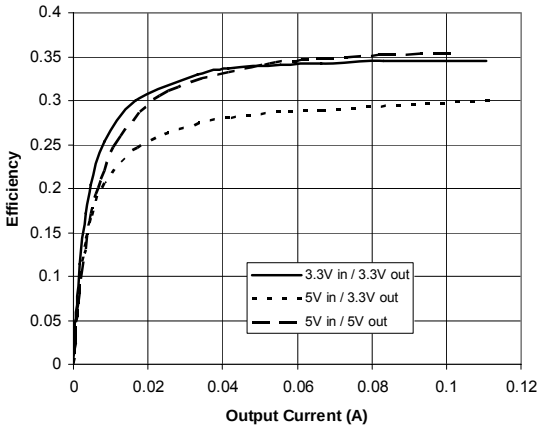


Figure 6. Typical Power Supply Efficiency at 5V/5V, 3.3V/3.3V and 5V/3.3V

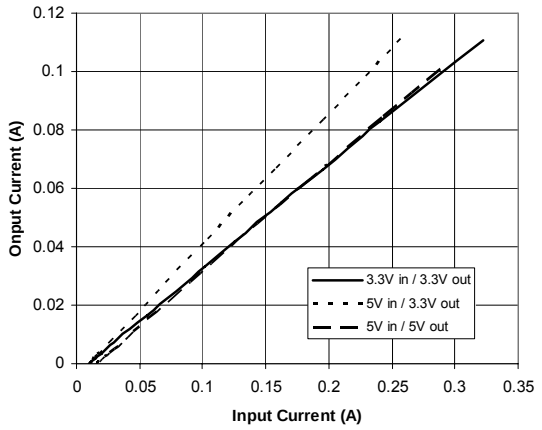


Figure 7. Typical Isolated Output Supply Current, I_{ISO} as a function of external load, no dynamic current draw at 5V/5V, 3.3V/3.3V and 5V/3.3V

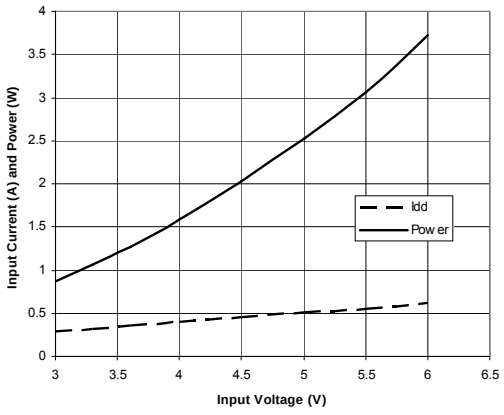


Figure 8. Typical Short Circuit Input Current and Power vs. V_{DD} supply voltage

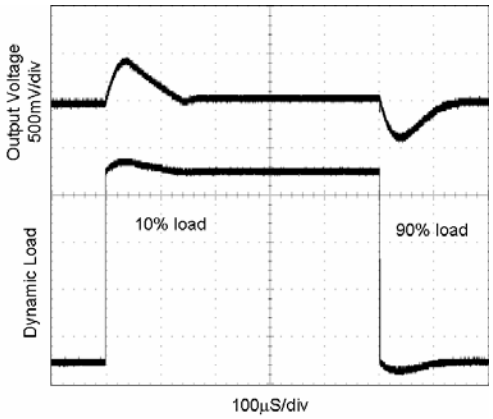


Figure 9. Typical V_{ISO} Transient Load Response 5V Output 10%-90% Load Step

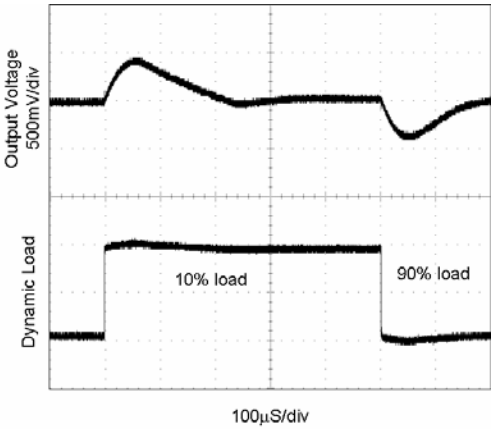


Figure 10. Typical Transient Load Response 3V Output 10%-100% Load Step

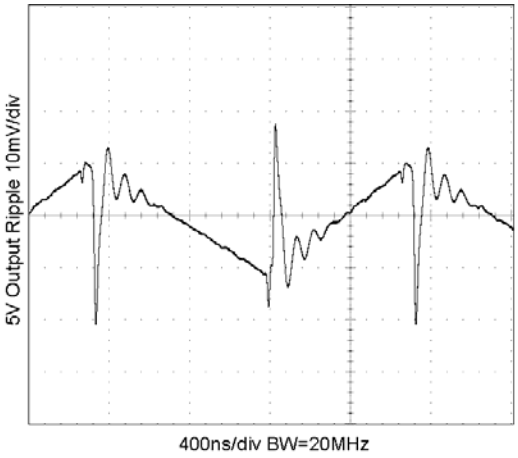


Figure 11. Typical Viso=5V Output Voltage Ripple at 90% Load

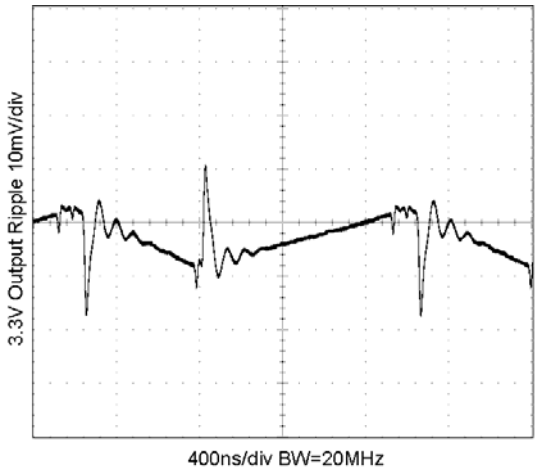


Figure 12. Typical Viso=3.3V Output Voltage Ripple at 90% Load

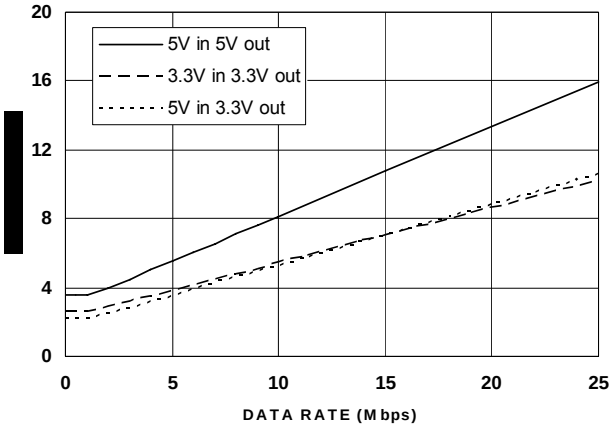


Figure 13. . Typical I_{CH} Supply Current per Forward Data Channel (15 pF Output Load

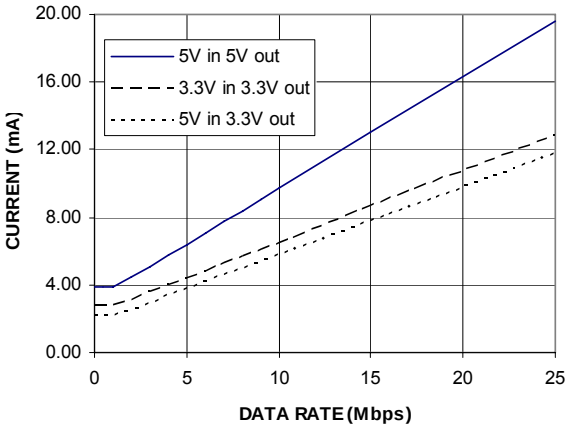


Figure 14 Typical I_{CH} Supply Current per Reverse Data Channel (15 pF Output Load

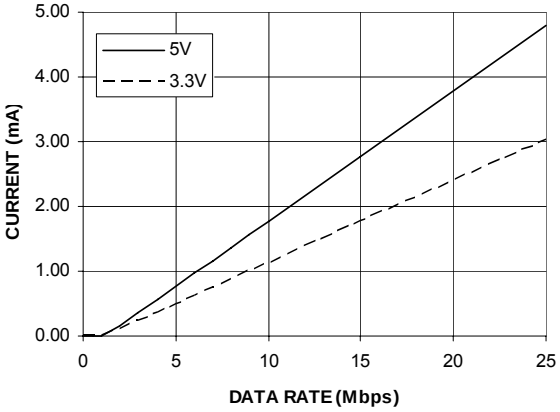


Figure 15. Typical $I_{ISO(D)}$ Dynamic Supply Current per Input

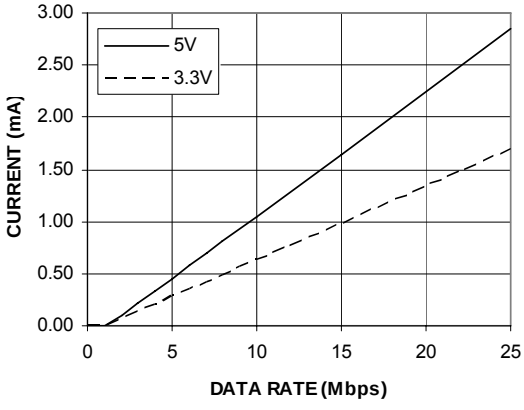


Figure 16. Typical $I_{ISO(D)}$ Dynamic Supply Current per Output (15pF Output Load)

TERMINOLOGY

$I_{DD1(Q)}$
$I_{DD1(Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2 Mbps, requiring no additional dynamic supply current. $I_{DDIO(Q)}$ reflects the minimum current operating condition.

$I_{DD1(D)}$
$I_{DD1(D)}$ is the typical input supply current with all channels simultaneously driven at maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Resistive loads on the outputs should be treated separately from the dynamic load.

$I_{DD1(MAX)}$
$I_{DD1(MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.

t_{PHL} Propagation Delay
t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

t_{PLH} Propagation Delay
t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew (t_{PSK})
t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel-to-Channel Matching
Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

Minimum Pulse Width
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate
The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

APPLICATION INFORMATION

THEORY OF OPERATION

The DC/DC converter section of the ADuM520x works on principles that are common to most modern power supply designs. It is implemented as a secondary side controller with isolated PWM feedback. V_{DD1} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power is transferred to the secondary side where it is rectified to a DC voltage. The power is then regulated to either 3.3or 5V and supplied to the secondary side data section and to the V_{ISO} pin for external use. Active feedback is implemented by a digital feedback path. The output regulator creates a pulse width modulated signal which is coupled to the input side and switches the oscillator on and off regulating the power. Feedback allows for significantly higher power, efficiency, and synchronization of multiple supplies.

The ADuM520x provides its Regulation Control output (RCout) signal that can be connected to other isoPower devices. This allows a single regulator to control multiple power modules without contention. When auxiliary power modules are present, the V_{SIO} pins can be connected together to work as a single supply. Since there is only one feedback control path, the supplies will work together seamlessly. The ADuM520x can only be a source of Regulation Control, other devices

There is hysteresis into the input V_{DD} input voltage detect circuit. Once the DC/DC converter is active, the input voltage must be decreased below the turn on threshold to disable the converter. This feature ensures that the converter does not go into oscillation due to noisy input power.

PC BOARD LAYOUT

The ADuM520x digital isolator with a ½W *iso*Power integrated DC/DC converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (Figure 17). The power supply section of the ADuM520X uses a very high oscillator frequency to efficiently pass power through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins.

Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance high frequency capacitor, ripple suppression and proper regulation require a large value capacitor. These are most conveniently connected between Pins 1 and 2 for V_{DD1} and between Pins 15 and 16 for V_{ISO}. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0. 1 µF, and 6.6µF. It is strongly recommended that a very low inductance ceramic or equivalent capacitor be used for the smaller value.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 4 mm. Installing the bypass capacitor with traces more than 4 mm in length may result in data corruption. A bypass between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless both common ground pins are connected together close to the package.

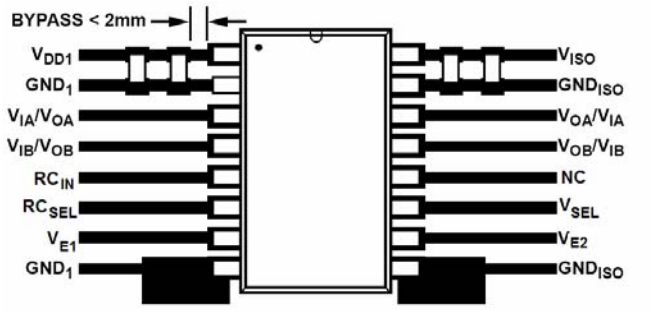


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, specified in Table 9 thereby leading to latch-up and/or permanent damage.

The ADuM520x is a power device that dissipates about 1W of power when fully loaded and running at maximum speed. Since it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device will be used at high ambient temperatures, care should be taken to provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 17 shows enlarged pads for pins 2, 8, 9, and 15. Multiple vias should be implemented from the pad to the ground plane. This will significantly reduce the temperatures inside of the chip. The dimensions of the expanded pads are left to discretion of the designer and the available board space.

THERMAL ANALYSIS

The ADuM520x parts consist of four internal die, attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} from Table 4. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4 layer board with fine width traces and still air. Under normal operating conditions the ADuM520x will operate at full load across the full temperature range without derating the output current. However, following the recommendations in the PC Board Layout section will

decrease the thermal resistance to the PCB allowing increased thermal margin it high ambient temperatures.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

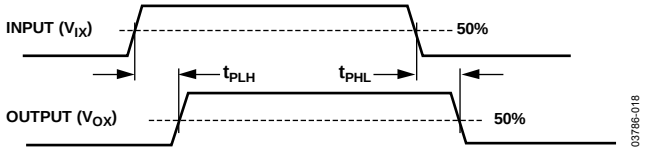


Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM520x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM520x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see **Error! Reference source not found.**) by the watchdog timer circuit.

The limitation on the ADuM520x's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM520x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:

β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM520x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

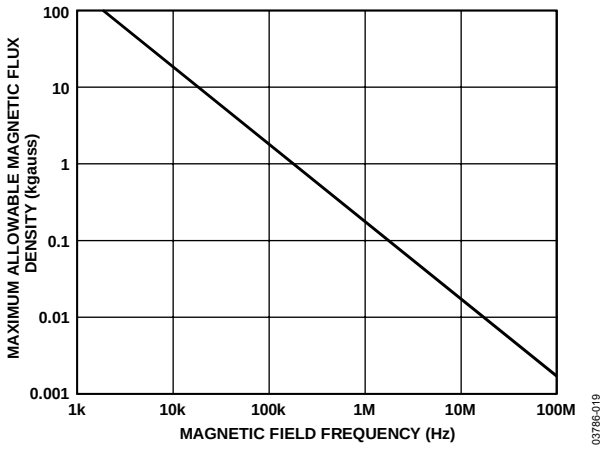


Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM520x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM520x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM520x to affect the component's operation.

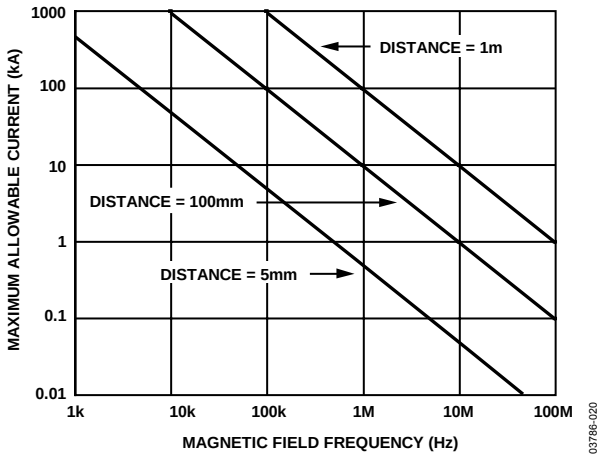


Figure 20. Maximum Allowable Current for Various Current-to-ADuM520x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The V_{DD1} power supply input provides power to the iCoupler data channels as well as the power converter. For this reason, the quiescent currents drawn by the data converter and the primary and secondary I/O channels cannot be determined separately. All of these quiescent power demands have been combined into the $I_{DD1(Q)}$ current as shown in Figure 21. The total I_{DD1} supply current will be the sum of the quiescent operating current, dynamic current $I_{DD1(D)}$ demanded by the I/O channels, and any external I_{ISO} load.

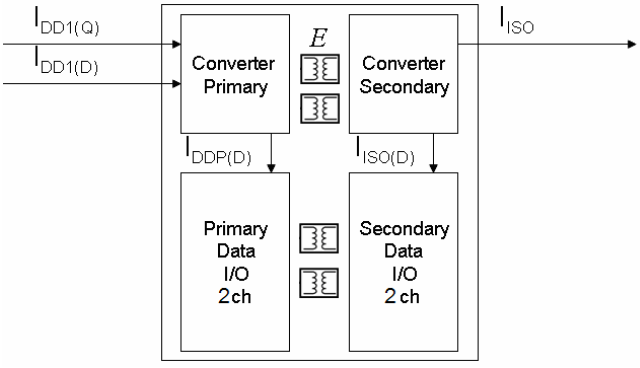


Figure 21 Power consumption within the ADuM520x

Both Dynamic I/O current is consumed only when operating at channel at speeds higher than the rate f_r. Since each channel will have a dynamic current that is determined by its data rate, Figure 15 shows the current for a channel in the forward direction, which means that the input on the primary side of the part. Figure 16 shows the current for a channel in the reverse direction, which means that the input on the secondary side of the part. Both figures assume a typical 15pF load. The following relationship allows the total I_{DD1} current to be calculated.

$$I_{DD1} = (I_{ISO} \times V_{ISO})/(E \times V_{DD1}) + \Sigma I_{CHn}; n = 1to4$$

Equation 1

Where :

I_{DD1} is the total supply input current.

I_{CHn} is the current drawn by a single channel determined from Figure 15 or Figure 16 depending on channel direction.

I_{ISO} is the current drawn by the secondary side external loads.

E is the power supply efficiency at 100mA load from Figure 6 at the V_{ISO} and V_{DD1} condition of interest.

The maximum external load can be calculated by subtracting the dynamic output load from the maximum allowable load.

$$I_{ISO(LOAD)} = I_{ISO(MAX)} - \Sigma I_{ISO(D)n}; n = 1to4$$

Equation 2

Where:

$I_{ISO(LOAD)}$ is the current available to supply an external secondary side load.

$I_{ISO(MAX)}$ is the maximum external secondary side load current available at V_{ISO}.

$I_{ISO(D)n}$ is the dynamic load current drawn from V_{ISO} by an input or output channel, as shown in Figure 15 and Figure 16. Data is presented assuming a typical 15pF load

The preceding analysis assumes a 15pF capacitive load on each data output. If a capacitive load larger than 15pF, he additional current must be included in the analysis of I_{DD1} and $I_{ISO(LOAD)}$.

To determine I_{DD1} in Equation 1, additional primary side dynamic output current I_{AOD} is added directly to I_{DD1}. Additional secondary side dynamic output current I_{AOD} is added to I_{ISO} on a per channel basis.

To determine $I_{ISO(LOAD)}$ in Equation 2, additional secondary side output current I_{AOD} is subtracted from $I_{ISO(MAX)}$ on a per channel basis.

For each output channel with C_L greater than 15pF, the additional capacitive supply current is given by:

$$I_{AOD} = 0.5 \times 10^{-3} \times (C_L\text{-}15) \times V_{ISO}) \times (2f - f_r) \quad f > 0.5\, f_r$$

Equation 3

Where:

C_L is the output load capacitance. (pF).

V_{ISO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

f_r is the input channel refresh rate (Mbps).

POWER CONSIDERATIONS

The ADuM520x Converter Primary side, Data input channels on the Primary side and Data input channels on the Secondary side are all protected from premature operation by Under Voltage Lock Out (UVLO) circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive and all input channel drivers and refresh circuits are idle. Outputs are held in their default low state. This is to prevent transmission of undefined states during power up and power down operations.

During application of power to V_{DD1}, the primary side circuitry is held idle until the UVLO preset voltage is reached. At that time the data channels initialize to their default low output state until they receive data pulses from the secondary side.

The primary side input channels sample the input and send pulse to the inactive secondary output. The secondary side converter begins to accept power from the primary and the V_{ISO} voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data, either a transition or a DC refresh pulse, is received from the corresponding primary side input. It could take up to 1µS after the secondary side is initialized for the state of the output to correlate with the primary side input.

Secondary side inputs sample their state and transmit it to the Primary side. Outputs are valid one propagation delay after the secondary side becomes active.

Because the rate of charge of the secondary side is dependant on loading conditions, input voltage and output voltage level selected, care should be taken in the design to allow the converter to stabilize before valid data is required.

When power is removed from V_{DD1}, the primary side converter and coupler shut down when UVLO is reached. The secondary side stops receiving power and starts to discharge. The outputs on the secondary side will hold the last state that they received from the primary until either the UVLO level is reached and the outputs are put in their default low state or the output detects a lack of activity from the input and the outputs are set to default before secondary power reaches UVLO.

INCREASING AVAILABLE POWER

The ADuM5200 devices are designed with capability of running in combination with other compatible *iso*Power devices. The RC_{IN} and RC_{SEL} pins allow the ADuM5200 to receive a PWM signal from another device through the RC_{IN} pin and act as a slave to that control signal. The RC_{SEL} pin chooses whether the part will act as a stand alone self regulated device or slave device. When the ADuM5200 is acting as a slave, its power is regulated by the master device allowing multiple isoPower parts to be combined in parallel while sharing the load equally. When the ADuM5000 is configured as a Stand alone unit, it generates its own PWM feedback signal to regulate itself and slave devices.

The ADuM5000 can act as a master or a slave deice, the ADuM5400 can only be a master/stand alone device, and the ADuM5200 can only be a slave/Stand alone device. This means that the ADuM5000, ADuM5200, and ADuM5400 can only be used in certain master slave combinations as listed in Table 15.

		Slave		
		ADuM5000	ADuM5200	ADuM5400
Master	ADuM5000	Y	Y	N
	ADuM5200	N	N	N
	ADuM5400	Y	Y	N

Table 15 Allowed combinations of isoPower Parts

The allowed combinations of master and slave configured parts listed in Table 15 is sufficient to make any combination of power and channel count. Table 16 illustrates how isoPower devices can provide many combinations of data channel count and multiples of the single unit power.

	Number of Data Channels			
	0	2	4	6
1 Unit Power	ADuM5000 Master	ADuM520x Master	ADuM540x Master	ADuM540x Master ADuM12xx
2 Unit Power	ADuM5000 Master ADuM5000 Slave	ADuM500x Master ADuM5200 Slave	ADuM540x Master ADuM5200 Slave	ADuM540x Master ADuM520x Slave
3 Unit Power	ADuM5000 Master ADuM5000 Slave ADuM5000 Slave	ADuM5000 Master ADuM5000 Slave ADuM520x Slave	ADuM540x Master ADuM5000 Slave ADuM5000 Slave	ADuM540x Master ADuM520x Slave ADuM5000 Slave

Table 16 Configurations for Power and Data Channels

INSULATION LIFETIME

All insulation structures will eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependant on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM520x.

ADI performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors

for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM520x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 22, Figure 23, and Figure 24 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines ADI's recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50 year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross insulation voltage waveform that does not conform to Figure 23[1] or Figure 24 should be treated as a bipolar ac waveform and its peak voltage should be limited to the 50 year lifetime voltage value listed in Table 10.

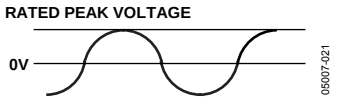


Figure 22. Bipolar AC Waveform

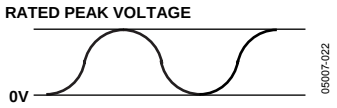


Figure 23. Unipolar AC Waveform

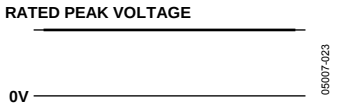
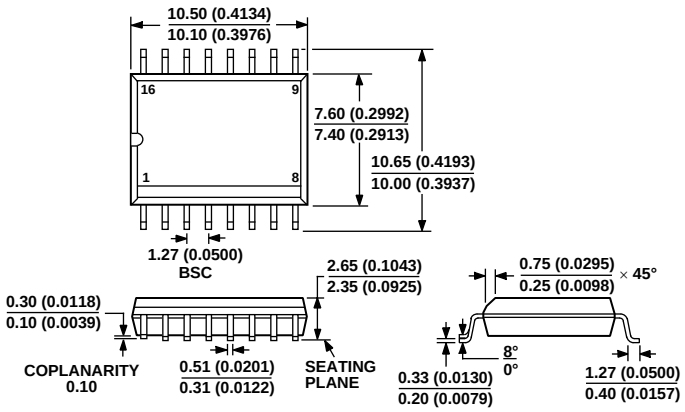


Figure 24. DC Waveform

[1] The voltage presented in Figure 23 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0V.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimension shown in millimeters and (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range (°C)	Package Option
ADuM5200ARWZ[1,2]	2	0	1	100	40	−40 to +105	16-Lead SOIC_W
ADuM5200CRWZ[1,2]	2	0	25	70	3	−40 to +105	16-Lead SOIC_W
ADuM5201ARWZ[1,2]	1	1	1	100	40	−40 to +105	16-Lead SOIC_W
ADuM5201CRWZ[1,2]	1	1	25	70	3	−40 to +105	16-Lead SOIC_W
ADuM5202ARWZ[1,2]	0	2	1	100	40	−40 to +105	16-Lead SOIC_W
ADuM5202CRWZ[1,2]	0	2	25	70	3	−40 to +105	16-Lead SOIC_W

[1] Tape and reel are available. The additional "-RL7" suffice designates a 7" (1,000 units) tape and reel options.
[2] Z = Pb-free part.