PIC24F04KA201 Family Silicon Errata and Data Sheet Clarification

The PIC24F04KA201 family devices that you have received conform functionally to the current Device Data Sheet (DS39937**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F04KA201 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device* and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F04KA201 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
PIC24F04KA201	0B00h	01h
PIC24F04KA200	0B02h	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FXXKAXXX Flash Programming Specification"* (DS39919) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
Resets	BOR	1.	Inadvertent Reset when disabling/enabling BOR.	X
Core	Deep Sleep	2.	Failure to avoid Deep Sleep entry.	X
Comparator	—	3.	Change in maximum VIOFF.	X
SPI	Enhanced Buffer mode	4.	Errors when polling SPITBF flag.	X
Core	Low-Voltage BOR	5.	LPBOR configuration results in ambiguous Resets.	X
Comparator	I/O Pins	6.	Enabling comparators disables some digital I/O ports.	X
Comparator	—	7.	Output polarity inversion also inverts edge-detect sensing.	X
Core	Doze mode	8.	Instruction execution glitches following DOZE bit changes.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Resets (BOR)

A device Reset may occur if the BOR is disabled and immediately re-enabled in software (RCON<14> is cleared, and then immediately set).

Work around

It is recommended that several NOP instructions be added to a BOR disable/enable sequence. Alternatively, place several instructions or a short routine between the instructions to disable and enable the BOR.

Affected Silicon Revisions

A1							
X							

2. Module: Core (Deep Sleep)

Deep Sleep wake-up sources may be ignored if they occur just prior to entry into Deep Sleep mode. As a result, the device may enter Deep Sleep mode when it should not.

Work around

If possible, configure external Deep Sleep wake-up sources to repeat themselves once. If the device does enter Deep Sleep, the second occurrence of the wake-up source will wake the device.

Alternatively, synchronize the entry into Deep Sleep with external wake-up sources, where possible.

Affected Silicon Revisions

A1							
X							

3. Module: Comparator

The maximum value for the input offset voltage (specification D300, VIOFF), shown in Table 26-12 of the Device Data Sheet, has changed for this silicon revision. The new value is shown in Table 3 (changes in **bold**).

Work around

None.

Affected Silicon Revisions

A1							
X							

TABLE 3: COMPARATOR DC SPECIFICATIONS (PARTIAL)

Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	VIOFF	Input Offset Voltage	—	20	**60**	mV	

4. Module: SPI (Enhanced Buffer Mode)

In Enhanced Buffer mode (SPI1CON2<0> = 1), polling the SPI Transmit Buffer Full bit, SPITBF (SPI1STAT<1>), may produce erroneous results. This occurs only under two circumstances:

- In Master mode, when the SPI divide clock is 4 or greater.
- In Slave mode, when the SPI sample clock is slower than 1/4 of the CPU instruction time (TCY).

For Master mode, this includes all combinations of the primary prescale bits (SPI11CON1<1:0>) and secondary prescale bits (SPI1CON1<4:2>) that, when combined, create an SPI sample clock divisor with a value of four or greater.

Work around

Instead of polling the SPITBF bit to test for an empty buffer (SPI1STAT<1> = 0), implement a SPI receive interrupt handler in software and add to the SPI transmit buffer in this routine.

Alternatively, poll the SPI Receive Full bit, SPIRBF (SPI1STAT<0>), or the Shift Register Empty bit, SRMPT (SPI1STAT<7>), to determine when to service the SPI transmit and transmit buffers.

Affected Silicon Revisions

A1							
X							

5. Module: Core (Low-Power BOR)

When the low-power BOR is enabled (FPOR<6:5> = 00), Brown-out Reset events may result in a device Reset in which both the BOR and POR bits are set.

This differs from the expected behavior of simply re-arming the POR circuit to ensure that a Power-on Reset occurs when VDD drops below the POR threshold.

Work around

None.

Affected Silicon Revisions

A1							
X							

6. Module: Comparator (I/O Pins)

Certain I/O pins may not function correctly as digital inputs or outputs after specific comparator outputs have been enabled with the COE bit (CMxCON<14> = 1). These are:

- RB14 (with Comparator 1)
- RA6 (with Comparator 2)

This condition may continue, even after the comparator in question has been disabled using the corresponding CON bit (CMxCON<15> = 0).

Work around

In addition to clearing the CON bit, also clear the COE bit.

Affected Silicon Revisions

A1							
X							

7. Module: Comparator

When a comparator is programmed to trigger on certain edge-detect events (CMxCON<7:6> = 10 or 01), setting the CPOL bit (CMxCON<13> = 1) may cause the comparator to flag the opposite edge-detect event (e.g., a high-to-low edge instead of the programmed low-to-high).

Work around

Leave CPOL = 0. In addition, use the opposite setting of CMxCON<7:6> to achieve the correct response (e.g., use '10' for '01').

Affected Silicon Revisions

A1							
X							

8. Module: Core (Doze Mode)

Operations that immediately follow any manipulations of the DOZE<2:0> or DOZEN bits (CLDIV<14:11>) may not execute properly. In particular, for instructions that operate on an SFR, data may not be read properly. Also, bits automatically cleared in hardware may not be cleared if the operation occurs during this interval.

Work around

Always insert a NOP instruction before and after either of the following:

- Enabling or disabling Doze mode by setting or clearing the DOZEN bit
- Before or after changing the DOZE<2:0> bits

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (DS39937**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications (DC Specifications)

Table 26-5 (“BOR Trip Points”) has changed to reflect the functionality of the LPBOR trip point (BORV<1:0> = 00), and to make other typographic corrections. The minimum and maximum values for the BOR trip points in Table 26-5 have changed. The new version of the table is shown below (changes in **bold**).

TABLE 26-5: BOR TRIP POINTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC19		BOR Voltage on VDD Transition	BOR**V** = 00	—	—	—	—	**Note (1)**
			BOR**V** = 01	2.92	3	3.25	V	
			BOR**V** = 10	2.63	2.7	2.92	V	
			BOR**V** = 11	1.75	1.82	2.01	V	

Note 1: LPBOR re-arms the POR circuit, but does not cause a BOR.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision A1. Includes silicon issues 1 (Resets – BOR), 2 (Core – Deep Sleep), 3 (Comparator) and 4 (SPI – Enhanced Buffer Mode).

Rev B Document (2/2011)

Adds new silicon issues 5 (Core – Low Power BOR), 6 and 7 (Comparators), and 8 (Core – Doze Mode) to silicon revision A1.

Added data sheet clarification 1 (Electrical Specifications – DC Specifications) to revision B of the data sheet.

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