1.5 GHz Low Noise Silicon MMIC Amplifier

Technical Data

INA-52063

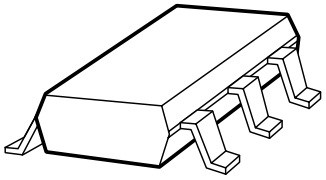
Features

- **Ultra-Miniature Package**
- **Single 5 V Supply (30 mA)**
- **22 dB Gain**
- **8 dBm P_{1dB}**
- **Unconditionally Stable**

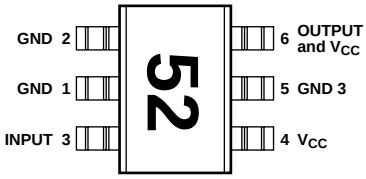
Applications

- **Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, Wireless LAN, DBS, TVRO, and TV Tuner Applications**

Surface Mount SOT-363 (SC-70) Package



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

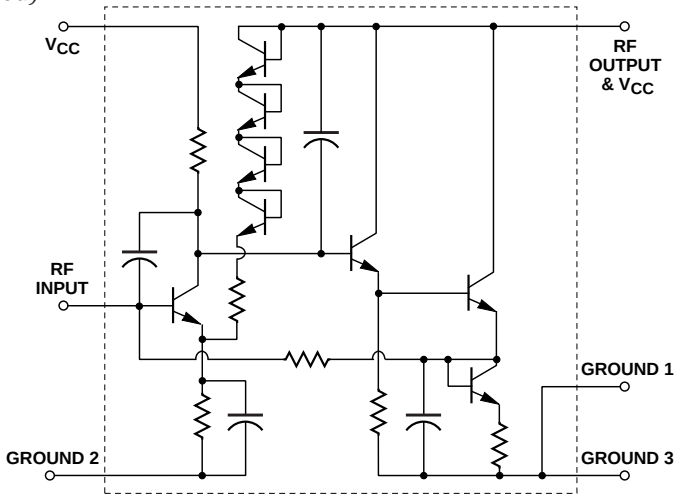
Description

Hewlett-Packard's INA-52063 is a Silicon monolithic amplifier that offers excellent gain and power output for applications to 1.5 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The INA-52063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment sub-micrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

Equivalent Circuit

(Simplified)



Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{CC}	Supply Voltage, to Ground	V	12
P_{in}	CW RF Input Power	dBm	+13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j-c} = 170°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board)

INA-52063 Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5$ V, unless noted

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_p	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz	dB	20	22	
NF	Noise Figure	f = 900 MHz	dB		4.0	
P_{1dB}	Output Power at 1 dB Gain Compression	f = 900 MHz	dBm		+8	
IP_3	Third Order Intercept Point	f = 900 MHz	dBm		+20	
IP_3	Third Order Intercept Point	f = 2100 MHz	dBm		+15	
VSWR	Input VSWR	f = 900 MHz			1.4	
	Output VSWR	f = 900 MHz			1.3	
I_{CC}	Device Current		mA		30	38
ι_d	Group Delay	f = 900 MHz	ps		238	

INA-52063 Typical Performance, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_{CC} = 5$ V, unless noted

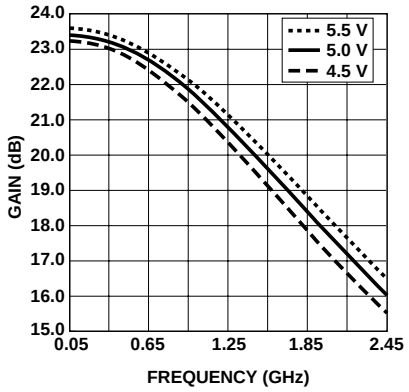


Figure 1. Gain vs. Frequency and Voltage.

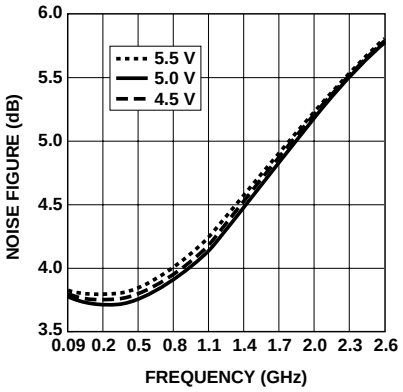


Figure 2. Noise Figure vs. Frequency and Voltage.

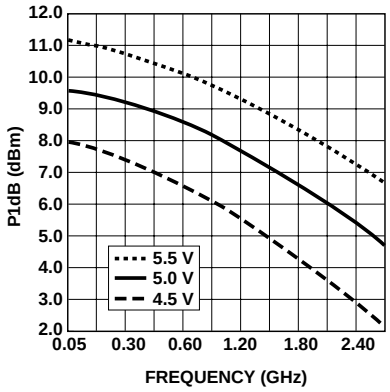


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

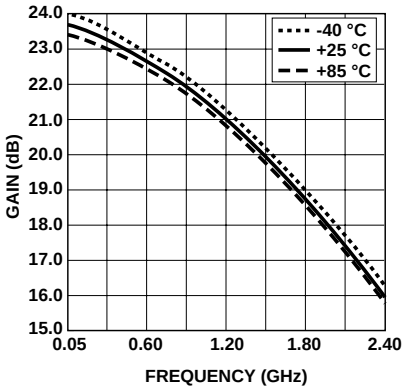


Figure 4. Gain vs. Frequency and Temperature.

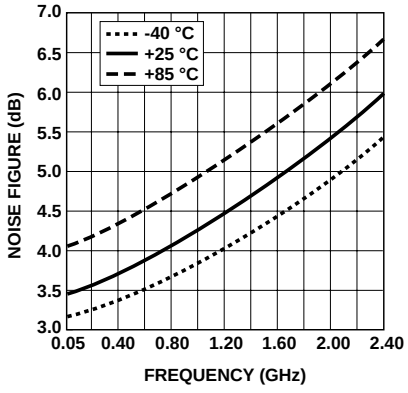


Figure 5. Noise Figure vs. Frequency and Temperature.

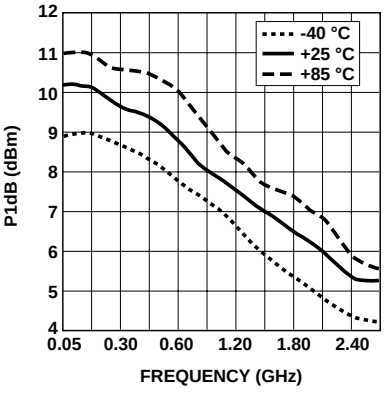


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

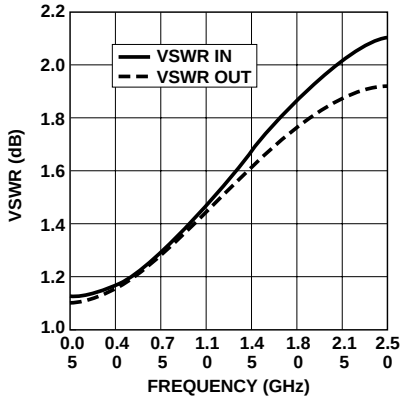


Figure 7. Input and Output VSWR vs. Frequency.

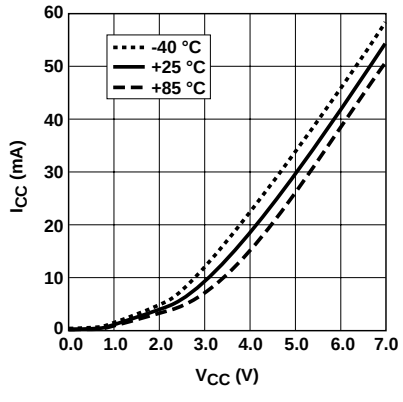


Figure 8. Supply Current vs. Voltage and Temperature.

INA-52063 Typical Scattering Parameters[3], $T_C = 25°C$, $Z_O = 50\,\Omega$, $V_{CC} = 5.0\,V$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.05	0.06	165	23.5	14.88	-5	-29.3	0.034	0	0.05	1	1.24
0.10	0.06	154	23.4	14.84	-9	-29.3	0.034	0	0.05	0	1.24
0.20	0.06	131	23.4	14.72	-19	-29.4	0.034	0	0.05	-1	1.25
0.30	0.07	104	23.3	14.57	-28	-29.5	0.034	1	0.06	-5	1.25
0.40	0.07	80	23.1	14.33	-37	-29.4	0.034	2	0.07	-10	1.26
0.50	0.09	66	23.0	14.08	-46	-29.4	0.034	3	0.08	-14	1.27
0.60	0.10	46	22.8	13.76	-55	-29.4	0.034	4	0.09	-21	1.28
0.70	0.12	30	22.6	13.41	-64	-29.3	0.034	5	0.11	-29	1.29
0.80	0.13	14	22.3	13.01	-73	-29.2	0.035	6	0.13	-37	1.28
0.90	0.15	0	22.0	12.59	-82	-29.0	0.036	6	0.14	-45	1.27
1.00	0.17	-12	21.7	12.14	-90	-28.8	0.036	7	0.16	-52	1.28
1.20	0.21	-33	21.0	11.22	-106	-28.4	0.038	7	0.20	-67	1.25
1.40	0.24	-50	20.2	10.28	-122	-28.1	0.040	6	0.23	-81	1.24
1.60	0.27	-66	19.4	9.38	-137	-27.7	0.041	4	0.25	-94	1.26
1.80	0.30	-80	18.6	8.55	-151	-27.5	0.042	2	0.27	-107	1.29
2.00	0.32	-93	17.8	7.80	-164	-27.4	0.043	-1	0.29	-118	1.33
2.20	0.33	-105	17.1	7.13	-177	-27.6	0.042	-5	0.30	-129	1.44
2.40	0.35	-117	16.3	6.52	170	-27.8	0.041	-8	0.31	-139	1.56
2.60	0.36	-128	15.5	5.98	159	-28.1	0.039	-12	0.32	-149	1.74
2.80	0.36	-139	14.8	5.52	147	-28.9	0.036	-15	0.33	-158	2.01
3.00	0.36	-149	14.1	5.08	136	-29.5	0.033	-16	0.33	-168	2.37

Note: 3. Reference plane per Figure 9 in Applications Information section.

INA-52063 Applications Information

Introduction

The INA-52063 is a silicon RFIC amplifier that is designed with an internal resistive feedback network to provide a 50 Ω input and 50 Ω output impedance. With a Third Order Intercept Point of +20 dBm and a low Noise Figure of 4 dB, the INA-52063 is especially useful for RF and IF amplifier applications requiring high dynamic ranges.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters for this device are shown in Figure 9. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

SOT-363 PCB Layout

The INA-52063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 10 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding pad parasitics that could impair the high frequency performance of the INA-52063. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads for reference.

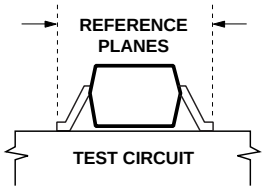


Figure 9. Phase Reference Planes.

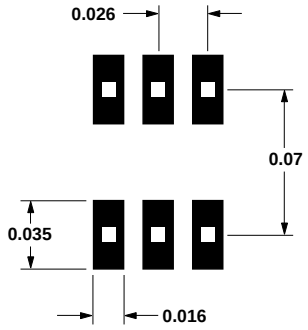


Figure 10. PCB Pad Layout (dimensions in inches).

Operating Details

The INA-52063 is a voltage biased device that operates from a +5 volt power supply with a typical current drain of 30 mA. All bias regulation circuitry is integrated into the RFIC.

Figure 11 shows a typical implementation of the INA-52063. The supply voltage for the INA-52063 must be applied to two terminals, the V_{CC} pin and the RF Output pin.

The V_{CC} connection to the amplifier is RF bypassed by placing a capacitor to ground near the V_{CC} pin of the amplifier package.

The power supply connection to the RF Output pin is achieved by means of a RF choke (inductor). The value of the RF choke must be large relative to 50 Ω in order to prevent loading of the RF Output.

The supply voltage end of the RF choke is bypassed to ground with a capacitor. If the physical layout permits, this can be the same bypass capacitor that is used at the V_{CC} terminal of the amplifier.

Blocking capacitors are normally placed in series with the RF Input and the RF Output to isolate the DC voltages on these pins from circuits adjacent to the amplifier. The values for the blocking and bypass capacitors are selected to provide a reactance at the lowest frequency of operation that is small relative to 50 Ω.

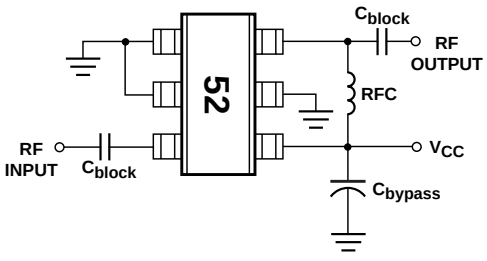


Figure 11. Basic Amplifier Application.

RF Layout

An example layout for an amplifier using the INA-52063 is shown in Figure 12.

This example uses a microstripline design (solid groundplane on the back side of the circuit board). The circuit board material is 0.031-inch thick FR-4. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the path to ground.

Figure 13 shows an assembled amplifier. The +5 volt supply is fed directly into the V_{CC} pin of the INA-52063 and into the RF Output pin through the RF choke (RFC). Capacitor C3 provides RF bypassing for both the V_{CC} pin and the power supply end of the RFC.

Capacitor C4 is optional and may be used to add additional bypassing for the V_{CC} line. A well bypassed V_{CC} line is especially necessary in cascades of amplifier stages to prevent oscillation that may occur as a result of RF feedback through the power supply lines.

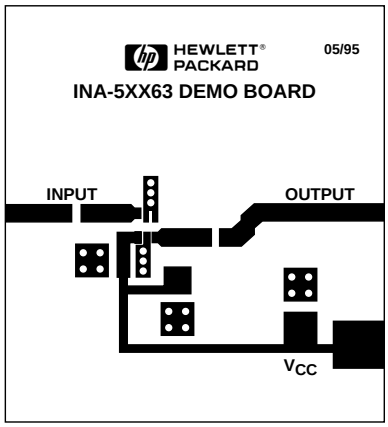


Figure 12. RF Layout.

For this demonstration circuit, the value chosen for the RF choke was 220 nH (Coilcraft 1008CS-221 or equivalent). All of the blocking and bypass capacitors are 1000 pF. These values provide excellent amplifier performance from under 50 MHz through 1 GHz. Larger values for the choke and capacitors can be used to extend the lower end of the bandwidth. Since the gain of the INA-52063 extends down to DC, the frequency response of the amplifier is limited only by the values of the capacitors and choke.

A convenient method for making RF connection to the demonstration board is to use a PCB mounting type of SMA connector (Johanson 142-0701-881, or equivalent). These connectors can be slipped over the edge of the PCB and the center conductors soldered to the input and output lines. The ground pins of the connectors are soldered to the ground plane on the backside of the board. The extra ground pins for the top of the board are not needed and are clipped off.

PCB Materials

Typical choices for PCB material for low cost wireless applications are FR-4 or G-10 with a thickness of 0.025 or 0.031 inches. A thickness of 0.062 inches is the maximum that is recommended for use with this particular device. The use of a thicker board material increases the inductance of the plated through vias used for RF grounding and may deteriorate circuit performance. Adequate grounding is needed not only to obtain maximum amplifier performance but also to reduce any possibility of instability.

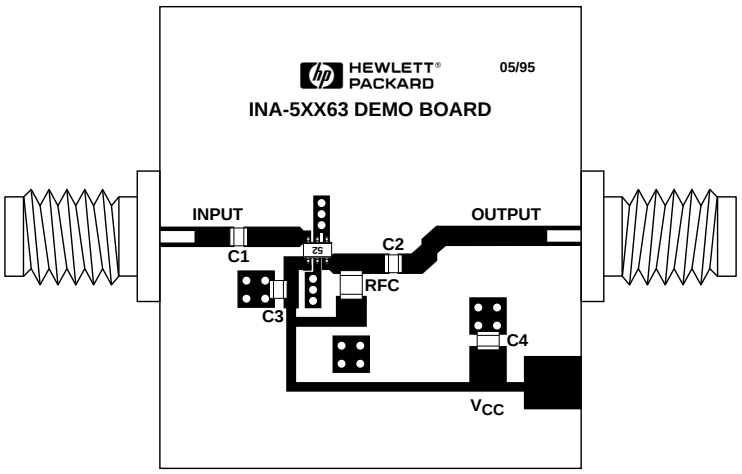
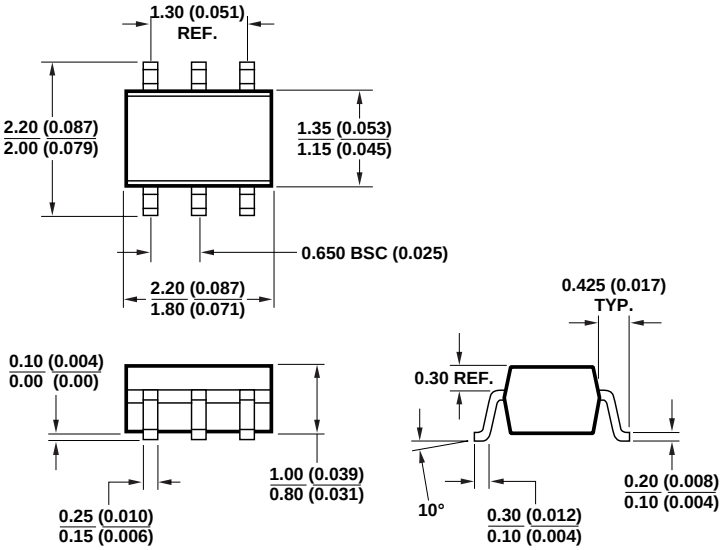


Figure 13. Assembled Amplifier.

Package Dimensions

Outline 63 (SOT-363/SC-70)

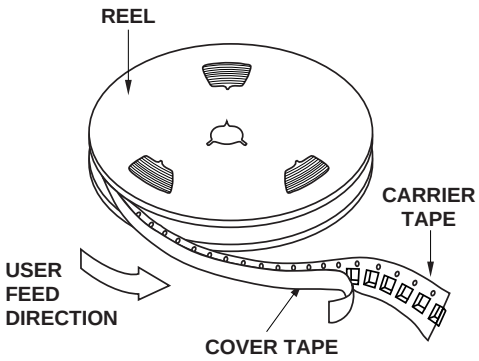


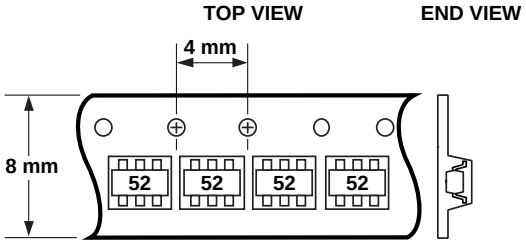
DIMENSIONS ARE IN MILLIMETERS (INCHES)

INA-52063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-52063-TR1	3,000	7" reel
INA-52063-BLK	100	Antistatic bag

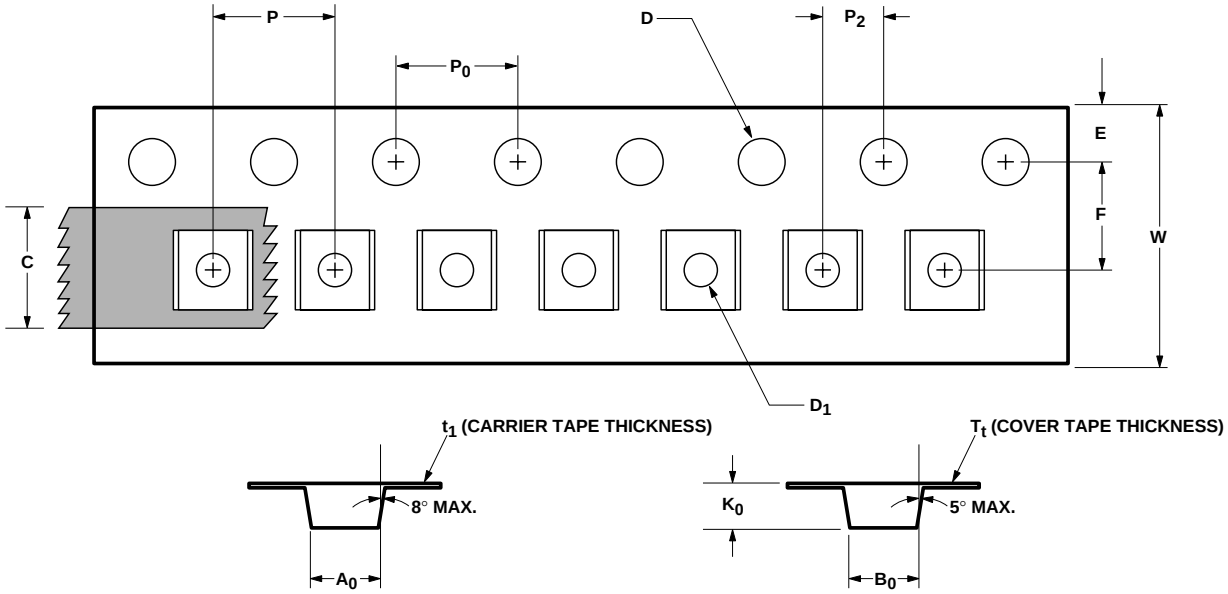
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002