

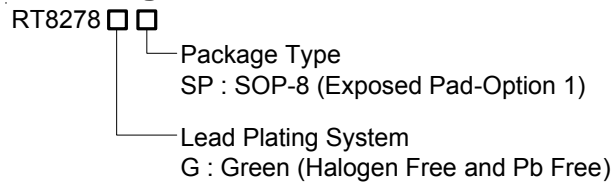
## 2A, 24V, 3MHz Step-Down Converter

### General Description

The RT8278 is a high voltage buck converter that can support an input voltage range from 4.5V to 24V with output current up to 2A. Current mode operation provides fast transient response and eases loop stabilization.

The chip provides protection functions such as cycle-by-cycle current limiting and thermal shutdown protection. In shutdown mode, the regulator only draws 25µA of supply current. The RT8278 is available in a SOP-8 (Exposed Pad) package.

### Ordering Information

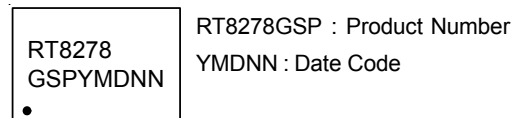


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### Marking Information



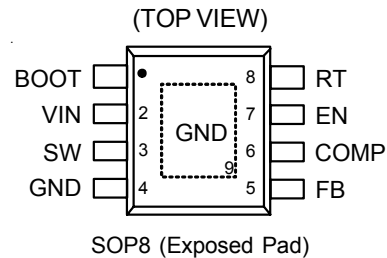
### Features

- Wide Operating Input Range : 4.5V to 24V
- Adjustable Output Voltage Range : 0.8V to 15V
- Output Current up to 2A
- 25µA Low Shutdown Current
- High Efficiency up to 90% at 2.2MHz
- Programmable Frequency : 220kHz to 3MHz
- Internal Soft-Start
- Stable with Low ESR Output Ceramic Capacitors
- Thermal Shutdown Protection
- Cycle-By-Cycle Over Current Protection
- RoHS Compliant and Halogen Free

### Applications

- DSL Modem for ADSL2+ Standard
- Distributed Power Systems
- Pre-Regulator for Linear Regulators

### Pin Configurations



### Typical Application Circuit

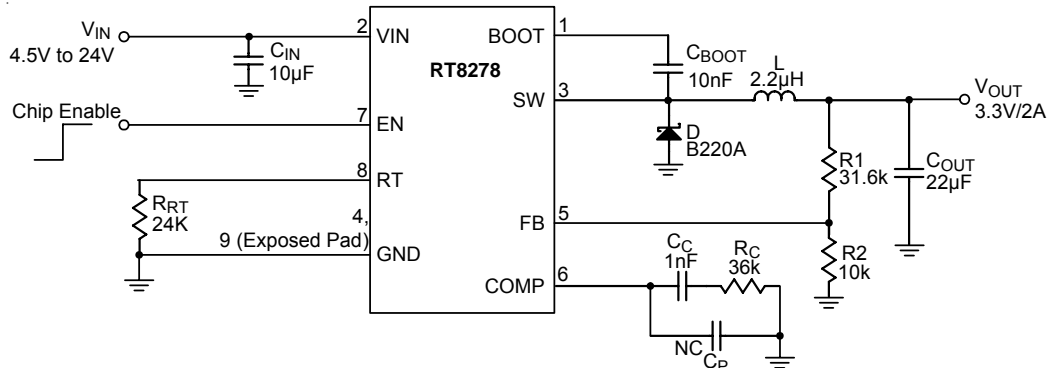


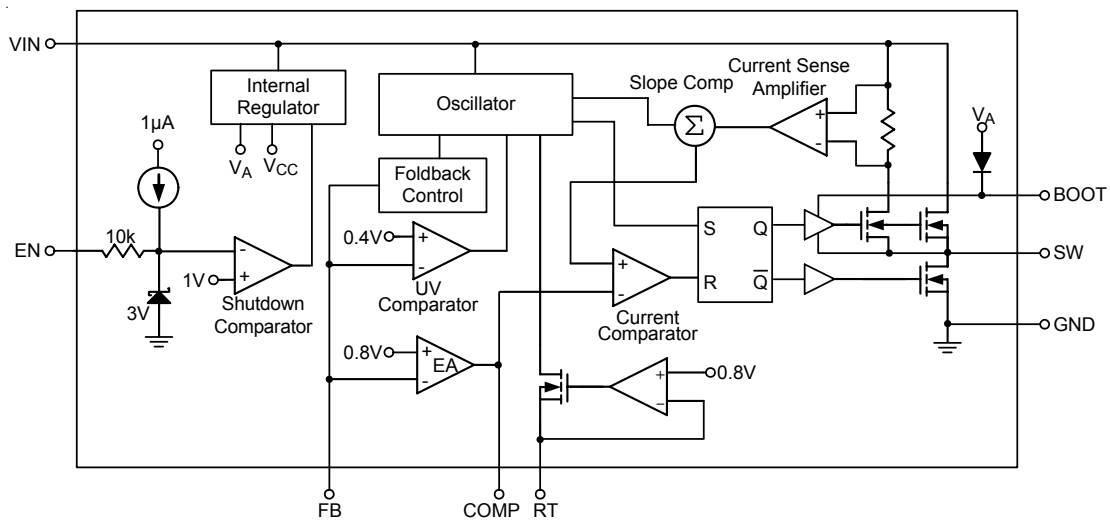
Table 1. Recommended Component Selection for  $f_{sw} = 2.2\text{MHz}$ 

| $V_{OUT}$ (V) | R1 (k $\Omega$ ) | R2 (k $\Omega$ ) | R <sub>C</sub> (k $\Omega$ ) | C <sub>C</sub> (nF) | L ( $\mu$ H) | C <sub>OUT</sub> ( $\mu$ F) |
|---------------|------------------|------------------|------------------------------|---------------------|--------------|-----------------------------|
| 10            | 115              | 10               | 82                           | 0.56                | 8.2          | 22                          |
| 8             | 91               | 10               | 68                           | 0.56                | 6.8          | 22                          |
| 5             | 52.3             | 10               | 56                           | 1.8                 | 4.7          | 22                          |
| 3.3           | 31.6             | 10               | 36                           | 1                   | 2.2          | 22                          |
| 2.5           | 21.5             | 10               | 27                           | 1.2                 | 2            | 22                          |
| 1.8           | 12.4             | 10               | 20                           | 1.8                 | 1.5          | 22                          |
| 1.5           | 8.87             | 10               | 16                           | 3.3                 | 1.5          | 22                          |
| 1.2           | 4.99             | 10               | 24                           | 1                   | 1            | 22                          |

## Functional Pin Description

| Pin No.               | Pin Name | Pin Function  |
|-----------------------|----------|---|
| 1                     | BOOT     | Bootstrap Power Pin. BOOT supplies the drive for the high side N-MOSFET switch. Connect a 10nF or greater capacitor from SW to BOOT to power the high side switch.  |
| 2                     | VIN      | Supply Input. $V_{IN}$ supplies the power to the IC, as well as the step-down converter switches. Drive $V_{IN}$ with a 4.5V to 24V power source. Bypass $V_{IN}$ to GND with a suitably large capacitor to eliminate noise on the input to the IC. |
| 3                     | SW       | Switch Node. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BOOT to power the high side switch.                                  |
| 4,<br>9 (Exposed Pad) | GND      | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.   |
| 5                     | FB       | Feedback Input. FB senses the output voltage to regulate. Drive FB with a resistive voltage divider from the output voltage.  |
| 6                     | COMP     | Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.             |
| 7                     | EN       | Enable Input. EN is a digital input that turns the regulator on or off. Drive EN higher than 1.4V to turn on the regulator, lower than 0.4V to turn off. For automatic startup, leave EN unconnected.   |
| 8                     | RT       | Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.  |

**Function Block Diagram**



**Absolute Maximum Ratings** (Note 1)

- $V_{IN}$  ----- -0.3V to 26V
- SW ----- -0.3V to ( $V_{IN} + 0.3V$ )
- BOOT ----- ( $V_{SW} - 0.3V$ ) to ( $V_{SW} + 6V$ )
- All Other Pins ----- -0.3V to 6V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ C$   
SOP-8 (Exposed Pad) ----- 1.333W
- Package Thermal Resistance (Note 2)  
SOP-8 (Exposed Pad),  $\theta_{JA}$  -----  $75^\circ C/W$   
SOP-8 (Exposed Pad),  $\theta_{JC}$  -----  $28^\circ C/W$
- Lead Temperature (Soldering, 10 sec.) -----  $260^\circ C$
- Junction Temperature -----  $150^\circ C$
- Storage Temperature Range -----  $-65^\circ C$  to  $150^\circ C$
- ESD Susceptibility (Note 3)  
HBM (Human Body Mode) ----- 2kV  
MM (Machine Mode) ----- 200V

**Recommended Operating Conditions** (Note 4)

- Supply Input Voltage,  $V_{IN}$  ----- 4.5V to 24V
- Junction Temperature Range -----  $-40^\circ C$  to  $125^\circ C$
- Ambient Temperature Range -----  $-40^\circ C$  to  $85^\circ C$

**Electrical Characteristics** $(V_{IN} = 12V, T_A = 25^\circ C, \text{ unless otherwise specified})$ 

| Parameter  | Symbol            | Test Conditions                           | Min   | Typ  | Max   | Unit      |
|--|-------------------|---|-------|------|-------|-----------|
| Feedback Reference Voltage   | $V_{FB}$          | $4.5V \leq V_{IN} \leq 24V$               | 0.784 | 0.8  | 0.816 | V         |
| Upper Switch On Resistance   | $R_{DS(ON)1}$     |   | --    | 0.18 | --    | $\Omega$  |
| Lower Switch On Resistance   | $R_{DS(ON)2}$     |   | --    | 10   | --    | $\Omega$  |
| Upper Switch Leakage   | $I_{LEAK}$        | $V_{EN} = 0V, V_{SW} = 0V$                | --    | 0    | 10    | $\mu A$   |
| Current Limit  | $I_{LIM}$         | Duty = 90%,<br>$V_{BOOT} - V_{SW} = 4.8V$ | --    | 3    | --    | A         |
| Current Sense<br>Transconductance<br>Output Current to Comp Pin<br>Voltage | $g_{CS}$          |   | --    | 1.8  | --    | A/V       |
| Error Amplifier<br>Transconductance  | $g_{EA}$          | $\Delta I_C = \pm 10\mu A$                | --    | 920  | --    | $\mu A/V$ |
| Oscillator Frequency   | $f_{SW}$          | $R_{RT} = 24k\Omega$                      | --    | 2.2  | --    | MHz       |
| Short Circuit Frequency  |                   | $V_{FB} = 0V, R_{RT} = 24k\Omega$         | --    | 550  | --    | kHz       |
| Under Voltage Lockout<br>Threshold Rising                                  | $V_{UVLO}$        |   | --    | 4.2  | --    | V         |
| Under Voltage Lockout<br>Threshold Hysteresis                              | $\Delta V_{UVLO}$ |   | --    | 430  | --    | mV        |
| Maximum Duty Cycle   | $D_{MAX}$         | $V_{FB} = 0.7V, R_{RT} = 24k\Omega$       | --    | 65   | --    | %         |
| Minimum On Time  | $t_{ON}$          |   | --    | 70   | --    | ns        |

*To be continued*

| Parameter              |            | Symbol     | Test Conditions            | Min | Typ | Max | Unit        |
|------------------------|------------|------------|----------------------------|-----|-----|-----|-------------|
| EN Threshold Voltage   | Logic-High | $V_{IH}$   |                            | 1.4 | --  | --  | V           |
|                        | Logic-Low  | $V_{IL}$   |                            | --  | --  | 0.4 |             |
| Enable Pull Up Current |            |            |                            | --  | 1   | --  | $\mu A$     |
| Quiescent Current      |            | $I_Q$      | $V_{EN} = 2V, V_{FB} = 1V$ | --  | 0.8 | 1   | mA          |
| Shutdown Current       |            | $I_{SHDN}$ | $V_{EN} = 0V$              | --  | 25  | --  | $\mu A$     |
| Thermal Shutdown       |            |            |                            | --  | 150 | --  | $^{\circ}C$ |

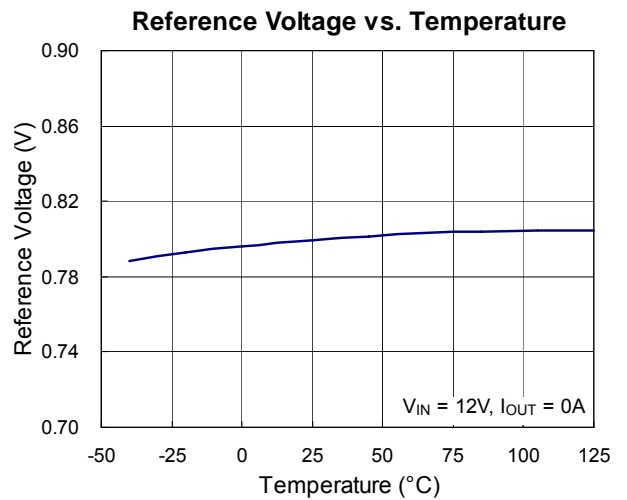
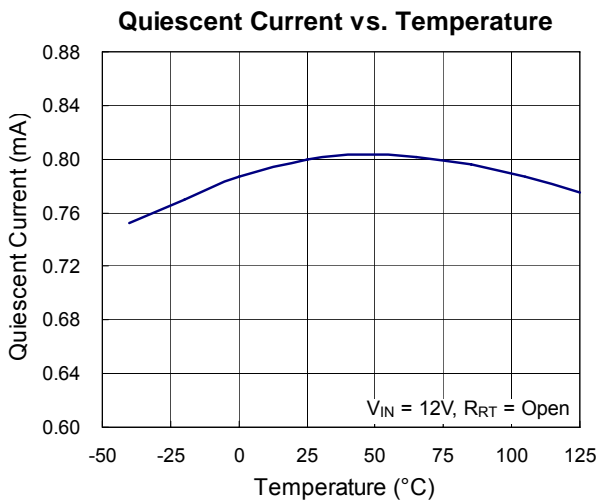
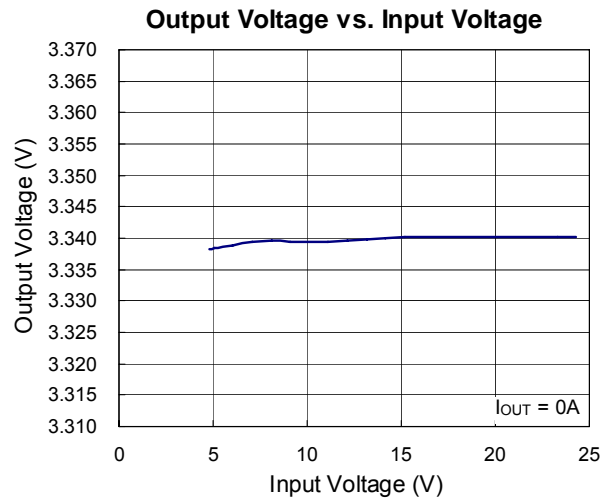
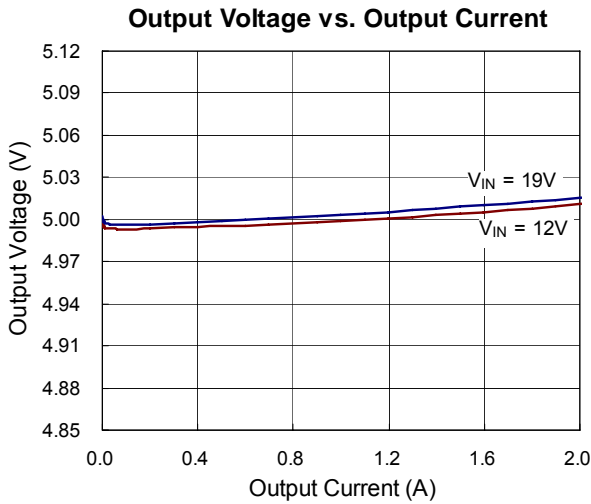
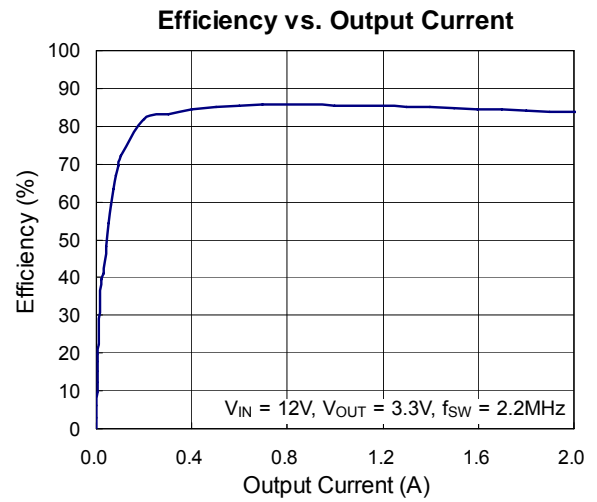
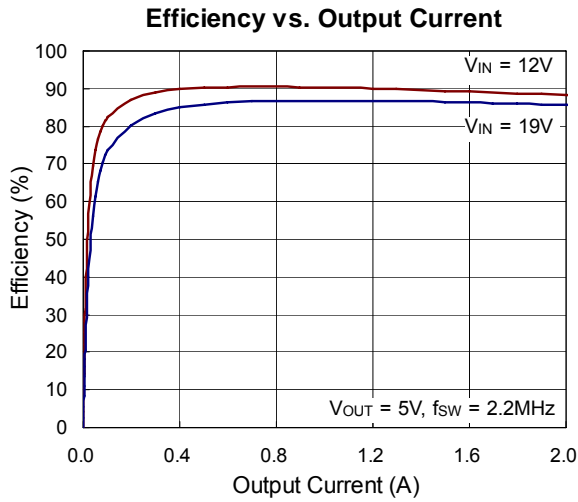
**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

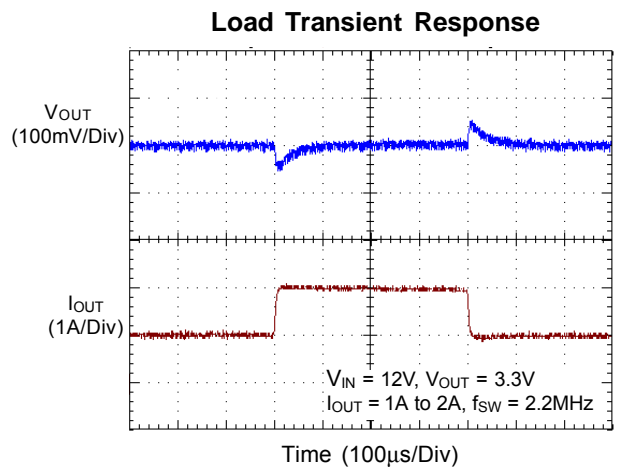
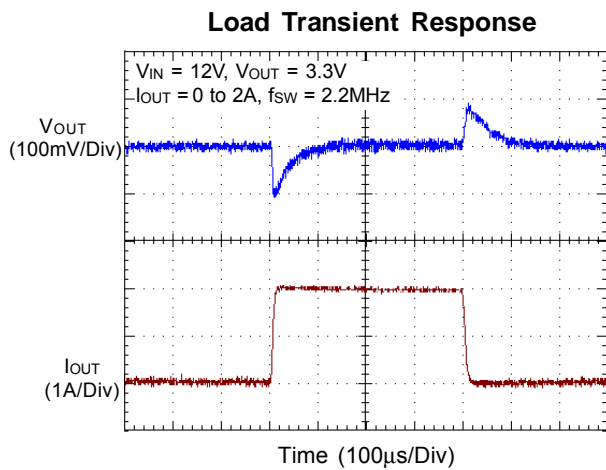
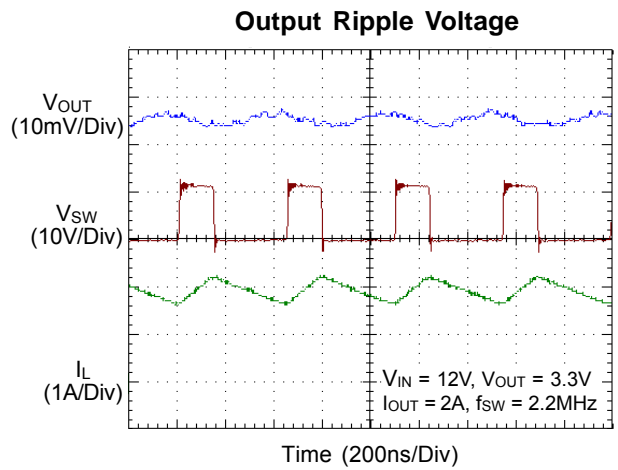
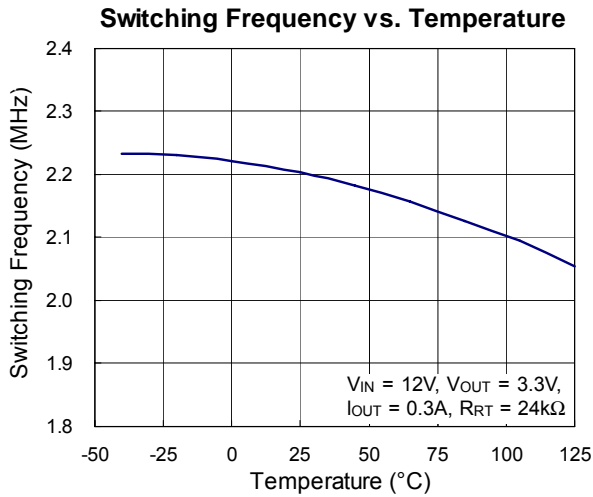
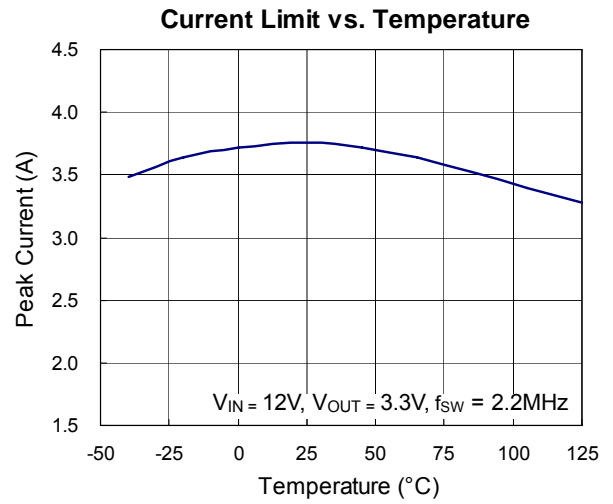
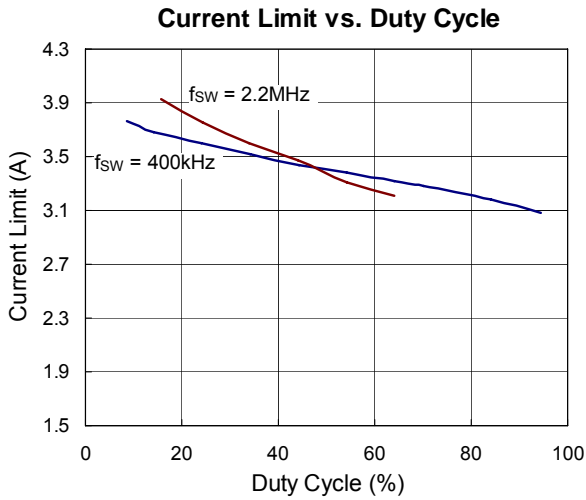
**Note 2.**  $\theta_{JA}$  is measured in natural convection at  $T_A = 25^{\circ}C$  on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of  $\theta_{JC}$  is on the exposed pad of the package.

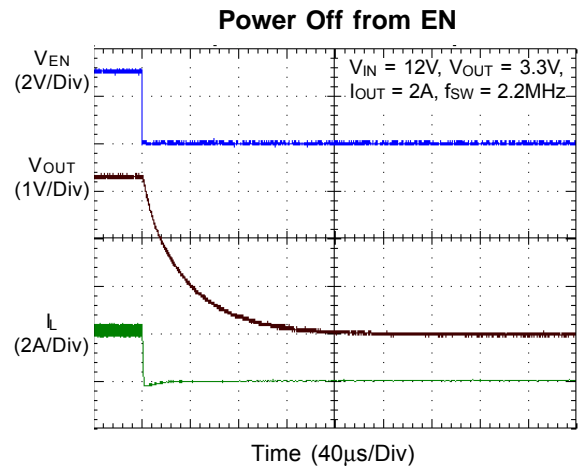
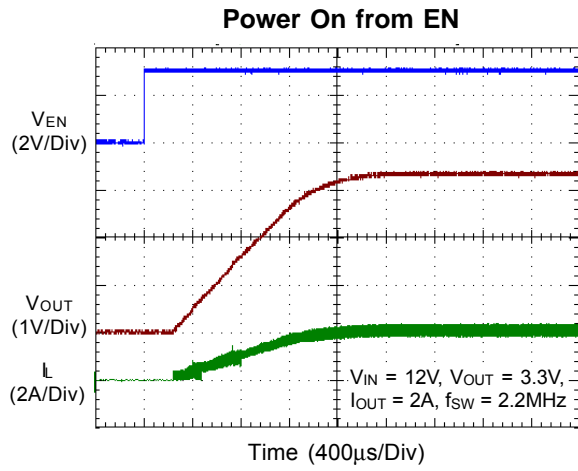
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics









### Application Information

The RT8278 is an asynchronous high voltage buck converter that supports an input voltage range from 4.5V to 24V with output current up to 2A.

#### Output Voltage Setting

The resistive voltage divider allows the FB pin to sense the output voltage as shown in Figure 1.

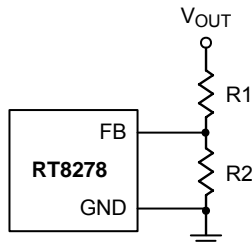


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB} \left( 1 + \frac{R1}{R2} \right)$$

where  $V_{FB}$  is the feedback reference voltage (0.8V typ.).

#### External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V voltage source and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty cycle is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external voltage source must be fixed at 5V and can be provided from the system or the output of the RT8278.

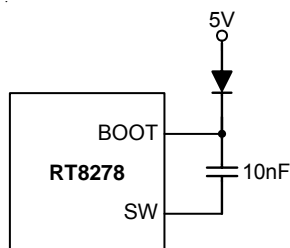


Figure 2. External Bootstrap Diode

#### Operating Frequency

Selection of the operating frequency is a trade off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The operating frequency of the RT8278 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. Selection of the RT resistor value can be determined by examining the curve below in Figure3. Although frequencies as high as 3MHz are available, the minimum on-time of the RT8278 imposes a limit on the operating duty cycle. Figure 4 shows the examples of minimum on-time constraint for output voltages 3.3V and 1.8V. It is recommended to operate the RT8278 in the region under the corresponding Vout curve.

Except the minimum on-time constraint, the limit of maximum duty also needs to be considered. In ideal case, the duty cycle of the RT8278 can be calculated by below equation, But in practical case it will be higher than the calculation result since all the components in a converter circuit are not ideal. Figure 5 shows an example for the limit of maximum duty. With 5V input voltage, the 3.3V output voltage of the RT8278 becomes out of regulation when the output current is increased. However, when the input voltage is changed to 12V, the 3.3V output voltage of the RT8278 remains in regulation even with 2A output current. According to equation below, the duty cycle is 0.67 for the RT8278 operated with 5V input voltage and 3.3V output voltage in 2.2MHz switching frequency. The ideal case duty cycle calculation is already over the limit of maximum duty(65%). Thus, it is obvious that the RT8278 can't support 2A output current in such conditions :

$$\text{Duty Cycle} = 1 - 0.15 \times f_{SW} \quad (\text{MHz})$$

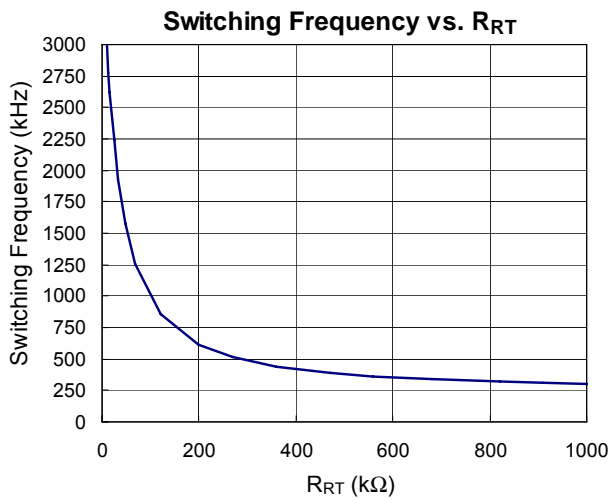


Figure 3. Switching Frequency vs. R<sub>RT</sub>

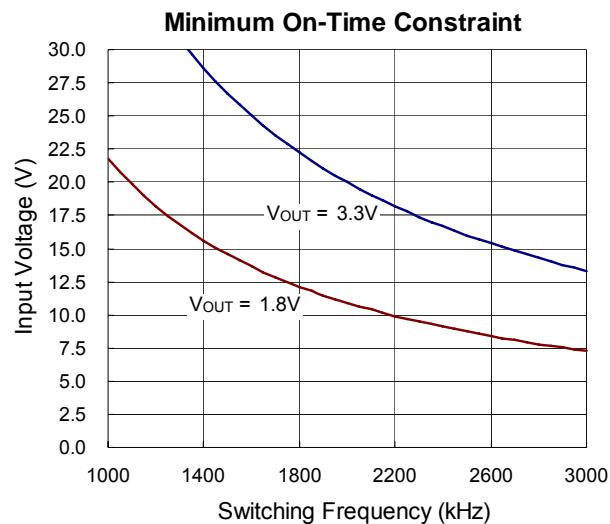


Figure 4. Minimum On-Time Constraint to Input Voltage

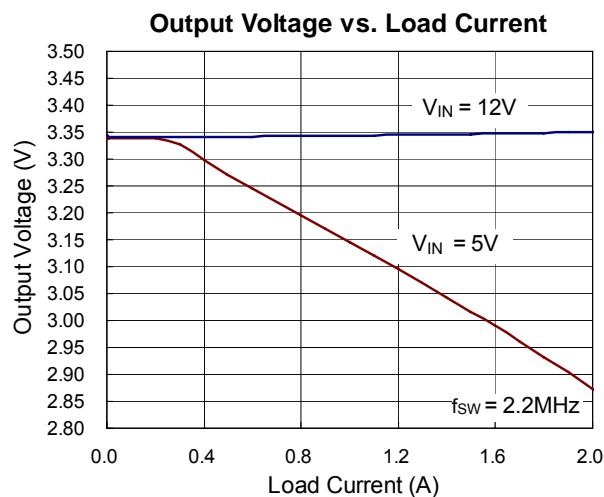


Figure 5. Limit of Maximum Duty

**Chip Enable Operation**

The EN pin is the enable input. Pull the EN pin low (<0.4V) to shutdown the device. During shutdown mode, the RT8278 quiescent current drops to lower than 25µA. Drive the EN pin high (>1.4V, < 5.5V), to turn on the device. If the EN pin is open, it will be pulled high by the internal circuit. For external timing control (e.g.RC), the EN pin can also be externally pulled high by adding a 100kΩ or greater resistor from the VIN pin (see Figure 6). In some cases, the output voltage of the RT8278 may still be under UVP threshold when soft-start finishes. Then the RT8278 will restart again and the output voltage of the RT8278 will rise to the regulation voltage. This phenomenon often happens in high frequency operation and with slow rising input voltage. It can easily be solved by adding a voltage divider on the EN pin. The RT8278 will be enabled when the input voltage rises close to the nominal input voltage.

**Inductor Selection**

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI<sub>L</sub> increases with higher V<sub>IN</sub> and decreases with higher inductance :

$$\Delta I_L = \left[ \frac{V_{OUT}}{f_{SW} \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Higher frequency combined with smaller ripple current is necessary to achieve high efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, setting the maximum value of the ripple current ΔI<sub>L</sub> = 0.24(I<sub>MAX</sub>) is a reasonable starting point. The largest ripple current occurs at the highest V<sub>IN</sub>. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[ \frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

The inductor's current rating (defined by that which causes a temperature rise from 25°C ambient to 40°C) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Refer to Table 2 for the suggested inductor selection.

**Table2. Suggested Inductors for Typical Application Circuit**

| Component Supplier | Series   | Dimensions (mm)   |
|--------------------|----------|-------------------|
| TDK                | VLC6045  | 6 x 6 x 4.5       |
| TDK                | SLF12565 | 12.5 x 12.5 x 6.5 |
| TAIYO YUDEN        | NR8040   | 8 x 8 x 4         |

**Diode Selection**

When the power switch turns off, the path for the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimal voltage drop and recovery time. Schottky diodes are recommended and should be able to handle those current. The reverse voltage rating of the diode should be greater than the maximum input voltage, and the current rating should be greater than the maximum load current. For details, please refer to Table 3.

**Table 3. Suggested Diode**

| Component Supplier | Series | V <sub>RRM</sub> (V) | I <sub>OUT</sub> (A) | Package  |
|--------------------|--------|----------------------|----------------------|----------|
| DIODES             | B330A  | 30                   | 3                    | SMA      |
| DIODES             | B220A  | 20                   | 2                    | SMA      |
| PANJIT             | SK22   | 20                   | 2                    | DO-214AA |
| PANJIT             | SK23   | 30                   | 2                    | DO-214AA |

**C<sub>IN</sub> and C<sub>OUT</sub> Selection**

The input capacitance, C<sub>IN</sub>, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V<sub>IN</sub> = 2V<sub>OUT</sub>, where I<sub>RMS</sub> = I<sub>OUT</sub> / 2. This simple worst-case condition is commonly used for design.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, one 10μF low ESR ceramic capacitors is recommended. For the recommended capacitor, please refer to Table 4 below for more details.

The selection of C<sub>OUT</sub> is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C<sub>OUT</sub> selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV<sub>OUT</sub>, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI<sub>L</sub> increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Nevertheless, high value low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V<sub>IN</sub>. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V<sub>IN</sub> large enough to damage the part.

**Checking Transient Response**

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{OUT}$  immediately shifts by an amount equal to  $\Delta I_{LOAD} (ESR)$  and  $C_{OUT}$  also begins to be charged or discharged generating a feedback error signal for the regulator to return  $V_{OUT}$  to its steady state value. During this recovery time,  $V_{OUT}$  can be monitored for overshoot or ringing to indicate any stability problem.

**Compensation Parameters**

The switching frequency of RT8278 can be programmed from free running frequency to 3MHz. Table 1 only lists the recommended compensation parameters for 2.2MHz switching frequency. Optimized compensation parameters for other switching frequency can also be determined through below procedures. The first step is to decide the crossover frequency,  $f_c$ . In general, the crossover frequency is one tenth of the switching frequency. Then,  $R_c$  can be obtained through the following equation :

$$C_C = \frac{1}{2\pi \times R_C \times \frac{f_c}{4}}$$

where

$g_{CS}$  is Current Sense Transconductance = 1.8 (A/V)

$g_{EA}$  is Error Amplifier Transconductance = 920 ( $\mu A/V$ )

Once the value of  $R_c$  has been determined, the value of  $C_c$  can be obtained by the following equation :

$$R_C = \frac{2\pi \times C_{OUT} \times f_c \times V_{OUT}}{g_{CS} \times g_{EA} \times V_{FB}}$$

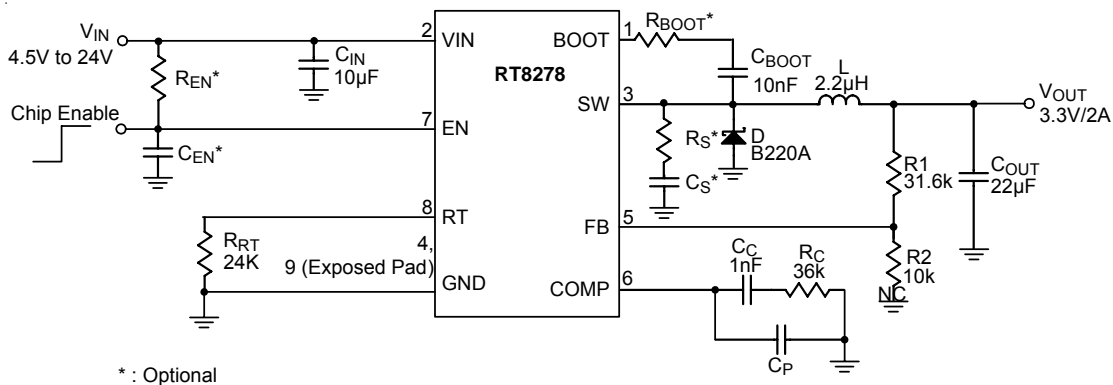
Choose a capacitor that is greater than the above calculation result. The frequency of the zero, which consists of  $R_C$  and  $C_C$ , should be lower than one fourth of  $f_c$  to get a sufficient phase margin. If the zero moves close to  $f_c$ , the phase margin decreases.

In some applications, the output capacitor will be an electrolytic capacitor, not a ceramic capacitor. A zero will be produced by the electrolytic capacitor and its ESR.  $C_P$  can be used to produce a pole with  $R_C$  to cancel the zero. To calculate  $C_P$ , follow the equation below :

$$C_P = \frac{C_{OUT} \times ESR}{R_C}$$

**EMI Consideration**

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on the SW pin when the high side MOSFET is turned-on/off, this spike voltage on SW may impact EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C snubber between SW and GND and place them as close as possible to the SW pin (see Figure 6). Another method is to add a resistor in series with the bootstrap capacitor,  $C_{BOOT}$ . But this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful for EMI performance. For detailed PCB layout guide, please refer to the section on Layout Consideration.



\* : Optional

Figure 6. Reference Circuit with Snubber and Enable Timing Control

**Thermal Considerations**

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8278, the maximum junction temperature is 125°C and  $T_A$  is the ambient temperature. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance,  $\theta_{JA}$ , is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A=25^\circ\text{C}$  can be calculated by the following formulas :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C/W}) = 1.333\text{W}$$

(min. copper area PCB layout)

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.04\text{W}$$

(70mm<sup>2</sup> copper area PCB layout)

The thermal resistance,  $\theta_{JA}$ , of SOP-8 (Exposed Pad) is determined by the package architectural design and the PCB layout design. The package architectural design is fixed. However, it's possible to increase thermal performance via better PCB layout copper design. The thermal resistance,  $\theta_{JA}$ , can be decreased by adding copper area under the exposed pad of the SOP-8 (Exposed Pad) package.

As shown in Figure 7, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted on affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) (Figure 7a),  $\theta_{JA}$  is 75°C/W. Adding copper area under the SOP-8 (Exposed Pad) (Figure 7b) reduces  $\theta_{JA}$  to 64°C/W. Further increasing the copper area to 70mm<sup>2</sup> (Figure 7e) will reduce  $\theta_{JA}$  to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal

resistance,  $\theta_{JA}$ . For the RT8278 packages, the derating curves in Figure 8 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

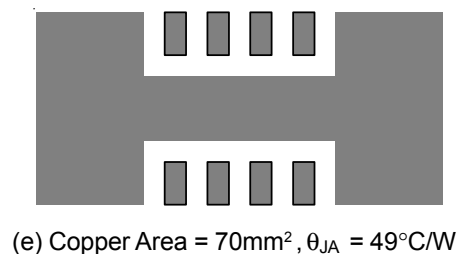
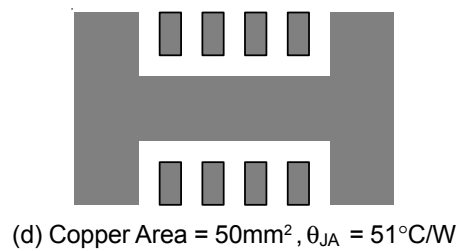
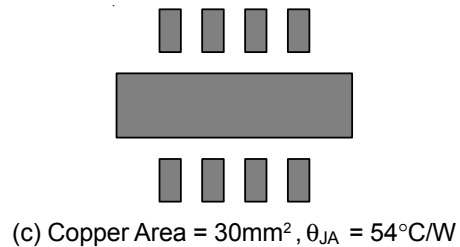
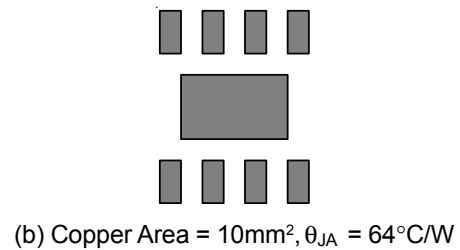
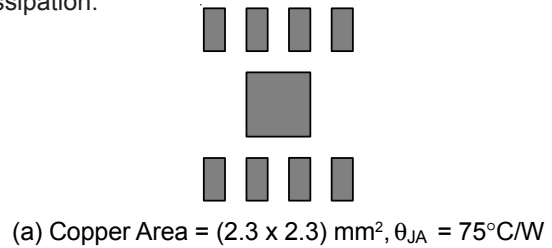


Figure 7. Thermal Resistance vs. Copper Area Layout Design

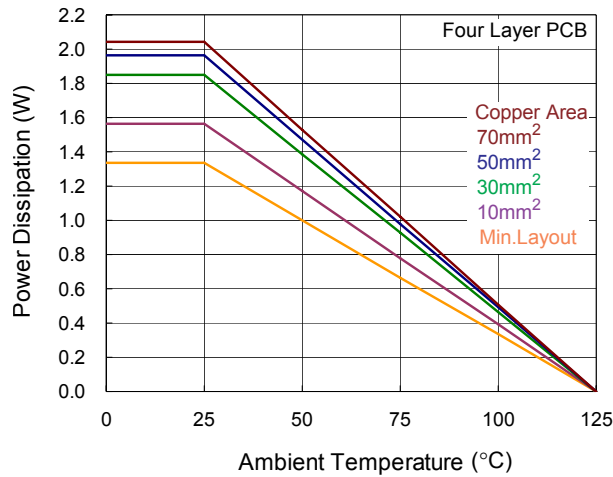


Figure 8. Derating Curves for RT8278 Package

**Layout Consideration**

Follow the PCB layout guidelines for optimum performance of the RT8278.

- ▶ Keep the traces of the main current paths as short and wide as possible.
- ▶ Place the input capacitor as close as possible to the device pins (VIN and GND).
- ▶ SW node experiences high frequency voltage swing and should be kept in a small area. Keep analog components away from the SW node to prevent stray capacitive noise pick up.

- ▶ Connect the feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8278.
- ▶ Connect all analog grounds to a common node and then connect the common node to ground behind the output capacitors.
- ▶ An example of the PCB layout guide is shown in Figure 9 for reference.

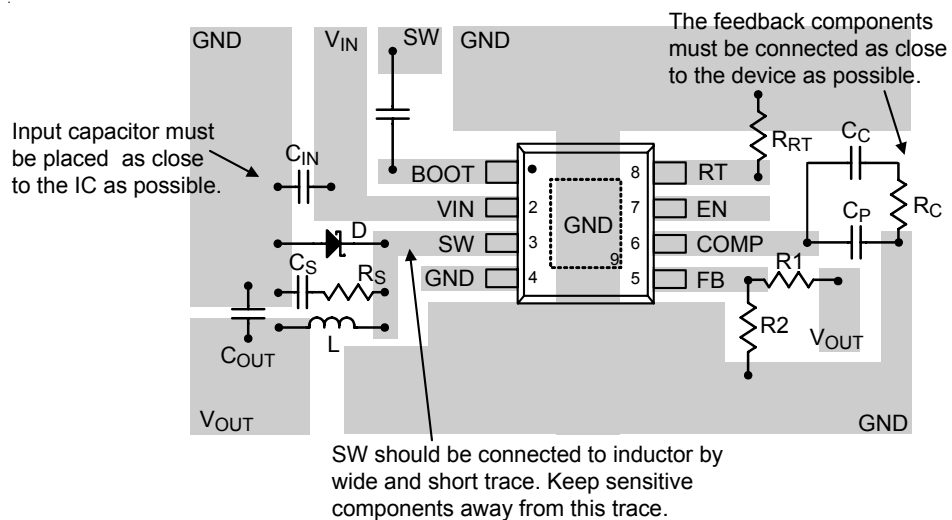


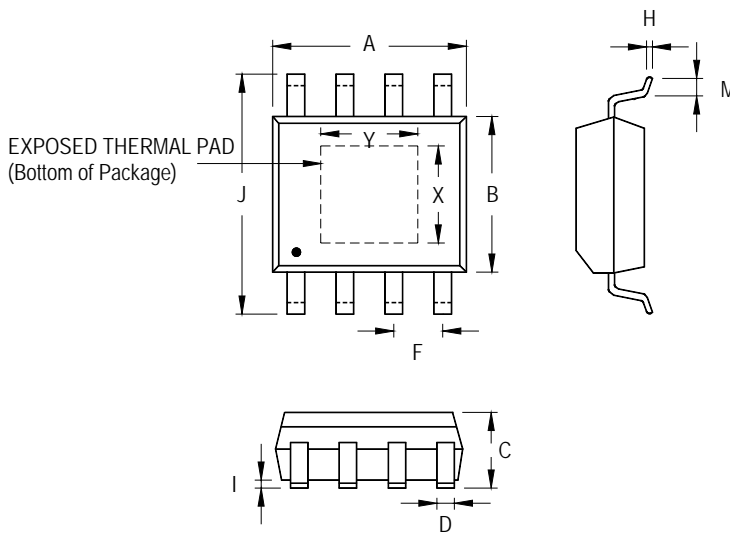
Figure 9. PCB Layout Guide

**Table 4. Suggested Capacitors for C<sub>IN</sub> and C<sub>OUT</sub>**

| Location         | Component Supplier | Part No.       | Capacitance (μF) | Case Size |
|------------------|--------------------|----------------|------------------|-----------|
| C <sub>IN</sub>  | MURATA             | GRM31CR61E106K | 10               | 1206      |
| C <sub>IN</sub>  | TDK                | C3225X5R1E106K | 10               | 1206      |
| C <sub>IN</sub>  | TAIYO YUDEN        | TMK316BJ106ML  | 10               | 1206      |
| C <sub>OUT</sub> | MURATA             | GRM31CR60J476M | 47               | 1206      |
| C <sub>OUT</sub> | TDK                | C3225X5R0J476M | 47               | 1210      |
| C <sub>OUT</sub> | MURATA             | GRM32ER71C226M | 22               | 1210      |
| C <sub>OUT</sub> | TDK                | C3225X5R1C226M | 22               | 1210      |



Outline Dimension



| Symbol   | Dimensions In Millimeters |       | Dimensions In Inches |       |       |
|----------|---------------------------|-------|----------------------|-------|-------|
|          | Min                       | Max   | Min                  | Max   |       |
| A        | 4.801                     | 5.004 | 0.189                | 0.197 |       |
| B        | 3.810                     | 4.000 | 0.150                | 0.157 |       |
| C        | 1.346                     | 1.753 | 0.053                | 0.069 |       |
| D        | 0.330                     | 0.510 | 0.013                | 0.020 |       |
| F        | 1.194                     | 1.346 | 0.047                | 0.053 |       |
| H        | 0.170                     | 0.254 | 0.007                | 0.010 |       |
| I        | 0.000                     | 0.152 | 0.000                | 0.006 |       |
| J        | 5.791                     | 6.200 | 0.228                | 0.244 |       |
| M        | 0.406                     | 1.270 | 0.016                | 0.050 |       |
| Option 1 | X                         | 2.000 | 2.300                | 0.079 | 0.091 |
|          | Y                         | 2.000 | 2.300                | 0.079 | 0.091 |
| Option 2 | X                         | 2.100 | 2.500                | 0.083 | 0.098 |
|          | Y                         | 3.000 | 3.500                | 0.118 | 0.138 |

8-Lead SOP (Exposed Pad) Plastic Package

**Richtek Technology Corporation**

Headquarter  
 5F, No. 20, Taiyuen Street, Chupei City  
 Hsinchu, Taiwan, R.O.C.  
 Tel: (8863)5526789 Fax: (8863)5526611

**Richtek Technology Corporation**

Taipei Office (Marketing)  
 5F, No. 95, Minchiuan Road, Hsintien City  
 Taipei County, Taiwan, R.O.C.  
 Tel: (8862)86672399 Fax: (8862)86672377  
 Email: marketing@richtek.com

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