1.8A, 24V, 1.4MHz Step-Down Converter

General Description

The RT8260A is a high voltage buck converter that can support the input voltage range from 4.5V to 24V and the output current can be up to 1.8A. Current Mode operation provides fast transient response and eases loop stabilization.

The chip also provides protection functions such as cycle-by-cycle current limiting and thermal shutdown protection. The RT8260A is available in a WDFN-8L 2x2 package.

Ordering Information

RT8260A □□

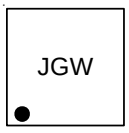
- Package Type
  QW : WDFN-8L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



JG : Product Code

W : Date Code

Features

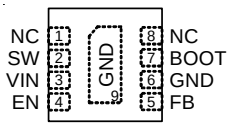
- **Wide Operating Input Voltage Range : 4.5V to 24V**
- **Adjustable Output Voltage Range : 0.8V to 15V**
- **1.8A Output Current**
- **0.3Ω Internal Power MOSFET Switch**
- **High Efficiency up to 92%**
- **1.4MHz Fixed Switching Frequency**
- **Stable with Low ESR Output Ceramic Capacitors**
- **Thermal Shutdown**
- **Cycle-By-Cycle Over Current Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Distributed Power Systems
- Battery Charger
- Pre-Regulator for Linear Regulators
- WLED Drivers

Pin Configurations

(TOP VIEW)



WDFN-8L 2x2

Typical Application Circuit

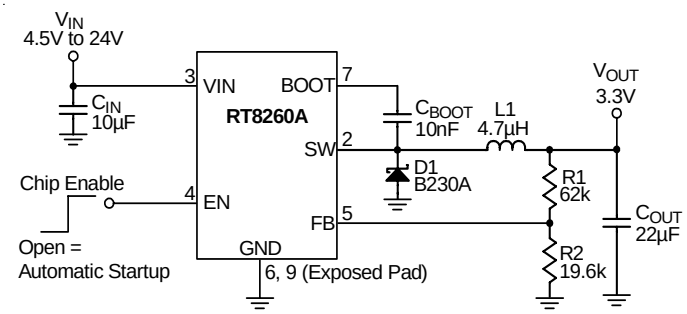


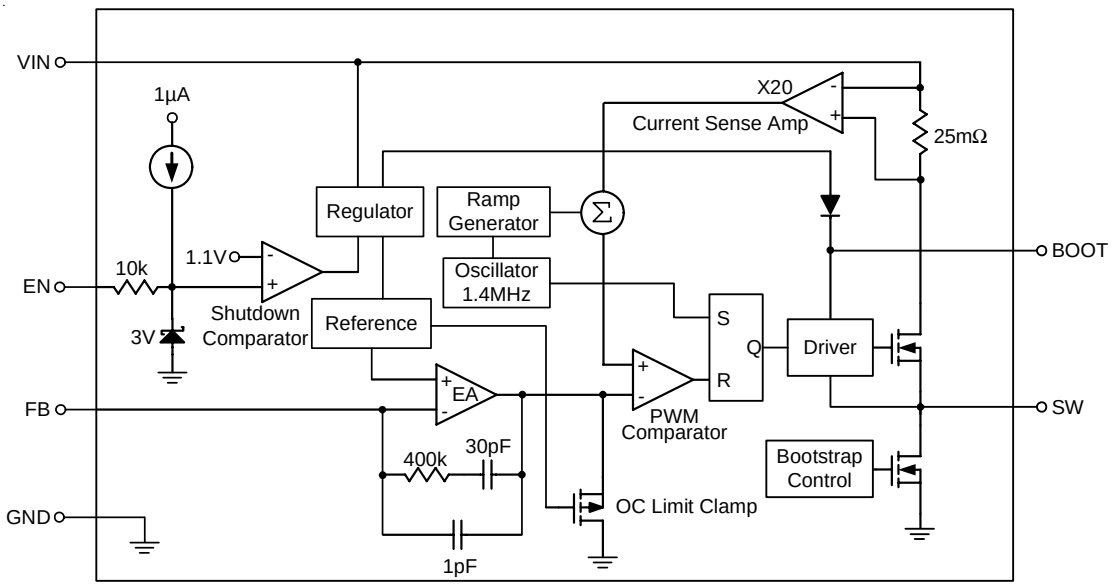
Table 1. Recommended Component Selection

V_{OUT} (V)	1.2	1.8	2.5	3.3	5	8	10	15
L1 (µH)	2	2	3.6	4.7	6.8	10	10	15
R2 (kΩ)	124	49.9	29.4	19.6	13	8.2	6.49	4.2
R1 (kΩ)	62	62	62	62	68	75	75	75
C_{OUT} (µF)	22	22	22	22	22	22	22	22

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 8	NC	No Internal Connection.
2	SW	Switch Output.
3	VIN	Supply Voltage. Bypass VIN to GND with a suitable large capacitor to prevent large voltage spikes from appearing at the input.
4	EN	Chip Enable (Active High). If the EN pin is open, it will be pulled to high by internal circuit.
5	FB	Feedback. An external resistor divider from the output to GND tapped to the FB pin sets the output voltage. The value of the divider resistors also set loop bandwidth.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	BOOT	Bootstrap. A capacitor is connected between SW and BOOT pins to form a floating supply across the power switch driver. This capacitor is needed to drive the power switch's gate above the supply voltage.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ---- 26V
- SW Voltage ---- –0.3V to (V_{IN} + 0.3V)
- BOOT Voltage ---- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- All Other Pins ---- 0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 2x2 ---- 0.833W
- Package Thermal Resistance (Note 2)
  WDFN-8L 2x2, θ_{JA} ---- 120°C/W
  WDFN-8L 2x2, θ_{JC} ---- 8.2°C/W
- Junction Temperature ---- 150°C
- Lead Temperature (Soldering, 10 sec.) ---- 260°C
- Storage Temperature Range ---- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---- 2kV
  MM (Machine Mode) ---- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---- 4.5V to 24V
- Output Voltage, V_{OUT} ---- 0.8V to 15V
- EN Voltage, V_{EN} ---- 0V to 5.5V
- Junction Temperature Range ---- –40°C to 125°C
- Ambient Temperature Range ---- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 24V	0.79	0.8	0.81	V
Feedback Current	I_{FB}	V_{FB} = 0.8V	--	0.1	0.3	μA
Switch On Resistance	$R_{DS(ON)}$		--	0.3	--	Ω
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V	--	--	10	μA
Current Limit	I_{LIM}	V_{BOOT} – V_{SW} = 4.8V	2.2	2.9	--	A
Oscillator Frequency	f_{SW}		1.2	1.4	1.6	MHz
Maximum Duty Cycle			--	75	--	%
Minimum On-Time	t_{ON}		--	100	--	ns
Under Voltage Lockout Threshold		Rising	3.9	4.2	4.5	V
Under Voltage Lockout Threshold Hysteresis			--	200	--	mV
EN Input Low Voltage			--	--	0.4	V
EN Input High Voltage			1.4	--	--	V
EN Pull Up Current		V_{EN} = 0V	--	1	--	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	25	--	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 1V (Not Switching)	--	0.55	1	mA
Thermal Shutdown	T_{SD}		--	150	--	°C

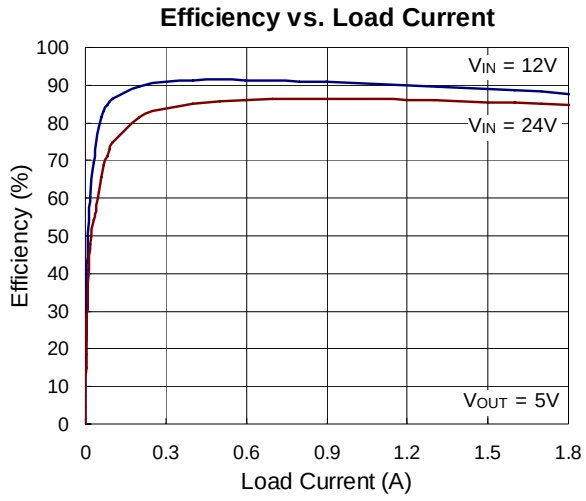
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

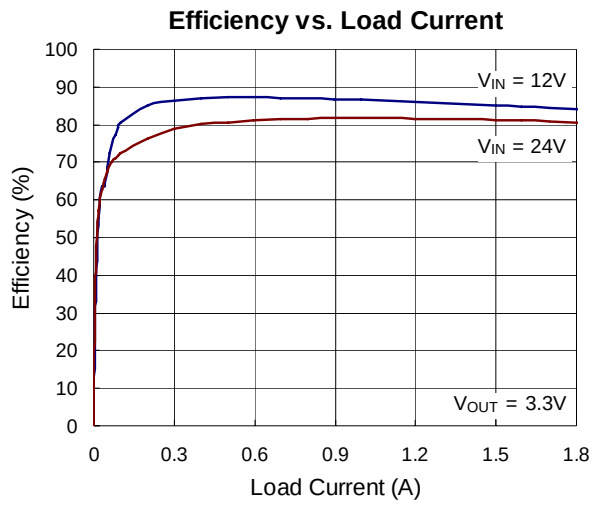
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

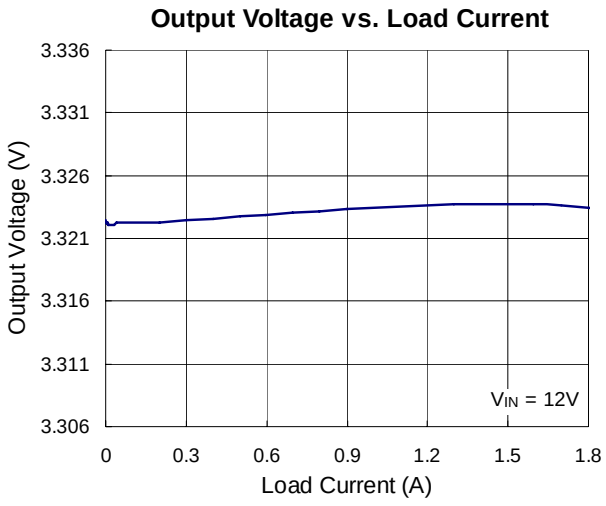
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

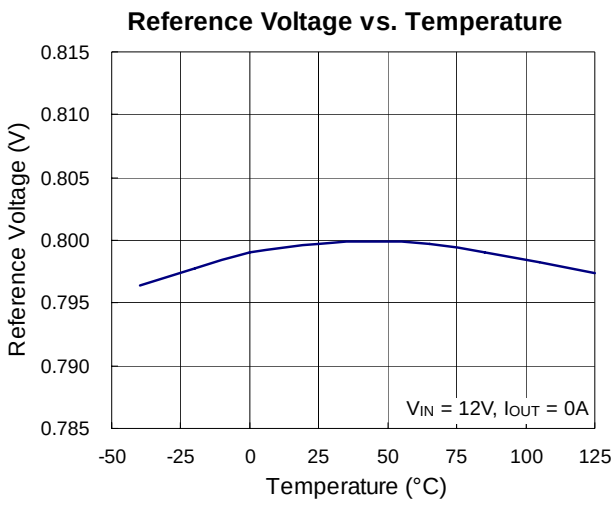
Note 4. The device is not guaranteed to function outside its operating conditions.

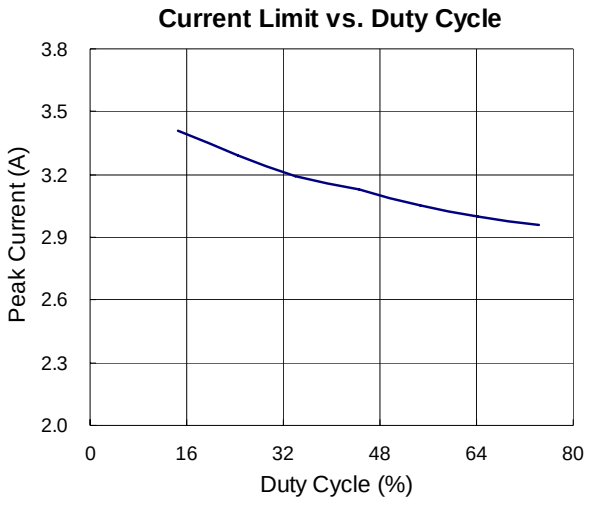
Typical Operating Characteristics

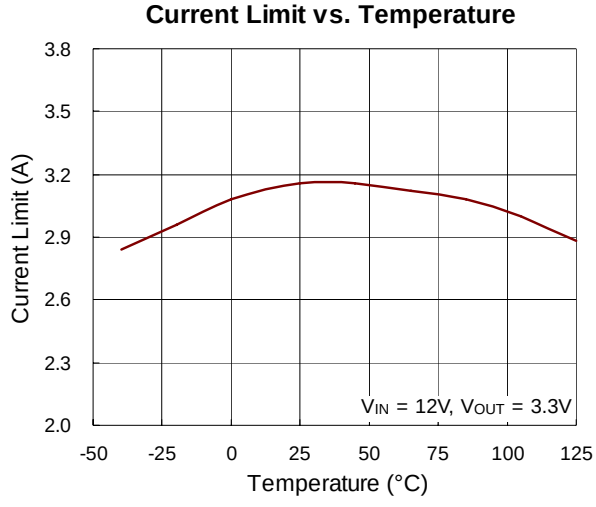




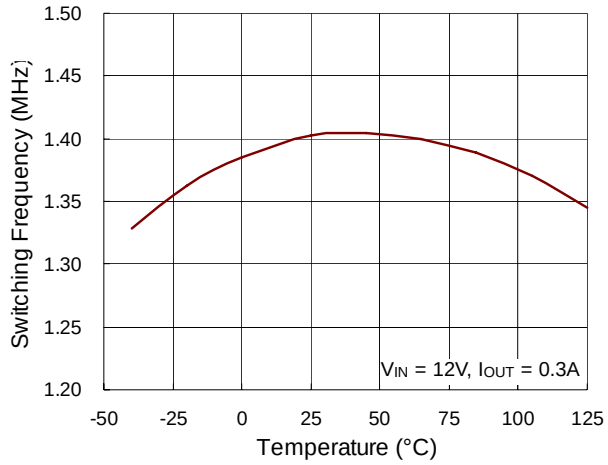




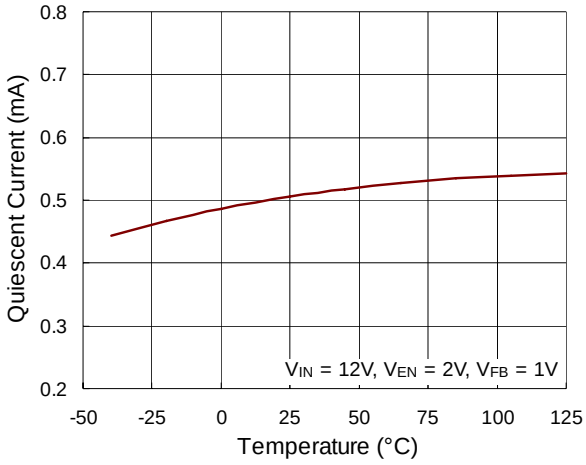




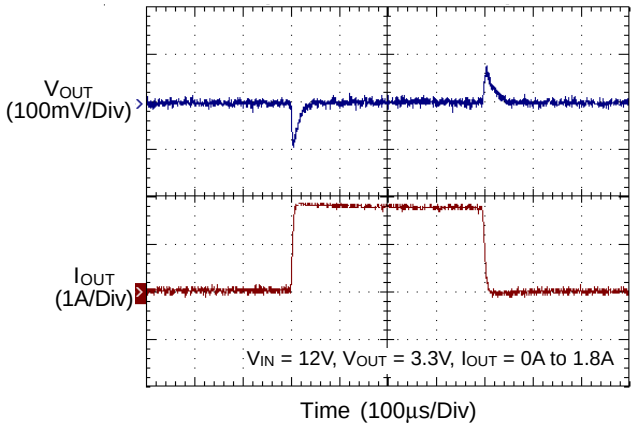
Switching Frequency vs. Temperature



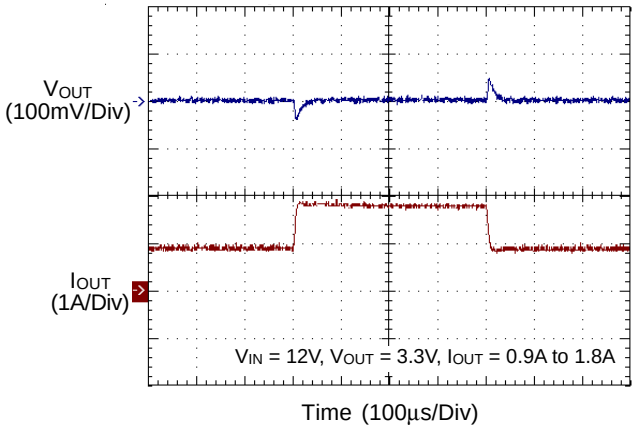
Quiescent Current vs. Temperature



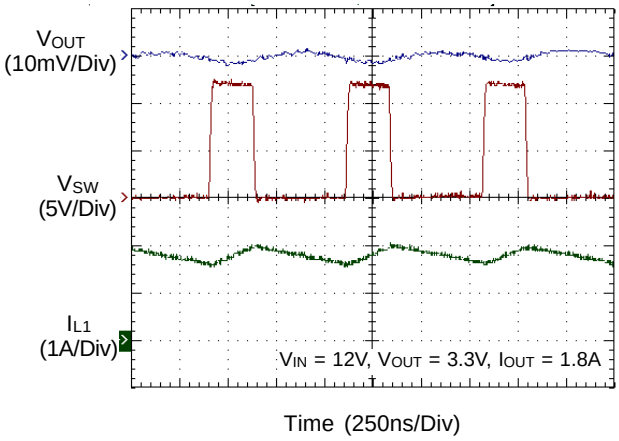
Load Transient Response



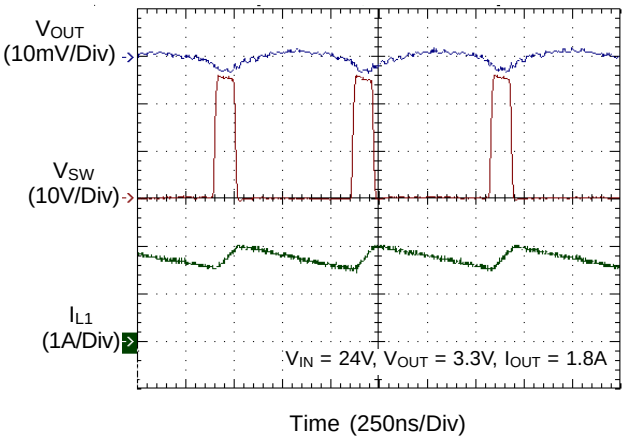
Load Transient Response



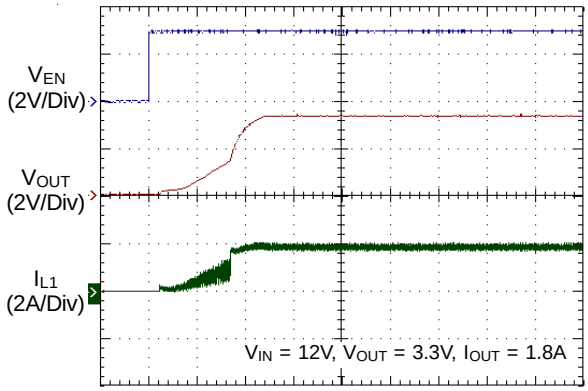
Output Ripple



Output Ripple

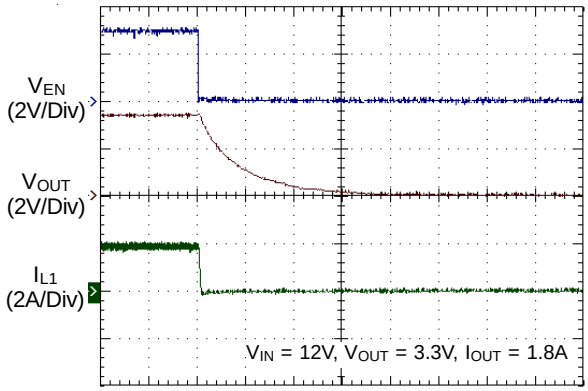


Power On from EN



Time (250μs/Div)

Power Off from EN



Time (50μs/Div)

Application Information

The RT8260A is a high voltage buck converter that can support the input voltage range from 4.5V to 24V and the output current can be up to 1.8A.

Output Voltage Setting

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

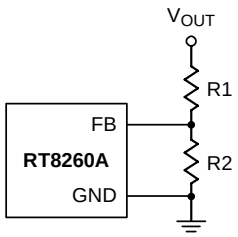


Figure 1. Output Voltage Setting

For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

The external 5V can be a 5V fixed input from system or a 5V output of the RT8260A. Note that the external boot voltage must be lower than 5.5V.

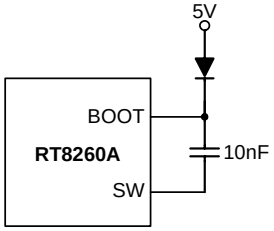


Figure 2. External Bootstrap Diode

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L = 0.24 (I_{MAX} = 1.8) will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1-\frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (defined by that which causes a temperature rise from 25°C ambient to 40°C) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Refer to Table 2 for the suggested inductor selection.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLC6045	6 x 6 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

Diode Selection

When the power switch turns off, the path for the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimum voltage drop and recovery times. Schottky diode is recommended and it should be able to handle those current. The reverse voltage rating of the diode should be greater than the maximum input voltage, and current rating should be greater than the maximum load current. For more detail, please refer to Table 3.

Table 3. Suggested Diode

Component Supplier	Series	V_{RRM} (V)	I_{OUT} (A)	Package
DIODES	B220A	20	2	SMA
DIODES	B230A	30	2	SMA
PANJIT	SK22	20	2	DO-214AA
PANJIT	SK23	30	2	DO-214AA

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the required Effective Series Resistance (ESR) to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on the SW pin when the high side MOSFET is turned-on/off, this spike voltage on SW may impact EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C snubber between SW and GND and place them as close as possible to the SW pin (see Figure 3). Another method is to add a resistor in series with the bootstrap capacitor, C_{BOOT}. But this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to

reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful for EMI performance. For detailed PCB layout guide, please refer to the section on Layout Consideration.

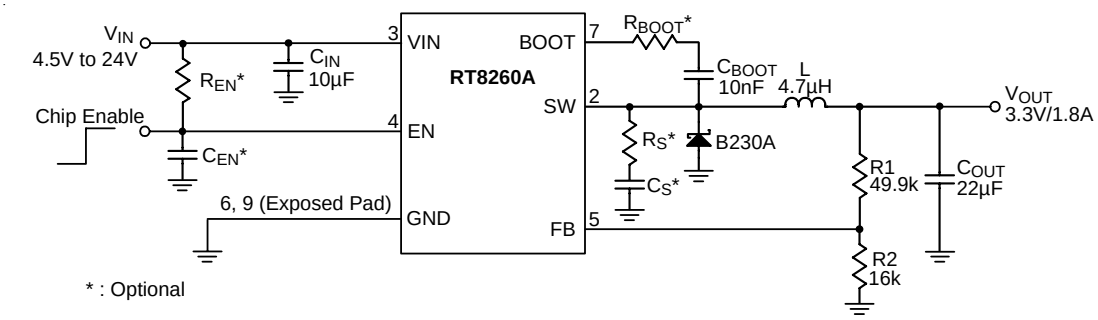


Figure 3. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8260A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8L 2x2 packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (120°C/W) = 0.833W$ for

WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8260A package, the derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

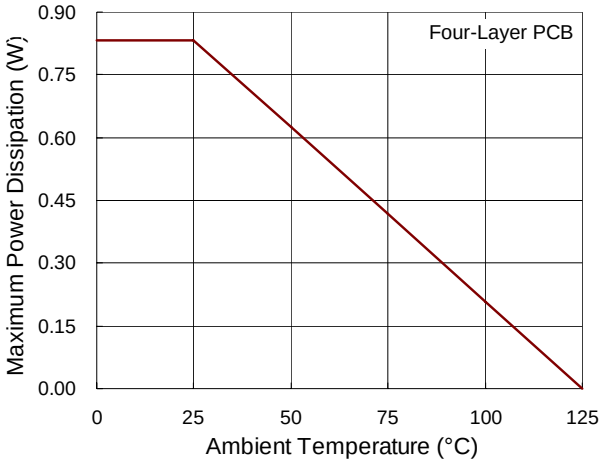


Figure 4. Derating Curves for RT8260A Packages

Layout Consideration

Follow the PCB layout guidelines for optimal performance of RT8260A.

- Keep the traces of the main current paths as short and wide as possible.
- Place the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept in a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pick-up.
- Place the feedback components as close to the FB pin as possible.
- Connect GND to a ground plane for noise reduction and thermal dissipation.

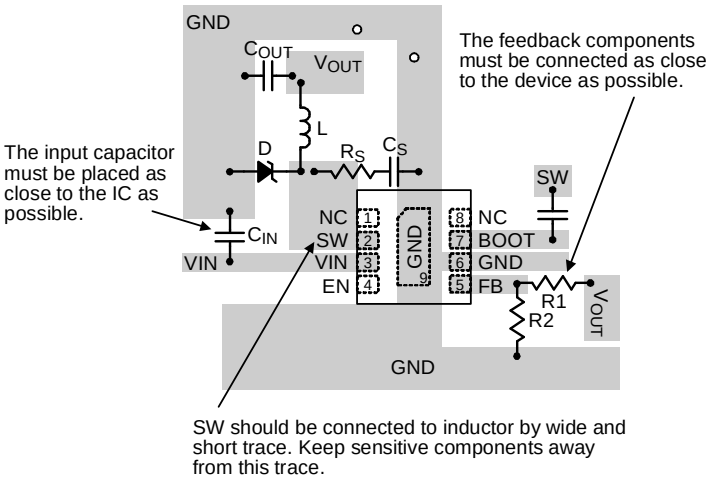
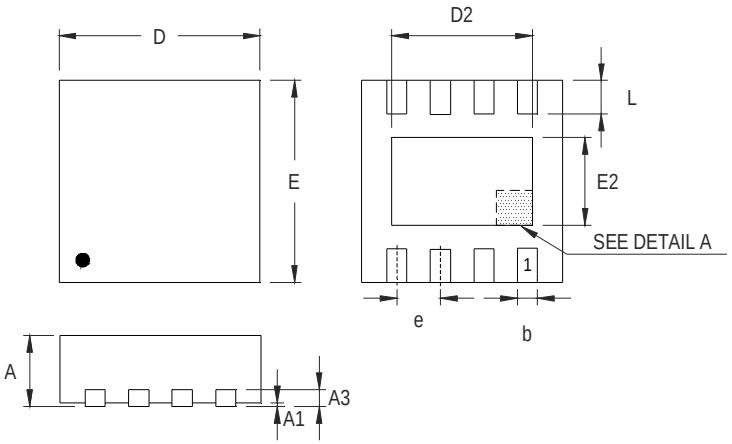


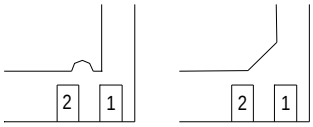
Figure 5. PCB Layout Guide

Table 4. Suggested Capacitors for CIN and COUT

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C_{IN}	**MURATA**	GRM31CR61E106K	10	1206
C_{IN}	**TDK**	C3225X5R1E106K	10	1206
C_{IN}	**TAIYO YUDEN**	TMK316BJ106ML	10	1206
C_{OUT}	**MURATA**	GRM31CR61C226M	22	1206
C_{OUT}	**TDK**	C3225X5R1C226M	22	1206
C_{OUT}	**TAIYO YUDEN**	EMK316BJ226ML	22	1206

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

Richtek Technology Corporation

Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com