AAT3258

300mA LDO Linear Regulator with µP Reset

PowerLinear™

General Description

The AAT3258 combines a high performance, low noise, 300mA low dropout (LDO) linear regulator with a microprocessor reset monitor. The 300mA output capability of the LDO regulator makes this device ideal for use with microprocessors and DSP cores in portable products. The microprocessor reset monitor section has very low quiescent current consumption and has an active low reset output. The AAT3258 has separate input pins for the reset monitor and LDO regulator so they may be operated from independent sources for increased design flexibility. This device features very low quiescent current, typically less than 71µA.

The LDO regulator has low dropout voltage, typically 400mV at the full output current level, making it ideal for portable applications where extended battery life is critical. The AAT3258 LDO regulator section has complete over-current/short-circuit and over-temperature protection circuits to guard against extreme operating conditions. The device also has an active output pull down function when disabled.

The AAT3258 is available in a space-saving 8-pin TSOPJW package. This device is capable of operation over a -40°C to +85°C temperature range.

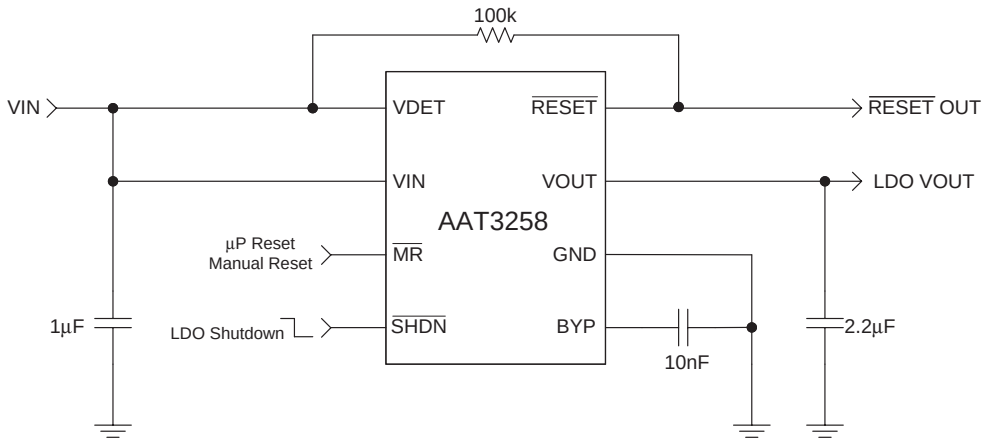
Features

- Integrated LDO Regulator with µP Reset
- 300mA Output LDO Regulator
- Low Dropout Regulator, 400mV at 300mA
- High LDO Output Voltage Accuracy, Typically 1.5%
- Very Low Noise and High Power Supply Rejection Ratio (PSRR) LDO
- Low Quiescent Current at 71µA
- LDO Over-Current/Short-Circuit Protection
- LDO Over-Temperature Protection
- LDO Power Saving Shutdown Mode
- Independent Device Power Inputs
- High Accuracy Reset Monitor Threshold: ±1.5%
- Active Low Push-Pull Monitor Reset Output
- <2.0µA of Shutdown Current
- Uses Low Equivalent Series Resistance (ESR) Ceramic Capacitors
- -40°C to +85°C Temperature Range
- 8-Pin TSOPJW Package

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instrumentation
- Microprocessor/DSP Core/IO Power
- Notebook Computers
- PDAs and Handheld Computers
- Portable Communication Devices

Typical Application

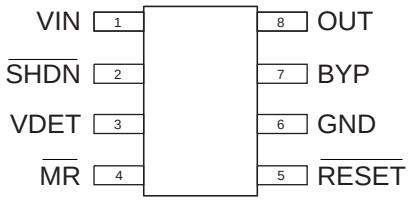


Pin Descriptions

Pin #	Symbol	Function
1	VIN	LDO voltage regulator input pin. This pin should be decoupled with 1µF or greater capacitor. See application information.
2	$\overline{SHDN}$	LDO voltage regulator shutdown pin. This pin should not be left floating. When connected low, all the internal circuitry is powered down. When high, it is in normal operation.
3	VDET	Microprocessor reset input power supply pin. It may be connected to V_{IN}.
4	$\overline{MR}$	Manual reset active low input. A logic low signal on $\overline{MR}$ asserts a reset condition. Asserted reset continues as long as $\overline{MR}$ is low and for a minimum of 150ms after $\overline{MR}$ returns high.
5	$\overline{RESET}$	Reset output remains low while V_{DET} is below the reset threshold and remains so for a minimum of 150ms after V_{DET} rises above the reset threshold.
6	GND	Ground connection pin.
7	BYP	LDO voltage regulator bypass capacitor connection. To improve AC ripple rejection and decrease LDO regulator self noise, connect a 10nF ceramic capacitor between this pin and GND.
8	OUT	LDO voltage regulator output pin; should be decoupled with a 2.2µF or greater value low ESR ceramic capacitor.

Pin Configuration

TSOPJW-8
(Top View)



Absolute Maximum Ratings[1]

T_A = 25°C, unless otherwise noted.

Symbol	Description	Value	Units
V_{IN}	Input Voltage	6.0	V
V_{RESET}	RESET to GND	-0.3 to V_{DET}+0.3	V
$V_{\overline{SHDN}IN(MAX)}$	Maximum $\overline{SHDN}$ to Input Voltage	0.3	V
I_{OUT}	LDO Regulator DC Output Current	$P_D/(V_{IN}-V_O)$	mA
I_{RESET}	Maximum Reset Output Current	20	mA
$\Delta V_{DET}/\Delta t$	Maximum Rate of V_{DET} Rise	100	V/µs
T_J	Operating Junction Temperature Range	-40 to 150	°C

Thermal Information[2]

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance (TSOPJW-8)	150	°C/W
P_D	Maximum Power Dissipation (TSOPJW-8)	833	mW

Recommended Operating Conditions

Symbol	Description	Value	Units
V_{IN}	Input Voltage to LDO[3]	(V_{OUT}+V_{DO}) to 5.5	V
V_{DET}	Input Voltage to µP Reset (0° to 70°C)	1.0 to 5.5	V
T	Ambient Temperature Range	-40 to +85	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a demo board.
3. To calculate minimum input voltage, use the following equation: $V_{IN(MIN)} = V_{OUT(MAX)} + V_{DO(MAX)}$ as long as $V_{IN} \geq 2.5V$.

Electrical Characteristics[1]

T_J = 25°C, unless otherwise noted.

Symbol	Description	Conditions		Min	Typ	Max	Units
300mA LDO Regulator							
V_{OUT}	Output Voltage	I_{OUT} = 1mA to 300mA	T_A = 25°C	-1.5		1.5	%
			T_A = -40°C to 85°C	-2.5		2.5	
I_{OUT}	Output Current	V_{OUT} > 1.2V		300			mA
I_{SC}	Short-Circuit Current	V_{OUT} < 0.4V			600		mA
I_{GND}	Ground Current	V_{IN} = 5V, No Load, $\overline{SHDN}$ = V_{IN}			70	125	µA
$I_{\overline{SHDN}}$	Shutdown Current	V_{IN} = 5V, $\overline{SHDN}$ = 0V				1.0	µA
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation	V_{IN} = V_{OUT} + 1 to 5.0V				0.09	%/V
ΔV_{OUT} (line)	Dynamic Line Regulation	I_{OUT} = 300mA, T_R/T_R = 2µs, V_{IN} = V_{OUT} + 1V to V_{OUT} + 2V			2.5		mV
V_{OUT} (load)	Dynamic Load Regulation	I_{OUT} = 1mA to 300mA, T_R < 5µs			60		mV
T_{ENDLY}	Enable Delay Time	BYP = Open			15		µs
V_{DO}	Dropout Voltage[2]	I_{OUT} = 300mA			400	600	mV
V_{IL}	Input Low Voltage					0.6	V
V_{IH}	Input High Voltage			1.5			V
I_{IL}	Input Low Current					1.0	µA
I_{IH}	Input High Current					1.0	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA, C_{BYP} = 10nF	1kHz		67		dB
			10kHz		47		
			1MHz		45		
T_{SD}	Over-Temperature Shutdown Threshold				145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				12		°C
e_N	Output Noise				50		μV_{RMS}
TC	Output Voltage Temperature Coefficient				22		ppm/°C

1. The AAT3258 is guaranteed to meet performance specifications over the -40°C to 85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.

Electrical Characteristics[1]

T_A = 25°C, unless otherwise noted.

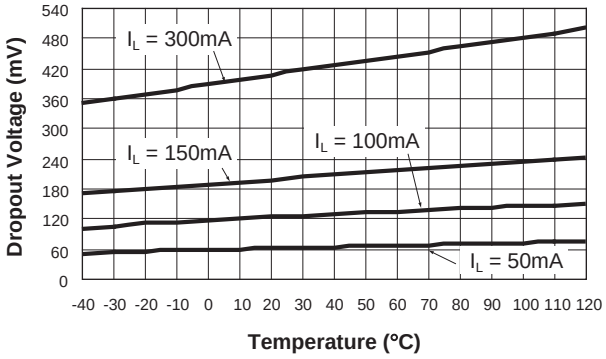
Symbol	Description	Conditions		Min	Typ	Max	Units
Microprocessor Reset Monitor							
V_{DET}	Input Voltage Range	T_A = 0°C to +70°C		1		5.5	V
		T_A = -40°C to +85°C		1.2		5.5	
I_Q	Quiescent Current	V_{CC} = 5.5V			1.05	3.0	µA
		V_{CC} = 3.0V			0.85	2.0	
I_{DD}	Operating Supply Current	V_{DET} = 3.0V			0.85	2.0	µA
I_{DOFF}	Reset Leakage Current	$V_{DET} > V_{TH}$				1.0	µA
V_{TH}	Reset Threshold Voltage	T_A = 25°C	AAT3258xxx-x.x-R	2.59	2.63	2.67	V
			AAT3258xxx-x.x-Y	2.41	2.45	2.49	
$\Delta V_{TH}/°C$	RESET Threshold Tempco				40		ppm/°C
T_P	Reset Propagation Delay	$V_{DET} = V_{TH}$ to (V_{TH} - 100mV)			15		µs
T_{RDY}	Reset Active Timeout Period			150	250	400	ms
T_{MR}	$\overline{MR}$ Minimum Pulse Width			10			µs
MRGI	$\overline{MR}$ Glitch Immunity				100		ns
R_{MR}	$\overline{MR}$ Pull-Up Resistance			30	65	90	kΩ
T_{MD}	$\overline{MR}$ to Reset Propagation Delay				0.5		µs
V_{IH}	$\overline{MR}$ Input Threshold (high)	$V_{DET} = V_{TH(MAX)}$		0.7 × V_{DET}			V
V_{IL}	$\overline{MR}$ Input Threshold (low)	$V_{DET} = V_{TH(MAX)}$				0.25 × V_{DET}	V
V_{OL}	Reset Low Voltage	I_{SINK} = 1.2mA, $V_{DET} = V_{TH(MIN)}$, $V_{TH} \leq$ 3.08V, Reset Asserted				0.3	V
		I_{SINK} = 3.2mA, $V_{DET} = V_{TH(MIN)}$, V_{TH} > 3.08V, Reset Asserted				0.4	
V_{OH}	Reset High Voltage	I_{SOURCE} = 800µA, V_{DET} > 3.08V, $V_{DET} > V_{TH(MAX)}$		V_{DET} - 1.5			V
		I_{SOURCE} = 500µA, $V_{DET} > V_{TH(MAX)}$, $V_{TH} \leq$ 3.08V		0.8 * V_{DET}			

1. The AAT3258 is guaranteed to meet performance specifications over the -40°C to 85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

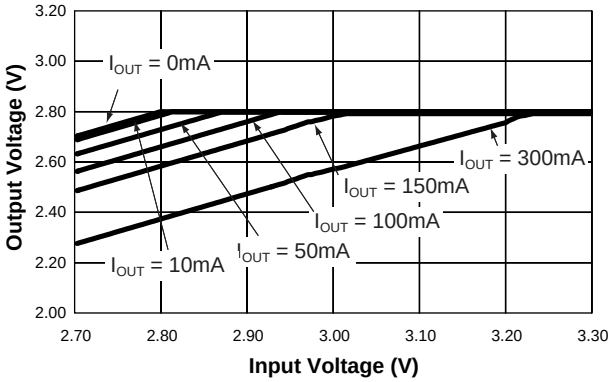
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

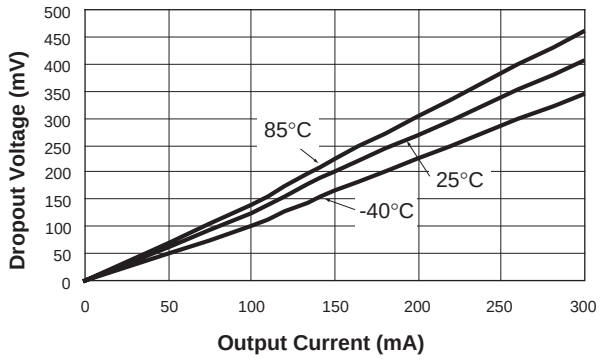
Dropout Voltage vs. Temperature



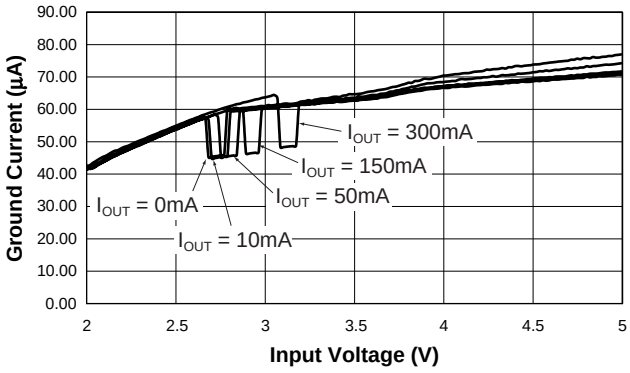
Dropout Characteristics



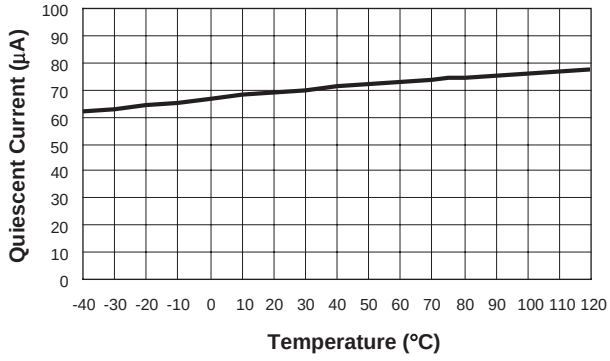
Dropout Voltage vs. Output Current



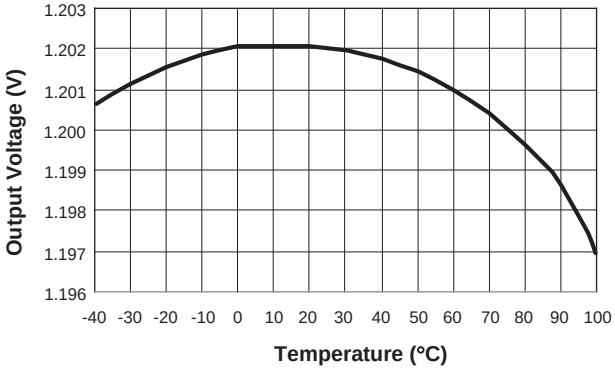
Ground Current vs. Input Voltage



Quiescent Current vs. Temperature



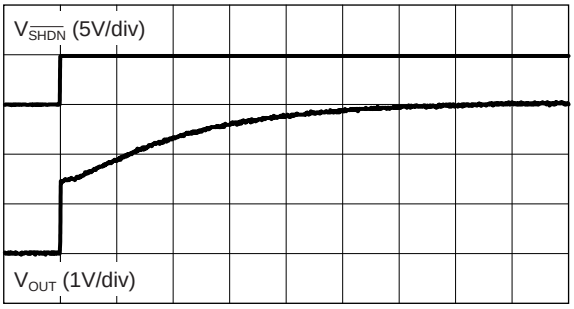
Output Voltage vs. Temperature



Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

Initial Power-Up Response Time
(C_{BYP} = 10nF)

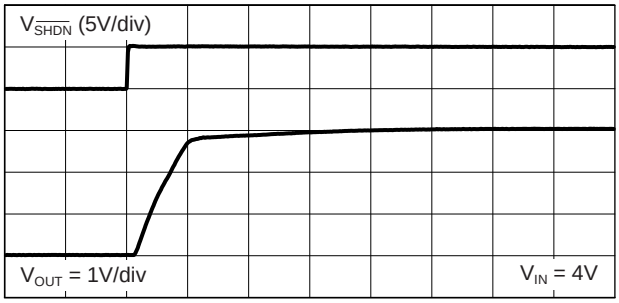


400µs/div

Turn-Off Response Time
(C_{BYP} = 10nF)

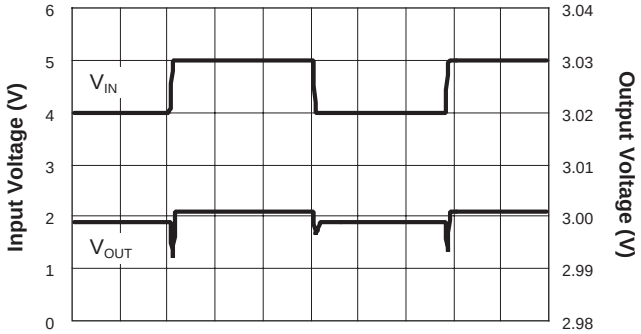
50µs/div

Turn-On Time From Enable (V_{IN} present)
(C_{BYP} = 10nF)



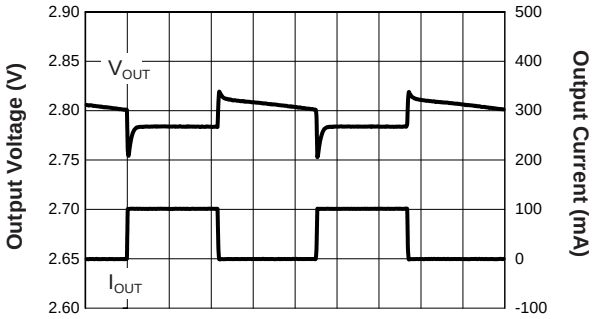
5µs/div

Line Transient Response



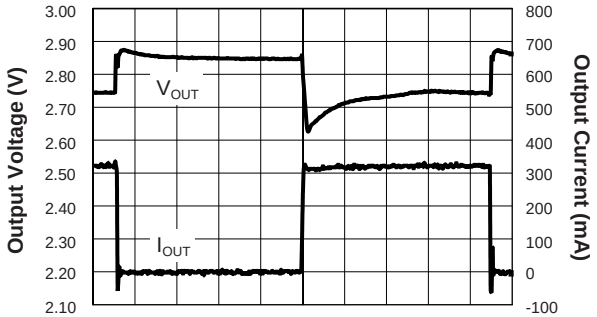
100µs/div

Load Transient Response



100µs/div

Load Transient Response 300mA

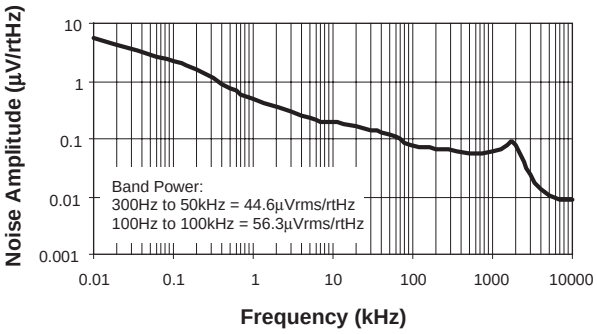


10µs/div

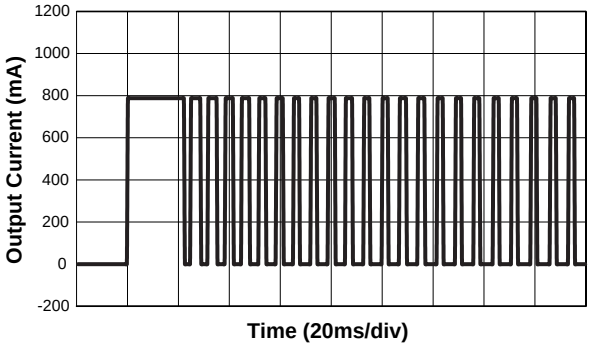
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

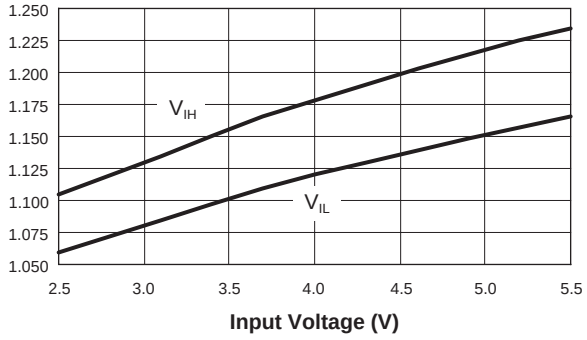
AAT3258 Self Noise
(C_{OUT} = 10µF, ceramic)



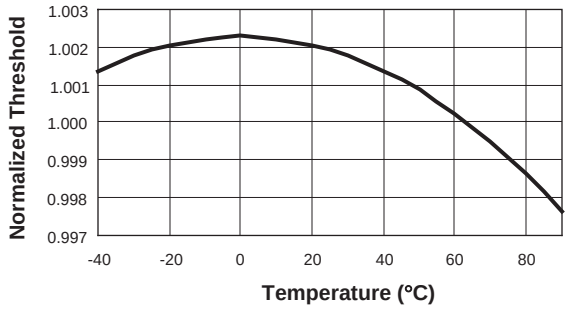
Over-Current Protection



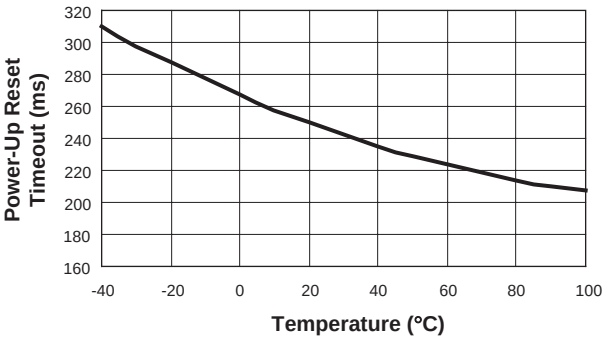
LDO $\overline{SHDN}$ V_{IH} and V_{IL} vs. V_{IN}



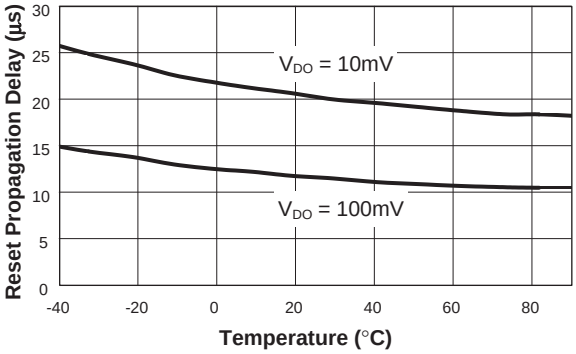
Normalized Reset Threshold vs. Temperature



Power-Up Reset Timeout vs. Temperature



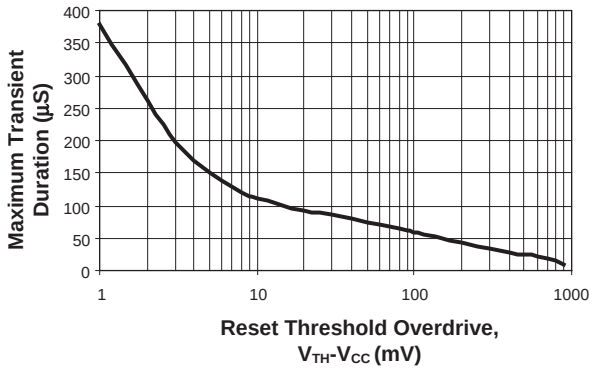
Power-Down Reset Propagation Delay vs. Temperature



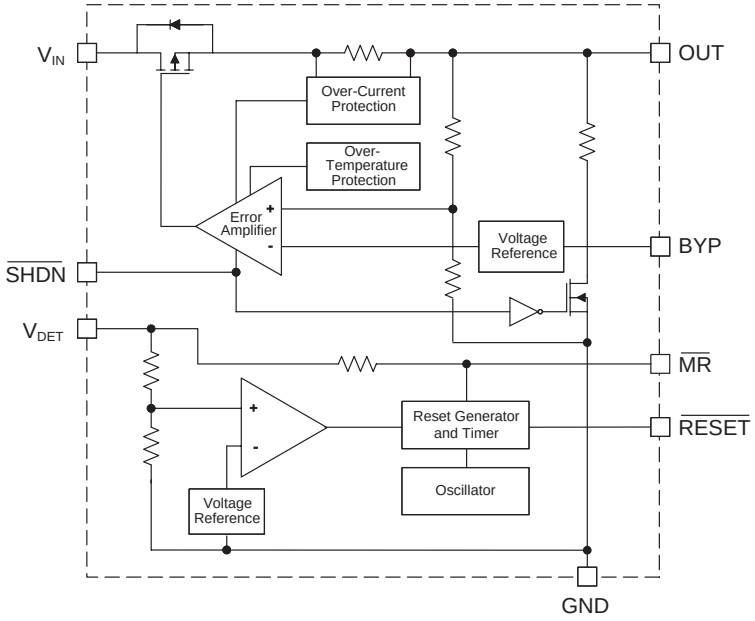
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

Maximum Transient Duration vs. Reset Threshold Overdrive



Functional Block Diagram



Functional Description

The AAT3258 is intended for LDO regulator applications where output current load requirements range from no load to 300mA.

The advanced circuit design of the AAT3258 has been specifically optimized for very fast start-up and shutdown timing. This proprietary CMOS LDO has also been tailored for superior transient response characteristics. These traits are particularly important for applications that require fast power supply timing, such as GSM cellular telephone handsets.

The high-speed turn-on capability is enabled through the implementation of a fast start control circuit, which accelerates the power-up behavior of fundamental control and feedback circuits within the LDO regulator.

Fast turn-off response time is achieved by an active output pull-down circuit, which is enabled when the LDO regulator is placed in the shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation.

The AAT3258 has very fast transient response characteristics, which is an important feature for applications where fast line and load transient response is required. This rapid transient response behavior is accomplished through the implementation of an active error amplifier feedback control. This proprietary circuit design is unique to this MicroPower LDO regulator.

The LDO regulator output has been specifically optimized to function with low-cost, low-ESR ceramic capacitors; however, the design will allow for operation over a wide range of capacitor types.

A bypass pin has been provided to allow the addition of an optional voltage reference bypass capacitor to reduce output self noise and increase power supply ripple rejection. Device self noise and PSRR will be improved by the addition of a small ceramic capacitor in this pin. However, increased values of C_{BYPASS} may slow down the LDO regulator turn-on time.

This LDO regulator has complete short-circuit and thermal protection. The integral combination of these two internal protection circuits gives the AAT3258 a comprehensive safety system to guard against extreme adverse operating conditions. Device power dissipation is limited to the package type and thermal dissipation properties. Refer to the Thermal Considerations section of this datasheet for details on device operation at maximum output current loads.

The microprocessor reset section monitors the supply voltage to a microprocessor and asserts a reset signal whenever the V_{DET} voltage falls below a factory-programmed threshold. This threshold is accurate within +/-1.5% at 25°C. The reset signal remains asserted for a minimum of 150ms after V_{DET} has risen above the threshold, as shown in Figure 1.

To assure the maximum possible performance is obtained from the AAT3258, please refer to the following application recommendations.

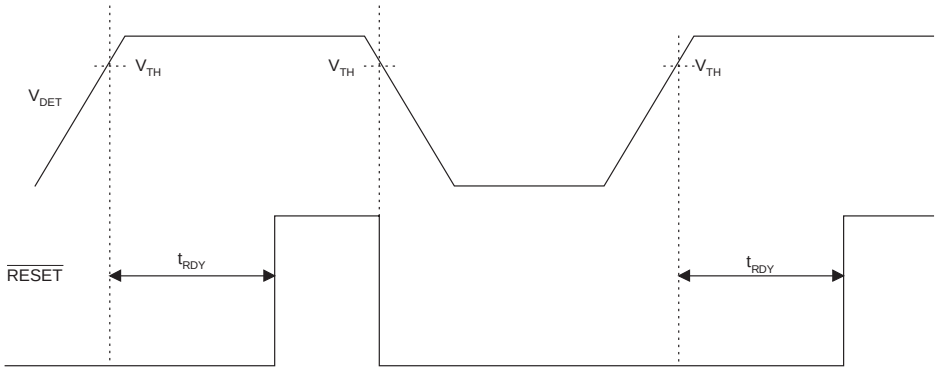


Figure 1: Reset Signal Assertion.

LDO Regulator Applications

Input Capacitor

Typically, a 1µF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT3258 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device V_{IN} pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 300mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT3258 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT3258 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit.

In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Bypass Capacitor and Low Noise Applications

A bypass capacitor pin is provided to enhance the low noise characteristics of the AAT3258 LDO regulator. The bypass capacitor is not necessary for operation. However, for best device performance, a small ceramic capacitor should be placed between the bypass pin (BYP) and the device ground pin (GND). The value of C_{BYP} may range from 470pF to 10nF. For lowest noise and best possible power supply ripple rejection performance, a 10nF capacitor should be used. To practically realize the highest power supply ripple rejection and lowest output noise performance, it is critical that the capacitor connection between the BYP pin and GND pin be direct and PCB traces should be as short as possible. Refer to the Evaluation Board Layout section of this document for examples.

There is a relationship between the bypass capacitor value and the LDO regulator turn-on and turn-off time. In applications where fast device turn-on and turn-off time are desired, the value of C_{BYP} should be reduced.

In applications where low noise performance and/or ripple rejection are less of a concern, the bypass capacitor may be omitted. The fastest device turn-on time will be realized when no bypass capacitor is used.

DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance. For this reason, the use of a low leakage, high quality, ceramic (NPO or C0G type) or film capacitor is highly recommended.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance: ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials: Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials are typically tight tolerance and are very stable over temperature. Larger capacitor values are typically composed of X7R, X5R, Z5U, and Y5V dielectric materials. Large ceramic capacitors, typically greater than 2.2µF, are often available in the low-cost Y5V and Z5U dielectrics. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%.

Capacitor area is another contributor to ESR. Capacitors that are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size.

Consult capacitor vendor data sheets carefully when selecting capacitors for LDO regulators.

Shutdown Function

The shutdown pin is designed to turn off the LDO regulator when the device is not in use. This pin is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the $\overline{SHDN}$ turn-on control level must be greater than 1.5 volts. The LDO regulator will go into the disable shutdown mode when the voltage falls below 0.6 volts. If the shutdown function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the LDO regulator is in the shutdown mode, an internal 1.5kΩ resistor is connected between V_{OUT} and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

Short-Circuit Protection

The LDO regulator section contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or the LDO regulator package power dissipation exceeds the device thermal limit.

Thermal Protection

The AAT3258 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 145°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of overtemperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 145°C trip point.

The combination and interaction between the short-circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The LDO regulator is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the LDO regulator.

In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45 volts.

MicroPower Supervisory Circuit Applications

Reset Output Options

The reset pin is an active low push-pull output. In the event of a power down or brown-out condition, the reset signal remains valid until the V_{DET} drops below 1.2V.

Manual Reset Input

A logic low signal on $\overline{MR}$ asserts a reset condition. Reset continues to be asserted as long as $\overline{MR}$ is low and for a minimum of 150ms after $\overline{MR}$ returns high. This input is internally pulled up to V_{CC} via a 20kΩ resistor, so leaving the pin unconnected is acceptable if a manual reset function is not needed. The $\overline{MR}$ input is internally debounced, which allows use of a mechanical switch. It should be a normally-open momentary switch connected from $\overline{MR}$ to GND. Additionally, the $\overline{MR}$ pin can be driven from TTL, CMOS, or open drain logic outputs.

Supply Voltage Transient Behavior

In some cases, fast negative transients of short duration can appear on the V_{CC} power supply. The AAT3258 series device provides some immunity to line transients which can generate invalid reset

pulses. Figure 2 shows typical behavior of short duration pulses versus RESET comparator overdrive. As shown in the Maximum Transient Duration vs. Reset Threshold Overdrive graph, when the transient voltage becomes larger, the time allowed before asserting a reset becomes shorter (e.g., typically a transient of 100mV below the reset threshold would have to be present for more than 50µs to cause a reset). Immunity can be increased by the addition of a small bypass capacitor of 0.1µF connected as closely to the V_{CC} pin as possible.

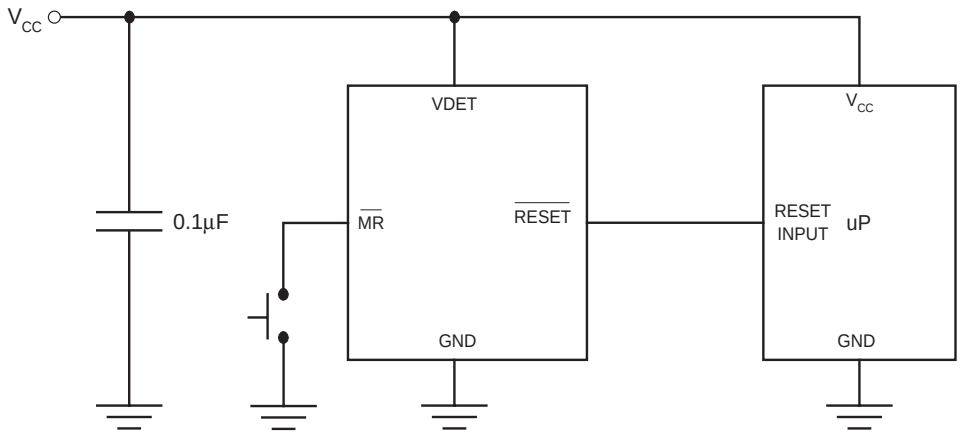


Figure 2: Typical Behavior of Short Duration Pulses vs. RESET Comparator Overdrive.

Evaluation Board Layout

The AAT3258 evaluation layout (Figures 3, 4, and 5) follows the recommend printed circuit board layout procedures and can be used as an example for good application layouts.

Note: Board layout shown is not to scale.

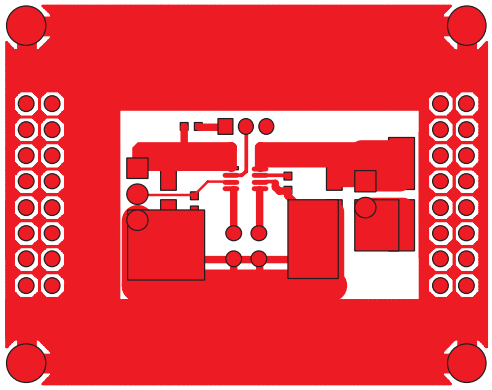


Figure 3: Evaluation Board Component Side Layout.

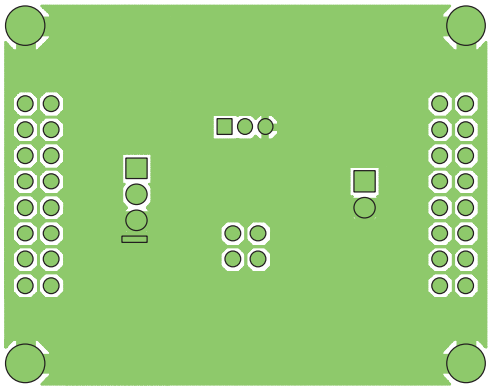


Figure 4: Evaluation Board Solder Side Layout.

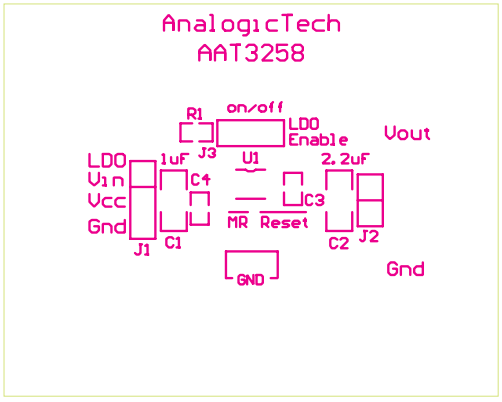


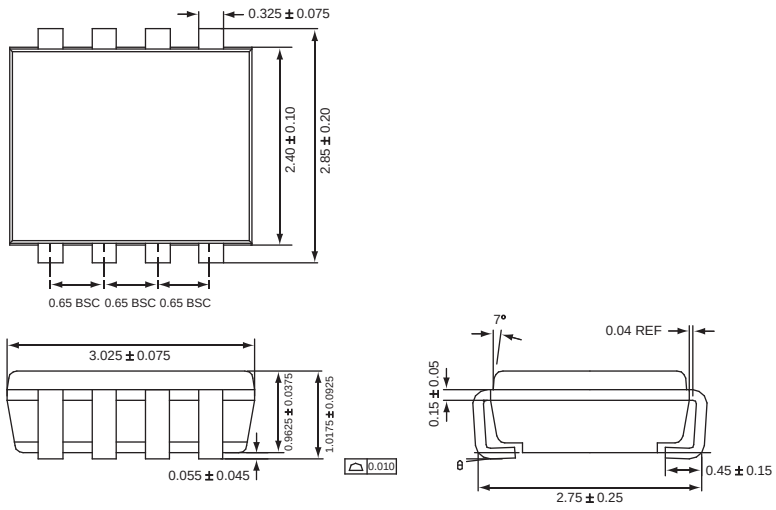
Figure 5: Evaluation Board Top Side Silk Screen Layout / Assembly Drawing.

Ordering Information

Package	Reset Threshold Voltage[1]	LDO Regulator	Marking[2]	Part Number (Tape and Reel)[3]
TSOPJW-8	2.63V	2.80V	IIXYY	**AAT3258ITS-2.8-R-T1**
TSOPJW-8	2.45V	2.80V	IHXYY	**AAT3258ITS-2.8-Y-T1**
TSOPJW-8	2.63V	3.0V	MEXYY	**AAT3258ITS-3.0-R-T1**
TSOPJW-8	2.63V	3.3V	MXXYY	**AAT3258ITS-3.3-R-T1**

Package Information

TSOPJW-8



All dimensions in millimeters.

1. Consult the factory for any additional reset or low dropout voltages.
2. XYY = assembly and date code.
3. Sample stock is generally held on part numbers listed in **BOLD**.

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