

ProASIC[®]3 Flash Family FPGAs with Optional Soft ARM[®] Support



Features and Benefits

High Capacity

- 30 k to 1 Million System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live at Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

On-Chip User Nonvolatile Memory

- 1 kbit of FlashROM with Synchronous Interfacing

High Performance

- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI (except A3P030)

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except A3P030 and ARM[®]-enabled ProASIC[®]3 devices) via JTAG (IEEE 1532-compliant)
- FlashLock[®] to Secure FPGA Contents

Low Power

- Core Voltage for Low Power
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- Ultra-Fast Local and Long-Line Network
- Enhanced High-Speed, Very-Long-Line Network

- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (A3P250 and above)
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—Up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X (except A3P030), and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS (A3P250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os (A3P030 only)
- Programmable Output Slew Rate (except A3P030) and Drive Strength
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages Across the ProASIC3 Family

Clock Conditioning Circuit (CCC) and PLL (except A3P030)

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz to 350 MHz)
- CoreMP7Sd (with debug) and CoreMP7S (without debug)

SRAMs and FIFOs (except A3P030)

- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (x1, x2, x4, x9, and x18 Organizations Available)
- True Dual-Port SRAM (except x18)
- 24 SRAM and FIFO Configurations with Synchronous Operation up to 350 MHz

Soft ARM[™] Core Support in M7 ProASIC3 Devices

- CoreMP7Sd (with debug) and CoreMP7S (without debug)

Table 1 • ProASIC3 Product Family

ProASIC3 Devices	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
ARM[®]-Enabled ProASIC3 Devices¹				M7A3P250	M7A3P400	M7A3P600	M7A3P1000
System Gates	30 k	60 k	125 k	250 k	400 k	600 k	1 M
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	9,216	13,824	24,576
RAM kbits (1,024 bits)	–	18	36	36	54	108	144
4,608-Bit Blocks	–	4	8	8	12	24	32
FlashROM Bits	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP ²	–	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	1	1	1	1	1	1
VersaNet Globals ³	6	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4
Maximum User I/Os	81	96	133	157	194	235	300
Package Pins							
QFN	QN132	QN132	QN132	QN132 ⁵			
VQFP	VQ100	VQ100	VQ100	VQ100			
TQFP		TQ144	TQ144				
PQFP			PQ208	PQ208	PQ208	PQ208	PQ208
FBGA		FG144	FG144	FG144, FG256 ⁵	FG144, FG256, FG484	FG144, FG256, FG484	FG144, FG256, FG484

Notes:

1. Refer to the CoreMP7 datasheet for more information.
2. AES is not available for ARM-enabled ProASIC3 devices.
3. Six chip (main) and three quadrant global networks are available for A3P060 and above.
4. For higher densities and support of additional features, refer to the ProASIC3E Flash FPGAs datasheet.
5. The M7A3P250 device does not support this package.

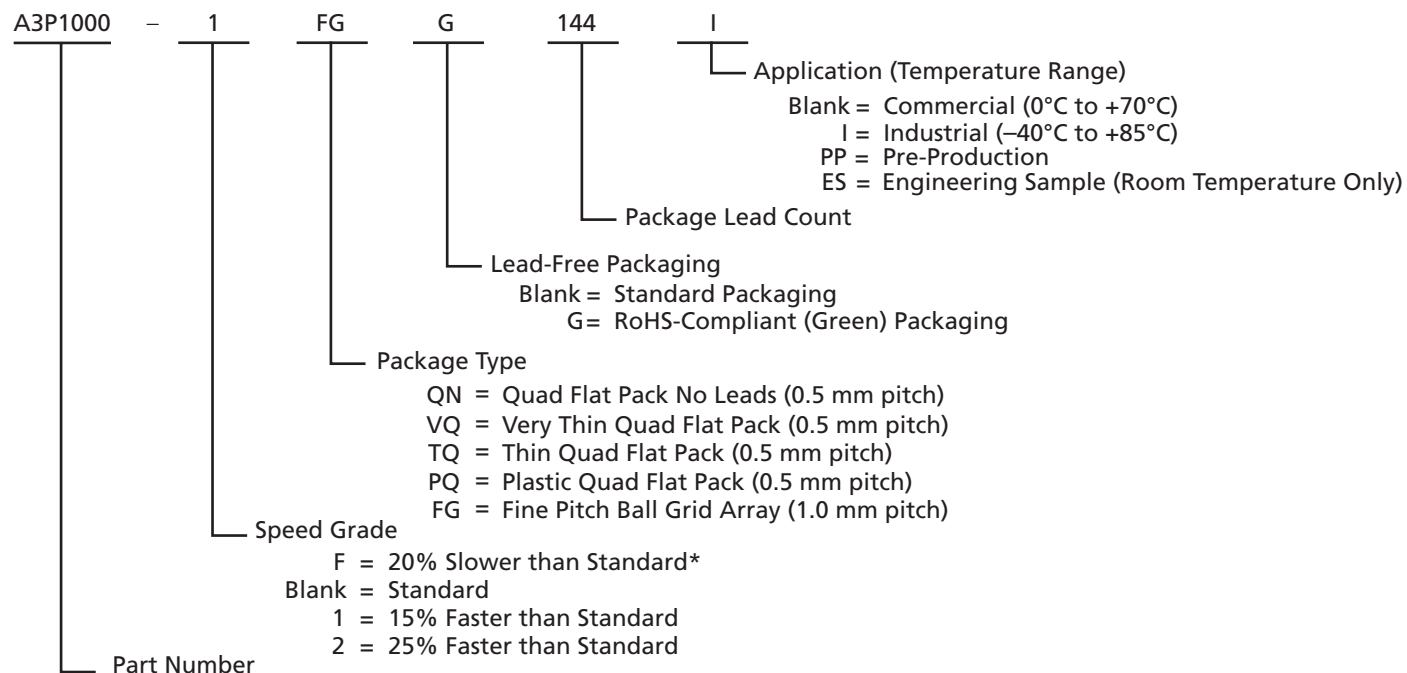
I/Os Per Package¹

ProASIC3 Devices	A3P030	A3P060	A3P125	A3P250 ³	A3P400 ³	A3P600	A3P1000				
ARM-Enabled ProASIC3 Devices				M7A3P250 ^{3,4}	M7A3P400 ³	M7A3P600	M7A3P1000				
Package	I/O Type										
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ²	Differential I/O Pairs	Single-Ended I/O ²	Differential I/O Pairs	Single-Ended I/O ²	Differential I/O Pairs	Single-Ended I/O ²	Differential I/O Pairs
QN132	81	80	84	87	19	–	–	–	–	–	–
VQ100	77	71	71	68	13	–	–	–	–	–	–
TQ144	–	91	100	–	–	–	–	–	–	–	–
PQ208	–	–	133	151	34	151	34	154	35	154	35
FG144	–	96	97	97	24	97	25	97	25	97	25
FG256	–	–	–	157	38	178	38	177	43	177	44
FG484	–	–	–	–	–	194	38	235	60	300	74

Notes:

- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15.
- The M7A3P250 device does not support FG256 or QN132 packages.
- FG256 and FG484 are footprint-compatible packages.
- "G" indicates RoHS-compliant packages. Refer to "ProASIC3 Ordering Information" on page 3 for the location of the "G" in the part number.

ProASIC3 Ordering Information



ProASIC3 Devices

A3P030 = 30,000 System Gates
 A3P060 = 60,000 System Gates
 A3P125 = 125,000 System Gates
 A3P250 = 250,000 System Gates
 A3P400 = 400,000 System Gates
 A3P600 = 600,000 System Gates
 A3P1000 = 1,000,000 System Gates

ARM-Enabled ProASIC3 Devices

M7A3P250 = 250,000 System Gates
 M7A3P400 = 400,000 System Gates
 M7A3P600 = 600,000 System Gates
 M7A3P1000 = 1,000,000 System Gates

Note: *The DC and switching characteristics for the -F speed grade targets are based only on simulation. The characteristics provided for the -F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The -F speed grade is only supported in the commercial temperature range.

Temperature Grade Offerings

Package	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
				M7A3P250 ¹	M7A3P400	M7A3P600	M7A3P1000
QN132	C, I	C, I	C, I	C, I	–	–	–
VQ100	C, I	C, I	C, I	C, I	–	–	–
TQ144	–	C, I	C, I	–	–	–	–
PQ208	–	–	C, I	C, I	C, I	C, I	C, I
FG144	–	C, I	C, I	C, I	C, I	C, I	C, I
FG256	–	–	–	C, I	C, I	C, I	C, I
FG484	–	–	–	–	C, I	C, I	C, I

Notes:

1. The M7A3P250 device does not support FG256 or QN132 packages.
2. C = Commercial temperature range: 0°C to 70°C
3. I = Industrial temperature range: –40°C to 85°C

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F ¹	Std.	–1	–2
C ²	✓	✓	✓	✓
I ³	–	✓	✓	✓

Notes:

1. The DC and switching characteristics for the –F speed grade targets are based only on simulation. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.
2. C = Commercial temperature range: 0°C to 70°C
3. I = Industrial temperature range: –40°C to 85°C

Datasheet references made to ProASIC3 devices also apply to ARM-enabled ProASIC3 devices. The ARM-enabled part numbers start with M7.

Contact your local Actel representative for device availability (<http://www.actel.com/contact/default.aspx>).

Introduction and Overview

General Description

ProASIC3, the third-generation family of Actel Flash FPGAs, offers performance, density, and features beyond those of the ProASIC^{PLUS}® family. Nonvolatile Flash technology gives ProASIC3 devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The A3P030 device has no PLL or RAM support. ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 288 user I/Os.

ProASIC3 devices support the ARM7 soft IP core in devices with at least 250 k system gates. The ARM-enabled devices have Actel ordering numbers that begin with M7A3P and do not support AES decryption.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based ProASIC3 devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, Flash-based ProASIC3 devices do not require a boot PROM, so there is no vulnerable external

bitstream that can be easily copied. ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile Flash programming can offer.

ProASIC3 devices utilize a 128-bit Flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3 devices have a built-in AES decryption engine and a Flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3 devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3 device cannot be read back, although secure design verification is possible.

ARM-enabled ProASIC3 devices do not support user-controlled AES security mechanisms. Since the ARM core must be protected at all times, AES encryption is always on for the core logic, so bitstreams are always encrypted. There is no user access to encryption for the FlashROM programming data.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3 family. The Flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An ProASIC3 device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs

and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel Flash-based ProASIC3 devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3 device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3 Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced Flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

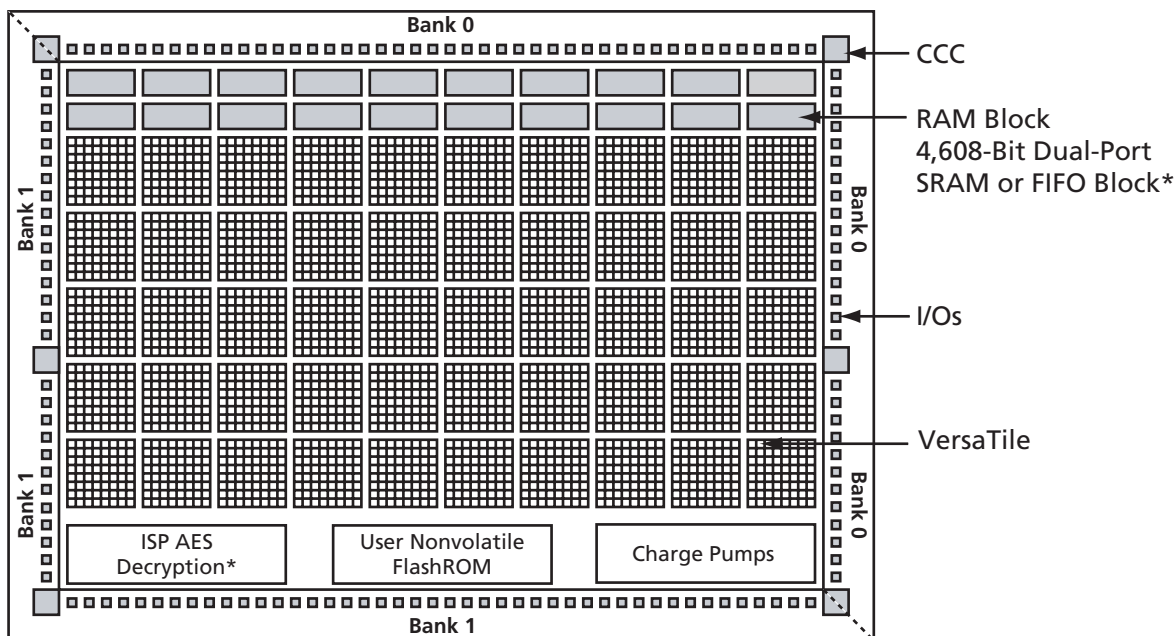
The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1 and Figure 2 on page 7):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory¹
- Extensive CCCs and PLLs¹
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate Flash switch interconnections. The versatility of the ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3 devices via an IEEE 1532 JTAG interface.

1. The A3P030 does not support PLL or SRAM.



Note: *Not supported by AGL030

Figure 1 • ProASIC3 Device Architecture Overview with Two I/O Banks (A3P030, A3P060, and A3P125)

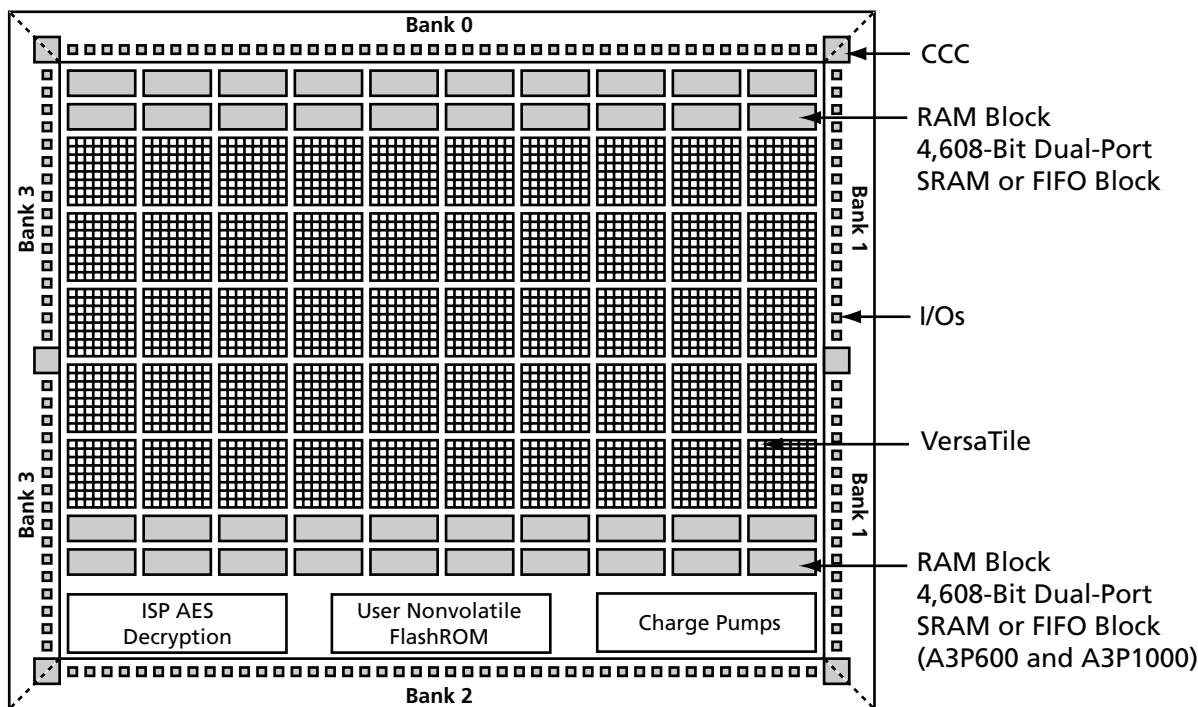


Figure 2 • ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250, A3P600, and A3P1000)

VersaTiles

The ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 3](#) for VersaTile configurations.

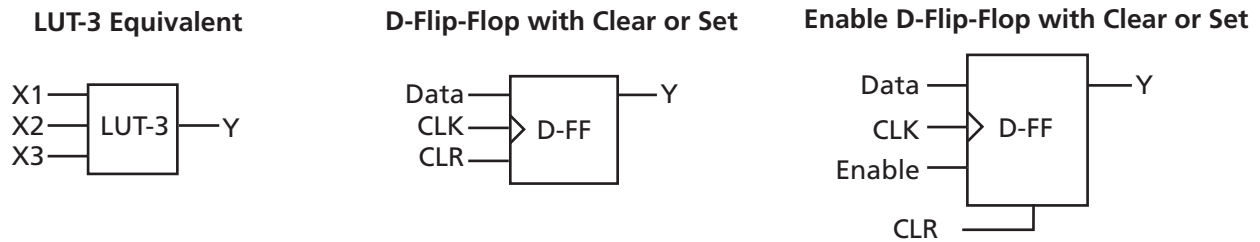


Figure 3 • VersaTile Configurations

User Nonvolatile FlashROM

Actel ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P030 device), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis

using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3 development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P030 device) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the A3P030 device).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P030 does not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from -7.56 ns to $+11.12$ ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0° , 90° , 180° , and 270° . Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = $50\% \pm 1.5\%$ or better (for PLL only)
- Low output jitter: worst case $< 2.5\% \times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = 300 μ s (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps \times (350 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, BLVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, BLVDS and M-LVDS. BLVDS and M-LVDS can support up to 20 loads.

Related Documents

Application Notes

ProASIC3/E I/O Usage Guide

http://www.actel.com/documents/PA3_E_IO_AN.pdf

In-System Programming (ISP) in ProASIC3/E Using FlashPro3

http://www.actel.com/documents/PA3_E_ISP_AN.pdf

ProASIC3/E FlashROM

http://www.actel.com/documents/PA3_E_FROM_AN.pdf

ProASIC3/E Security

http://www.actel.com/documents/PA3_E_Security_AN.pdf

ProASIC3/E SRAM/FIFO Blocks

http://www.actel.com/documents/PA3_E_SRAMFIFO_AN.pdf

Programming a ProASIC3/E Using a Microprocessor

http://www.actel.com/documents/PA3_E_Microprocessor_AN.pdf

UJTAG Applications in ProASIC3/E Devices

http://www.actel.com/documents/PA3_E_UJTAG_AN.pdf

Using DDR for ProASIC3/E Devices

http://www.actel.com/documents/PA3_E_DDR_AN.pdf

Using Global Resources in Actel ProASIC3/E Devices

http://www.actel.com/documents/PA3_E_Global_AN.pdf

Power-Up/Down Behavior of ProASIC3/E Devices

http://www.actel.com/documents/ProASIC3_E_PowerUp_AN.pdf

For additional ProASIC3 application notes, go to <http://www.actel.com/techdocs/an.aspx>.

User's Guides

SmartGen Cores Reference Guide

http://www.actel.com/documents/genguide_ug.pdf

Designer User's Guide

http://www.actel.com/documents/designer_ug.pdf

ProASIC3/E Macro Library Guide

http://www.actel.com/documents/pa3_libguide_ug.pdf

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