

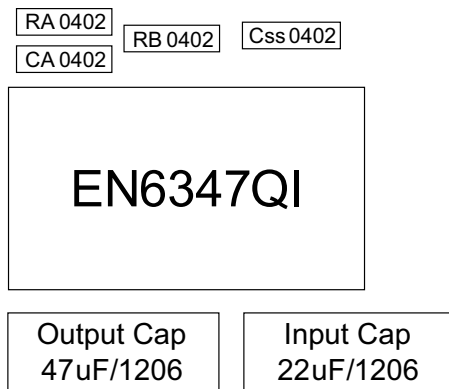
### Description

The EN6347QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal circuits, compensation, and the inductor in an advanced 4mm x 7mm QFN package.

The EN6347QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architecture. The device's advanced circuit techniques, ultra high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.



**Figure 1:** Total Solution Footprint PWM mode  
(Not to scale) Total Area  $\approx 75 \text{ mm}^2$

### Features

- Integrated Inductor, MOSFETS, Controller
- Minimal external components.
- Up to 4A Continuous Output Current Capability.
- 3 MHz operating frequency. Switching frequency can be phase locked to an external clock.
- High efficiency, up to 95%.
- Wide input voltage range of 2.5V to 6.6V.
- Light Load Mode with programmable set point.
- Output Enable pin and Power OK signal.
- Programmable soft-start time.
- Under Voltage Lockout, Over Current, Short Circuit and Thermal Protection.
- RoHS compliant, MSL level 3, 260C reflow.

### Applications

- Point of load regulation for processors, DSPs, FPGAs, and ASICs
- Noise sensitive applications such as A/V, RF and Gbit I/O
- Low voltage, distributed power architectures such as 0.8V, 1.0V, 1.2, 2.5V, 3.3V, 5V rails
- Blade servers, RAID storage systems, LAN/SAN adapter cards, wireless base stations, industrial automation, test and measurement, embedded computing, communications, and multi-function printers.
- Ripple sensitive applications
- Beat frequency sensitive applications

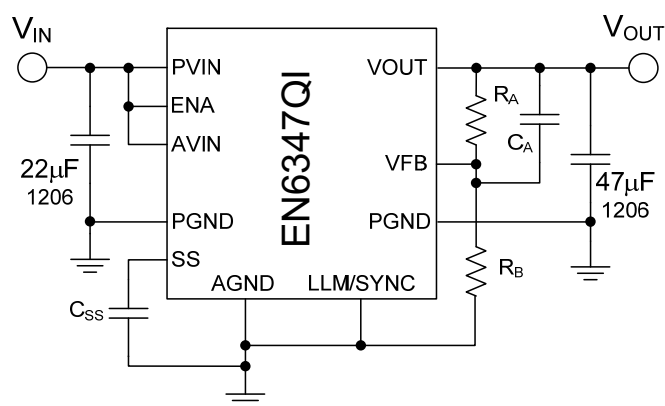
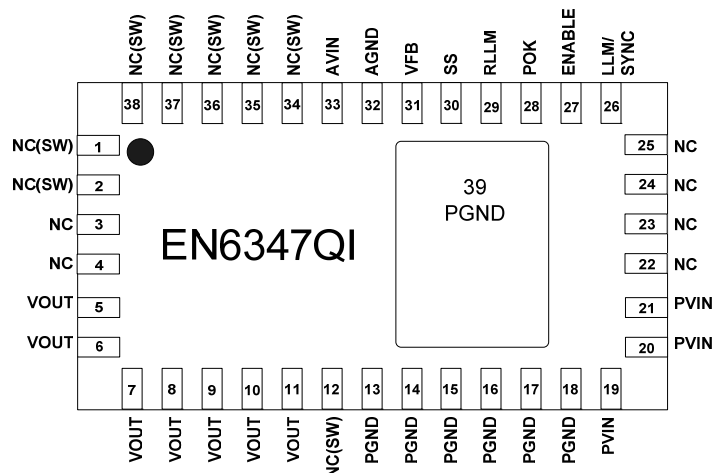


Figure 2: Typical Application Schematic (PWM mode)

## Pin Assignments (Top View)

Figure 3: Pinout Diagram (Top View)  
NOTE: All pins must be soldered to PCB.

## Ordering Information

| Part Number | Temp Rating (°C) | Package              |
|-------------|------------------|----------------------|
| EN6347QI    | -40 to +85       | 38-pin QFN T&R       |
| EN6347QI3   | -40 to +85       | 38-pin QFN T&R       |
| EN6347QI-E  |                  | QFN Evaluation Board |

## Pin Description

| PIN            | NAME     | FUNCTION  |
|----------------|----------|---|
| 1-2, 12, 34-38 | NC(SW)   | NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.   |
| 3-4, 22-25     | NC       | NO CONNECT – These pins may be internally connected. Do not connect to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.  |
| 5-11           | VOUT     | Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 13-15.   |
| 13-18          | PGND     | Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.   |
| 19-21          | PVIN     | Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 16-18.  |
| 26             | LLM/SYNC | Dual function pin providing LLM Enable and External Clock Synchronization (see Application Section). At static Logic HIGH, device will allow automatic engagement of light load mode. At static logic LOW, the device is forced into PWM only. A clocked input to this pin will synchronize the internal switching frequency to the external signal. If this pin is left floating, it will pull to a static logic high, enabling LLM. |
| 27             | ENABLE   | Input Enable. Applying logic high enables the output and initiates a soft-start. Applying logic low disables the output.  |
| 28             | POK      | Power OK is an open drain transistor used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal.  |
| 29             | RLLM     | Programmable LLM engage resistor to AGND allows for adjustment of load current at which Light-Load Mode engages. Can be left open for PWM only operation.   |
| 30             | SS       | Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time.  |
| 31             | VFB      | External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The midpoint of the divider is connected to VFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop.   |
| 32             | AGND     | Analog Ground. This is the controller ground return. Connect to a quiet ground.   |
| 33             | AVIN     | Input power supply for the controller. Connect to input voltage at a quiet point.   |
| 39             | PGND     | Device thermal pad to be connected to the system GND plane. See Layout Recommendations section.   |

## Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

| PARAMETER                                  | SYMBOL          | MIN  | MAX            | UNITS |
|--|-----------------|------|----------------|-------|
| Supply Voltage – PVIN, AVIN, VOUT          | $V_{IN}$        | -0.5 | 7.0            | V     |
| Pin Voltages – ENABLE, POK, LLM/SYNC       |                 | -0.5 | $V_{IN} + 0.3$ | V     |
| Pin Voltages – VFB, SS, RLLM               |                 | -0.5 | 2.75           | V     |
| Storage Temperature Range                  | $T_{STG}$       | -65  | 150            | °C    |
| Maximum Operating Junction Temperature     | $T_{J-ABS Max}$ |      | 150            | °C    |
| Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A |                 |      | 260            | °C    |
| ESD Rating - all pins (based on HBM)       |                 |      | 2000           | V     |

## Recommended Operating Conditions

| PARAMETER                                  | SYMBOL     | MIN  | MAX | UNITS |
|--|------------|------|-----|-------|
| Input Supply Voltage                       | $V_{IN}$   | 2.5  | 6.6 | V     |
| Operating Junction Temperature             | $T_{J-OP}$ | - 40 | 125 | °C    |
| Operating Ambient Temperature              | $T_{AMB}$  | - 40 | 85  | °C    |
| Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A |            |      | 260 | °C    |

## Thermal Characteristics

| PARAMETER   | SYMBOL        | MIN | TYP | MAX | UNITS |
|---|---------------|-----|-----|-----|-------|
| Thermal Shutdown  | $T_{SD}$      |     | 160 |     | °C    |
| Thermal Shutdown Hysteresis                               | $T_{SDH}$     |     | 35  |     | °C    |
| Thermal Resistance: Junction to Ambient ( <b>Note 1</b> ) | $\theta_{JA}$ |     | 30  |     | °C/W  |
| Thermal Resistance: Junction to Case                      | $\theta_{JC}$ |     | 3   |     | °C/W  |

**Note 1:** Based on 2oz. external copper layers and proper thermal design in line with EIA/JEDEC JESD51-7 standard for high thermal conductivity boards.

## Electrical Characteristics

NOTE:  $V_{IN}=6.6V$  over operating temperature range unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ .

| PARAMETER                                      | SYMBOL               | TEST CONDITIONS   | MIN             | TYP          | MAX             | UNITS            |
|--|----------------------|---|-----------------|--------------|-----------------|------------------|
| Operating Input Voltage                        | $V_{IN}$             |   | 2.5             |              | 6.6             | V                |
| Under Voltage Lock-out – $V_{IN}$ Rising       | $V_{UVLOR}$          | Voltage above which UVLO is not asserted  |                 | 2.3          |                 | V                |
| Under Voltage Lock-out – $V_{IN}$ Falling      | $V_{UVLOF}$          | Voltage below which UVLO is asserted  |                 | 2.075        |                 | V                |
| Shut-Down Supply Current                       | $I_S$                | ENABLE=0V   |                 | 100          |                 | $\mu A$          |
| Operating Quiescent Current                    | $I_Q$                | LLM/SYNC = High   |                 | 650          |                 | $\mu A$          |
| Feedback Pin Voltage<br>EN6347QI<br>EN6347QI3  | $V_{FB}$             | Feedback node voltage at:<br>$V_{IN} = 5V, I_{LOAD} = 0, T_A = 25^{\circ}C$   | 0.7425<br>0.735 | 0.75<br>0.75 | 0.7575<br>0.765 | V                |
| Feedback Pin Voltage<br>EN6347QI<br>EN6347QI3  | $V_{FB}$             | Feedback node voltage at:<br>$2.5V \leq V_{IN} \leq 6.6V$<br>$0A \leq I_{LOAD} \leq 4A, T_A = -40 \text{ to } 85^{\circ}C$  | 0.735<br>0.7275 | 0.75<br>0.75 | 0.765<br>0.7725 | V                |
| Feedback pin Input Leakage Current (Note 1)    | $I_{FB}$             | VFB pin input leakage current   | -5              |              | 5               | nA               |
| $V_{OUT}$ Rise Time (Note 1)                   | $t_{RISE}$           | Measured from when $V_{IN} > V_{UVLOR}$ & ENABLE pin voltage crosses its logic high threshold to when $V_{OUT}$ reaches its final value. $C_{SS} = 15 \text{ nF}$ | 0.9             | 1.2          | 1.5             | ms               |
| Soft Start Capacitor Range                     | $C_{SS\_RANGE}$      |   | 10              |              | 68              | nF               |
| Output Drop Out Voltage<br>Resistance (Note 1) | $V_{DO}$<br>$R_{DO}$ | $V_{INMIN} - V_{OUT}$ at Full load<br>Input to Output Resistance  |                 | 240<br>60    | 360<br>90       | mV<br>m $\Omega$ |
| Continuous Output Current                      | $I_{OUT}$            | PWM mode<br>LLM mode (Note 2)   | 0<br>0.002      |              | 4<br>4          | A                |
| Over Current Trip Level                        | $I_{OCP}$            | $V_{IN} = 5V, V_{OUT} = 1.2V$   |                 | 6.5          |                 | A                |
| Disable Threshold                              | $V_{DISABLE}$        | ENABLE pin logic low.   | 0.0             |              | 0.6             | V                |
| ENABLE Threshold                               | $V_{ENABLE}$         | ENABLE pin logic high<br>$2.5V \leq V_{IN} \leq 6.6V$   | 1.8             |              | $V_{IN}$        | V                |
| ENABLE Lockout Time                            | $T_{ENLOCKOUT}$      |   |                 | 3.2          |                 | ms               |
| ENABLE pin Input Current (Note 1)              | $I_{ENABLE}$         | ENABLE pin has $\sim 180k\Omega$ pull down  |                 | 40           |                 | $\mu A$          |
| Switching Frequency (Free Running)             | $F_{SW}$             | Free Running frequency of oscillator  |                 | 3            |                 | MHz              |
| External SYNC Clock Frequency Lock Range       | $F_{PLL\_LOCK}$      | Range of SYNC clock frequency   | 2.7             |              | 3.3             | MHz              |
| SYNC Input Threshold – Low (LLM/SYNC PIN)      | $V_{SYNC\_LO}$       | SYNC Clock Logic Level  |                 |              | 0.8             | V                |
| SYNC Input Threshold – High (LLM/SYNC PIN)     | $V_{SYNC\_HI}$       | SYNC Clock Logic Level - (Note 3)   | 1.8             |              | 2.5             | V                |
| POK Threshold                                  | POK                  | Threshold voltage as a fraction of expected output voltage  |                 | 90           |                 | %                |

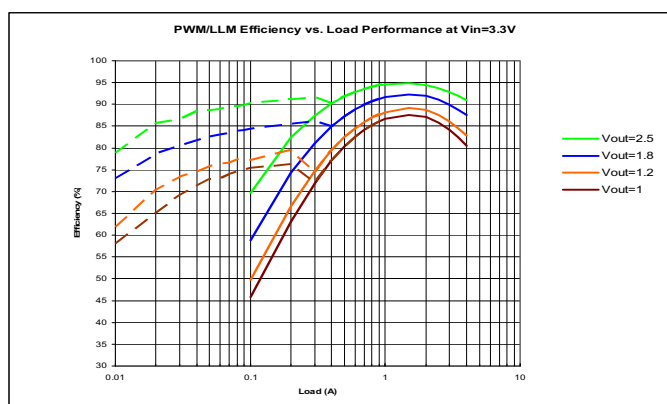
| PARAMETER                                 | SYMBOL        | TEST CONDITIONS   | MIN | TYP  | MAX      | UNITS   |
|---|---------------|---|-----|------|----------|---------|
| POK Output low Voltage                    | $V_{POKL}$    | With 4mA current sink into POK                          |     |      | 0.4      | V       |
| POK Output Hi Voltage                     | $V_{POKH}$    | $2.5V \leq V_{IN} \leq 6.6V$                            |     |      | $V_{IN}$ | V       |
| POK pin $V_{OH}$ leakage current (Note 1) | $I_{POKL}$    | POK high  |     |      | 1        | $\mu A$ |
| LLM Engage Headroom                       |               | Minimum $V_{IN}-V_{OUT}$ to ensure proper LLM operation |     | 800  |          | mV      |
| LLM Logic Low (LLM/SYNC PIN)              | $V_{LLM\_LO}$ | LLM Static Logic Level                                  |     |      | 0.3      | V       |
| LLM Logic High (LLM/SYNC PIN)             | $V_{LLM\_HI}$ | LLM Static Logic Level                                  | 1.5 |      |          | V       |
| LLM/SYNC Pin Current                      |               | LLM/SYNC Pin is <2.5V                                   |     | <100 |          | nA      |

**Note 1:** Parameter guaranteed by design.

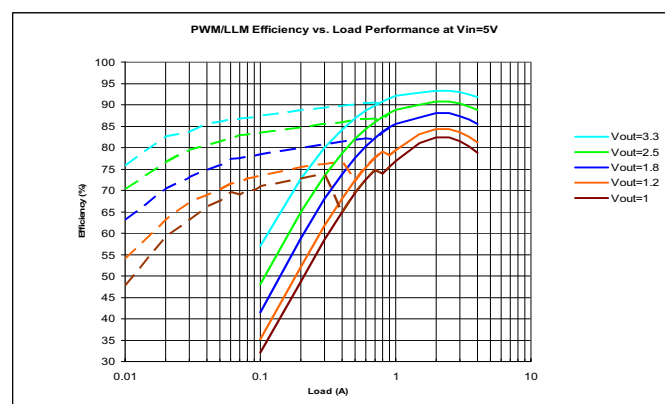
**Note 2:** LLM operation is normally only guaranteed above the minimum specified output current. Contact Enpirion Applications support for designs that need to operate at a lower  $I_{OUT}$ .

**Note 3:** For proper operation of the synchronization circuit, the high-level amplitude of the SYNC signal should not be above 2.5V.

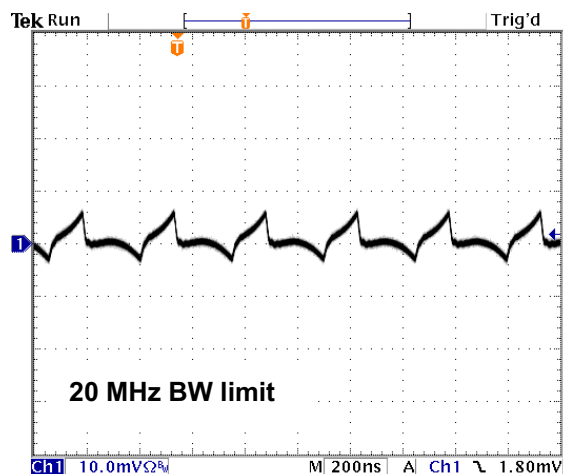
## Typical Performance Characteristics



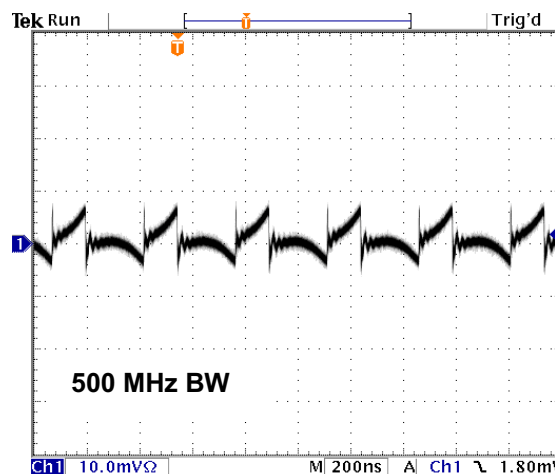
Efficiency  $V_{IN} = 3.3V$ ,  $V_{OUT}$  (From top to bottom) = 2.5, 1.8, 1.2, 1.0V



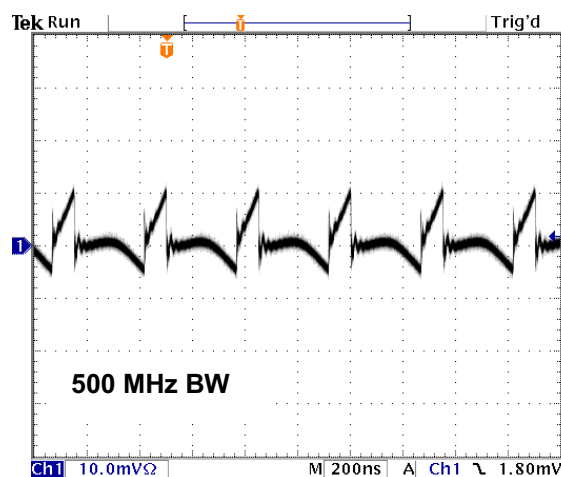
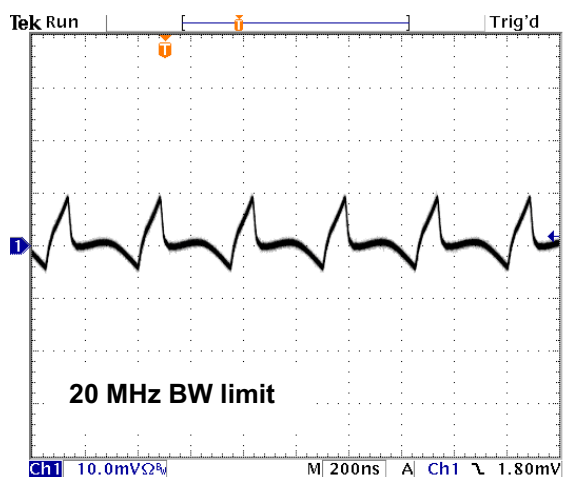
Efficiency  $V_{IN} = 5.0V$ ,  $V_{OUT}$  (From top to bottom) = 3.3, 2.5, 1.8, 1.0V



PWM Output Ripple:  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.0V$ ,  $I_{OUT} = 4A$   
 $C_{IN} = 22\mu F$ ,  $C_{OUT} = 47\mu F/1206 + 10\mu F/0805$

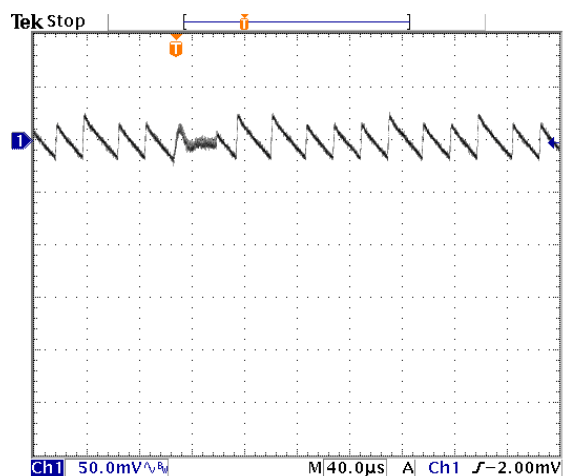


PWM Output Ripple:  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.0V$ ,  $I_{OUT} = 4A$   
 $C_{IN} = 22\mu F$ ,  $C_{OUT} = 47\mu F/1206 + 10\mu F/0805$



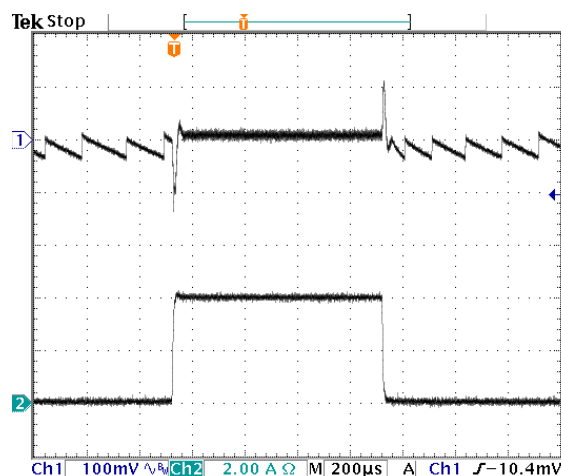
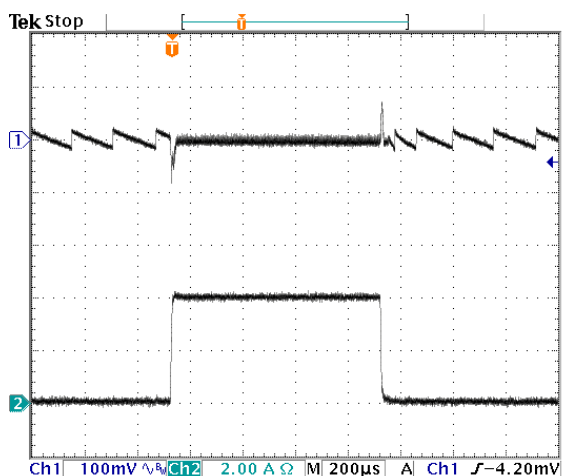
**PWM Output Ripple:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 1.0V$ ,  $I_{OUT} = 4A$   
 $C_{IN} = 22\mu F$ ,  $C_{OUT} = 47\mu F/1206 + 10\mu F/0805$**

**PWM Output Ripple:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 1.0V$ ,  $I_{OUT} = 4A$   
 $C_{IN} = 22\mu F$ ,  $C_{OUT} = 47\mu F/1206 + 10\mu F/0805$**



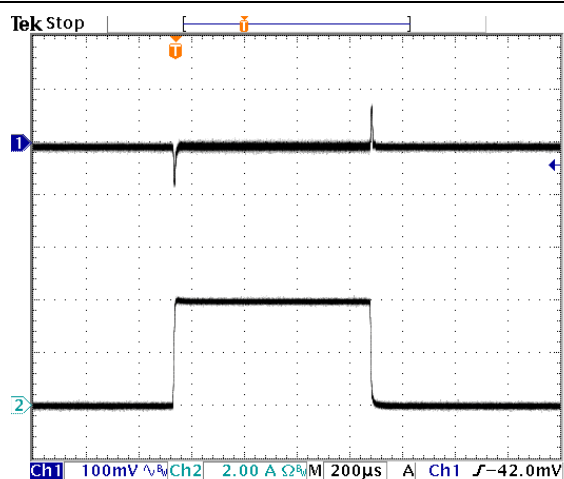
**LLM Output Ripple:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 1.0V$ ,  
 $I_{OUT} = 0.1A$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 2 \times 47\mu F/1206$**

**LLM Output Ripple:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 3.0V$ ,  
 $I_{OUT} = 0.1A$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 2 \times 47\mu F/1206$**

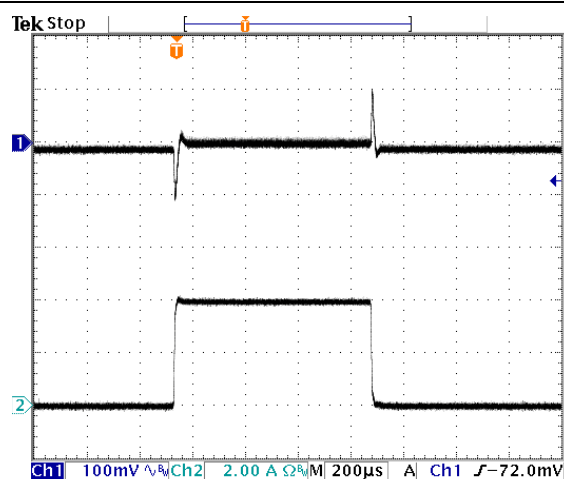


**Load Transient:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 1.0V$ , LLM Enabled  
 Ch.1:  $V_{OUT}$ , Ch.2:  $I_{OUT} = 0.01 \leftrightarrow 4A$   
 $C_{IN} = 22\mu F$ ,  $C_{OUT} = 2 \times 47\mu F/1206$**

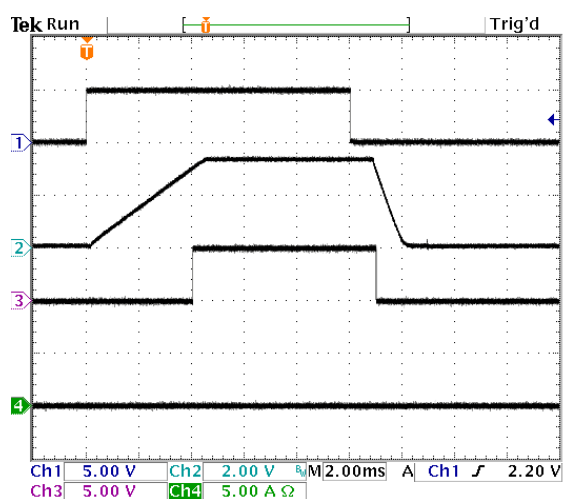
**Load Transient:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 3.0V$ , LLM Enabled  
 Ch.1:  $V_{OUT}$ , Ch.2:  $I_{OUT} = 0.01 \leftrightarrow 4A$   
 $C_{IN} = 22\mu F$ ,  $C_{OUT} = 2 \times 47\mu F/1206$**



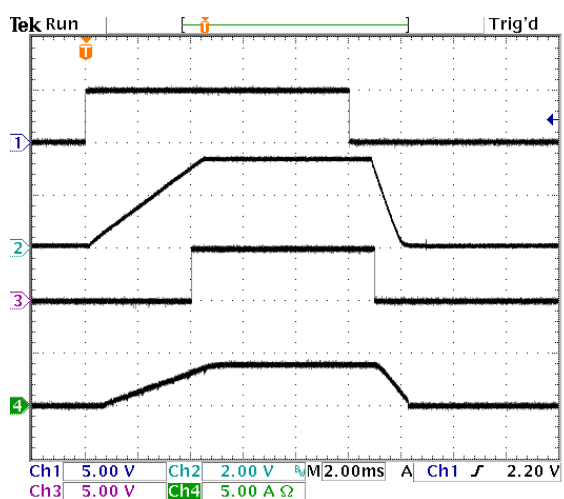
**PWM Load Transient:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 1.0V$**   
**Ch.1:  $V_{OUT}$ , Ch.2:  $I_{OUT} = 0 \leftrightarrow 4A$**   
 **$C_{IN} = 22\mu F$ ,  $C_{OUT} = 47\mu F/1206 + 10\mu F/0805$**



**PWM Load Transient:  $V_{IN} = 5.0V$ ,  $V_{OUT} = 3.0V$**   
**Ch.1:  $V_{OUT}$ , Ch.2:  $I_{OUT} = 0 \leftrightarrow 4A$**   
 **$C_{IN} = 22\mu F$ ,  $C_{OUT} = 47\mu F/1206 + 10\mu F/0805$**



**Power Up/Down at No Load:  $V_{IN}/V_{OUT} = 5V/3.3V$ ,**  
**47nF soft-start capacitor,  $C_{OUT} \approx 50\mu F$**   
**Ch.1: ENABLE, Ch. 2:  $V_{OUT}$ , Ch. 3: POK, Ch.4:  $I_{OUT}$**



**Power Up/Down into 0.825Ω load:  $V_{IN}/V_{OUT} = 5V/3.3V$ ,**  
**47nF soft-start capacitor,  $C_{OUT} \approx 50\mu F$**   
**Ch.1: ENABLE, Ch. 2:  $V_{OUT}$ , Ch. 3: POK, Ch.4:  $I_{OUT}$**

## Functional Block Diagram

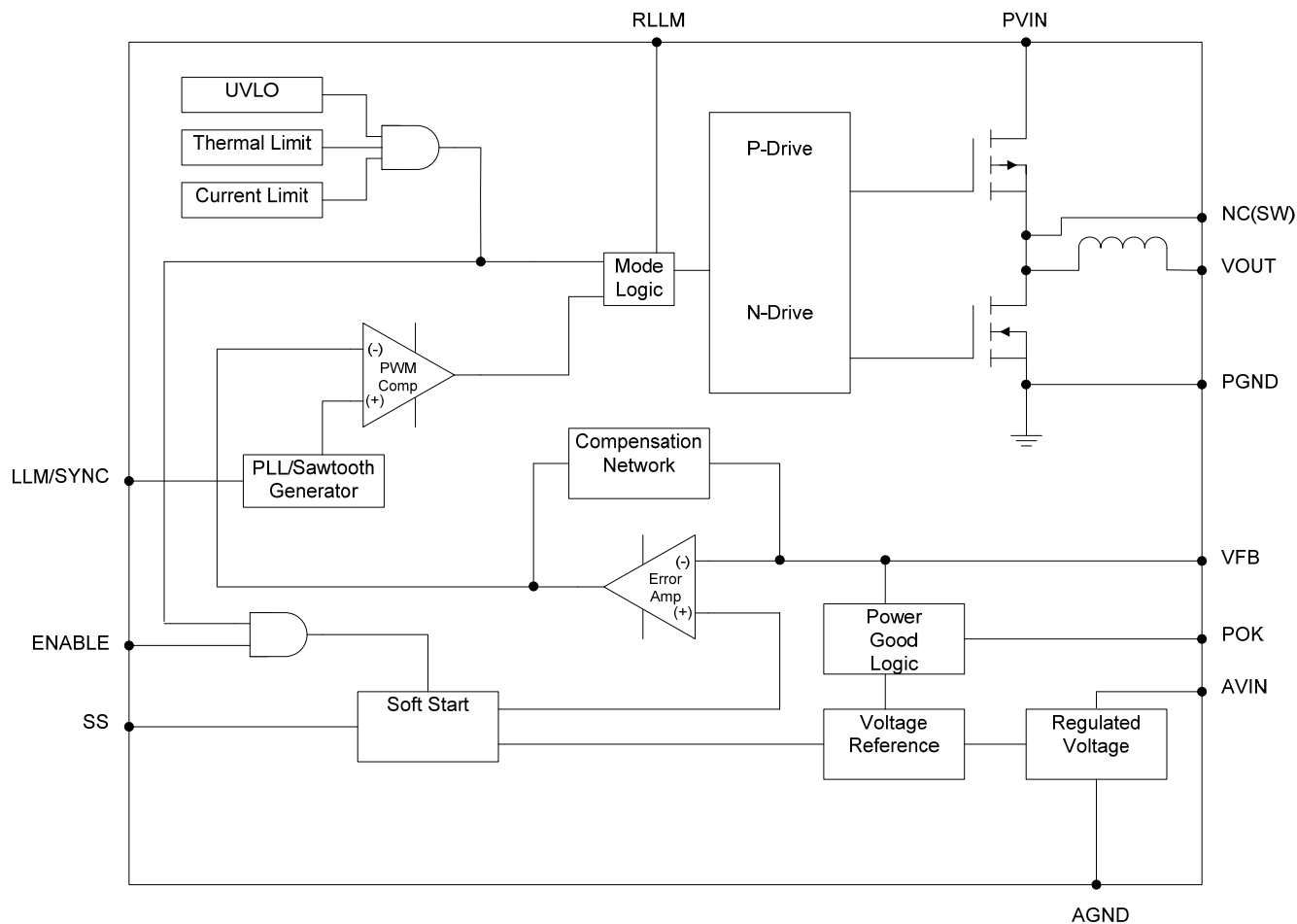


Figure 4: Functional Block Diagram

## Functional Description

### Synchronous Buck Converter

The EN6347QI is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.5V to 6.6V. The output voltage is programmed using an external resistor divider network. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the type III compensation network. The device uses a low-noise PWM topology and also integrates a unique light-load mode (LLM) to improve efficiency at light output load currents. LLM can be disabled with

a logic pin. Up to 4A of continuous output current can be drawn from this converter. The 3 MHz switching frequency allows the use of small size input / output capacitors, and enables wide loop bandwidth within a small footprint.

### Protection Features:

The power supply has the following protection features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Under-voltage lockout circuit to keep the converter output off while the input voltage is less than 2.3V.



## Additional Features:

- The switching frequency can be phase-locked to an external clock to eliminate or move beat frequency tones out of band.
- Soft-start circuit, allowing controlled startup when the converter is initially powered up. The soft start time is programmable with an appropriate choice of soft start capacitor.
- Power good circuit indicating  $V_{OUT}$  is greater than 90% of programmed value as long as the feedback loop is closed.
- To maintain high efficiency at low output current, the device incorporates automatic light load mode operation.

## Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. When the ENABLE pin is asserted (high) the device will undergo a normal soft start. A logic low on this pin will power the device down in a controlled manner. From the moment ENABLE goes low, there is a fixed lock out time before the output will respond to the ENABLE pin re-asserted (high). This lock out is activated for even very short logic low pulses on the ENABLE pin. See the Electrical Characteristics Table for technical specifications for this pin.

## LLM/SYNC Pin

This is a dual function pin providing LLM Enable and External Clock Synchronization. At static Logic HIGH, device will allow automatic engagement of light load mode. At static logic LOW, the device is forced into PWM only. A clocked input to this pin will synchronize the internal switching frequency – LLM mode is not available if this input is clocked.. If this pin is left floating, it will pull to a static logic high, enabling LLM.

## Frequency Synchronization

The switching frequency of the DC/DC converter can be phase-locked to an external clock source to move unwanted beat frequencies out of band. To avail this feature, the clock source should be connected to the LLM/SYNC pin. An activity detector recognizes

the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the clock frequency is in the range specified in the Electrical Characteristics Table. For proper operation of the synchronization circuit, the high-level amplitude of the SYNC signal should not be above 2.5V. Please note LLM is not available when synchronizing to an external frequency.

## Spread Spectrum Mode

The external clock frequency may be swept between the limits specified in the Electrical Characteristics Table at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

## Soft-Start Operation

During Soft-start, the output voltage is ramped up gradually upon start-up. The output rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (30) and the AGND pin (32).

$$\text{Rise Time: } T_R \approx (C_{SS} * 80k\Omega) \pm 25\%$$

During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10uA. Typical soft-start rise time is ~3.8ms with SS capacitor value of 47nF. The rise time is measured from when  $V_{IN} > V_{UVLOR}$  and ENABLE pin voltage crosses its logic high threshold to when  $V_{OUT}$  reaches its programmed value. Please note LLM function is disabled during the soft-start ramp-up time.

## POK Operation

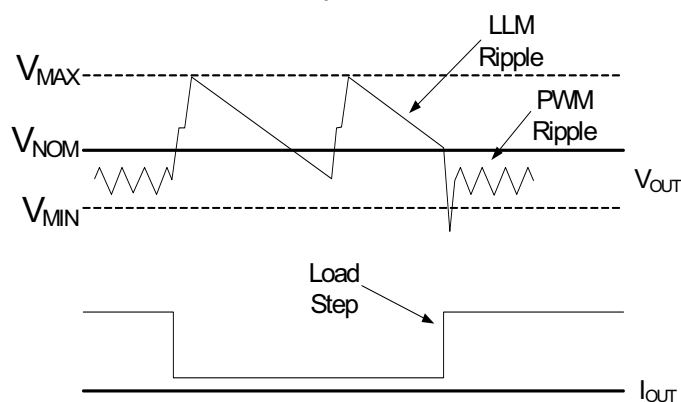
The POK signal is an open drain signal (requires a pull up resistor to  $V_{IN}$  or similar voltage) from the converter indicating the output voltage is within the specified range. The POK signal will be logic high ( $V_{IN}$ ) when the output voltage is above 90% of programmed  $V_{OUT}$ . If the output voltage goes below this threshold, the POK signal will be logic low.

## Light Load Mode (LLM) Operation

The EN6347QI uses a proprietary light load mode to provide high efficiency at low output currents. When the LLM/SYNC pin is high, the device is in automatic LLM “Detection” mode. When the LLM/SYNC pin is low, the device is forced into PWM mode. In automatic LLM “Detection” mode, when a light load condition is detected, the device will:

- (1) Step  $V_{OUT}$  up by approximately 1.0% above the nominal operating output voltage setting,  $V_{NOM}$  and as low as -0.5% below  $V_{NOM}$ , and then
- (2) Shut down unnecessary circuitry, and then
- (3) Monitor  $V_{OUT}$ .

When  $V_{OUT}$  falls below  $V_{NOM}$ , the device will repeat (1), (2), and (3). The voltage step up, or pre-positioning, improves transient droop when a load transient causes a transition from LLM mode to PWM mode. If a load transient occurs, causing  $V_{OUT}$  to fall below the threshold  $V_{MIN}$ , the device will exit LLM operation and begin normal PWM operation. Figure 5 demonstrates  $V_{OUT}$  behavior during transition into and out of LLM operation.



**Figure 5.**  $V_{OUT}$  behavior in LLM operation.

Many multi-mode DCDC converters suffer from a condition that occurs when the load current increases only slowly so that there is no load transient driving  $V_{OUT}$  below the  $V_{MIN}$  threshold. In this condition, the device would never exit LLM operation. This could adversely affect efficiency and cause unwanted ripple. To prevent this from occurring, the EN6347QI periodically exits LLM mode into PWM mode and measures the load current. If the load current is above the LLM threshold current, the

device will remain in PWM mode. If the load current is below the LLM threshold, the device will re-enter LLM operation. There may be a small overshoot or undershoot in  $V_{OUT}$  when the device exits and re-enters LLM.

The load current at which the device will enter LLM mode is a function of input and output voltage, and the RLLM pin resistor. Contact Enpirion Applications support for details regarding the optimization of this resistor for specific operating conditions. For PWM only operation, the RLLM pin can be left open.

To ensure normal LLM operation, LLM mode should be enabled and disabled with specific sequencing. For applications with explicit LLM pin control, enable LLM after  $V_{IN}$  ramp up is complete. For applications with only ENABLE control, tie LLM to ENABLE; and enable the device after  $V_{IN}$  ramp up is complete. For designs with ENABLE and LLM tied to  $V_{IN}$ , make sure the device soft-start time is longer than the  $V_{IN}$  ramp-up time. LLM will start operating after the soft-start time is completed.

**NOTE:** For proper LLM operation the EN6347QI requires a minimum difference between  $V_{IN}$  and  $V_{OUT}$ , and a minimum LLM load requirement as specified in the Electrical Characteristics Table. For LLM designs requiring lower voltage headroom or a lower minimum load, contact Enpirion Applications support.

## Over-Current Protection

The current limit function is achieved by sensing the current flowing through the Power PFET. When the sensed current exceeds the over current trip point, both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed, the over-current protection circuit will enable normal PWM operation. If the over-current condition persists, the soft start capacitor will gradually discharge causing the output voltage to fall. When the OCP fault is removed, the output voltage will ramp back up to the desired voltage. This circuit is designed to provide high noise immunity.

## Thermal Overload Protection

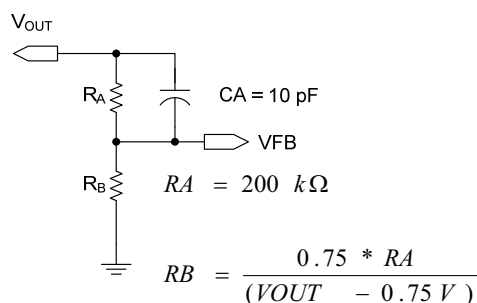
Thermal shutdown circuit will disable device operation when the Junction temperature exceeds approximately 150°C. After a thermal shutdown event, when the junction temperature drops by approx 20°C, the converter will re-start with a normal soft-start.

## Input Under-Voltage Lock-Out

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis and input de-glitch circuits ensure high noise immunity and prevent false UVLO triggers.

## Application Information

The EN6347QI output voltage is programmed using a simple resistor divider network. Figure 6 shows the resistor divider configuration.



**Figure 6:  $V_{OUT}$  Resistor Divider & Compensation Capacitor**

An additional compensation capacitor  $C_A$  is also required in parallel with the upper resistor.

## Input Capacitor Selection

The EN6347QI requires about 20 $\mu$ F of input capacitance. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling.

## Compensation

The EN6347QI uses a type 3 compensation network. As noted earlier, a piece of the compensation network is the phase lead capacitor  $C_A$  in Figure 6. This network is optimized for use with about 50-100 $\mu$ F of output capacitance and will provide wide loop bandwidth and excellent transient performance for most applications. Voltage mode operation provides high noise immunity at light load.

In some applications modifications to the compensation may be required. For more information, contact Enpirion Applications Engineering support.

## Recommended Input Capacitors

| Description  | MFG         | P/N                |
|--|-------------|--------------------|
| 10 $\mu$ F, 10V, 10%<br>X7R, 1206<br>(2 capacitors needed) | Murata      | GRM31CR71A106KA01L |
|  | Taiyo Yuden | LMK316B7106KL-T    |
| 22 $\mu$ F, 10V, 20%<br>X5R, 1206<br>(1 capacitor needed)  | Murata      | GRM31CR61A226ME19L |
|  | Taiyo Yuden | LMK316BJ226ML-T    |

## Output Capacitor Selection

The EN6347QI has been nominally optimized for use with approximately 50-100 $\mu$ F of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as  $Z$ , is comprised of effective series resistance, ESR, and effective series inductance, ESL:

$$Z = \text{ESR} + \text{ESL}$$

Placing output capacitors in parallel reduces the impedance and will hence result in lower PWM ripple voltage. In addition, higher output capacitance will improve overall regulation and ripple in light-load mode.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \dots + \frac{1}{Z_n}$$

## Typical PWM Ripple Voltages

| Output Capacitor Configuration | Typical Output Ripple (mVp-p)<br>(as measured on EN6347QI Evaluation Board)* |
|--------------------------------|--|
| 1 x 47 $\mu$ F                 | 25   |
| 47 $\mu$ F + 10 $\mu$ F        | 15   |

\* Note: 20 MHz BW limit

## Recommended Output Capacitors

| Description   | MFG         | P/N                |
|---|-------------|--------------------|
| 47 $\mu$ F, 6.3V, 20%<br>X5R, 1206<br>(1 or 2 capacitors needed)                              | Murata      | GRM31CR60J476ME19L |
|   | Taiyo Yuden | JMK316BJ476ML-T    |
| 10 $\mu$ F, 10V, 10%<br>X5R, 1206<br>(Optional 1 capacitor in parallel with 47 $\mu$ F above) | Murata      | GRM31CR71A106KA01L |
|   | Taiyo Yuden | LMK316BJ226ML-T    |

For best LLM performance, we recommend using just 2x47 $\mu$ F capacitors mentioned in the above table, and no 10 $\mu$ F capacitor.

The  $V_{OUT}$  sense point should be just after the last output filter capacitor right next to the device. Additional bulk output capacitance

## Thermal Considerations

The Enpirion EN6347QI DC-DC converter is packaged in a 7x4x1.85mm 38-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C will reduce long-term reliability. The device has a thermal overload protection circuit designed to shut it off at a junction temperature specified in the Electrical Characteristics Table.

The silicon is mounted on a copper thermal pad that is exposed at the bottom of the package. The thermal resistance from the silicon to the exposed thermal pad is very low. In order to take advantage of this low resistance, the exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB). The PCB then acts as a heat sink. In order for the PCB to be an effective heat sink, the device thermal pad should be coupled to copper ground planes or special heat sink structures designed into the PCB (refer to the Layout Recommendations section).

beyond the above recommendations can be used on the output node of the EN6347QI as long as the bulk capacitors are far enough from the  $V_{OUT}$  sense point such that they don't interfere with the control loop operation.

In some cases modifications to the compensation or output filter capacitance may be required to optimize device performance such as transient response, ripple, or hold-up time. The EN6347QI provides the capability to modify the control loop response to allow for customization for such applications. For more information, contact Enpirion Applications Engineering support.

## Power-Up Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. Tying all three pins together meets these requirements.

The junction temperature,  $T_J$ , is calculated from the ambient temperature,  $T_A$ , the device power dissipation,  $P_D$ , and the device junction-to-ambient thermal resistance,  $\theta_{JA}$  in °C/W, as follows:

$$T_J = T_A + (P_D) (\theta_{JA})$$

The junction temperature,  $T_J$ , can also be expressed in terms of the device case temperature,  $T_C$ , and the device junction-to-case thermal resistance,  $\theta_{JC}$  in °C/W, as follows:

$$T_J = T_C + (P_D) (\theta_{JC})$$

The device case temperature,  $T_C$ , is the temperature at the center of the exposed thermal pad at the bottom of the package.

The device junction-to-ambient and junction-to-case thermal resistances,  $\theta_{JA}$  and  $\theta_{JC}$ , are shown in the Thermal Characteristics Table. The  $\theta_{JC}$  is a function of the device and the QFN package design. The  $\theta_{JA}$  is a function of  $\theta_{JC}$  and the user's system design parameters that include the thermal effectiveness of the customer PCB and airflow.

The  $\theta_{JA}$  value shown in the Thermal Characteristics table on page 3 is for free convection with the device heat sunk (through the thermal pad) to a copper plated four-layer PC board with a full ground and a full power plane following EIA/JEDEC JESD51-7

Standard. The  $\theta_{JA}$  can be reduced with the use of forced air convection. Because of the strong dependence on the thermal effectiveness of the PCB and the system design, the actual  $\theta_{JA}$  value will be a function of the specific application.

## Layout Recommendations

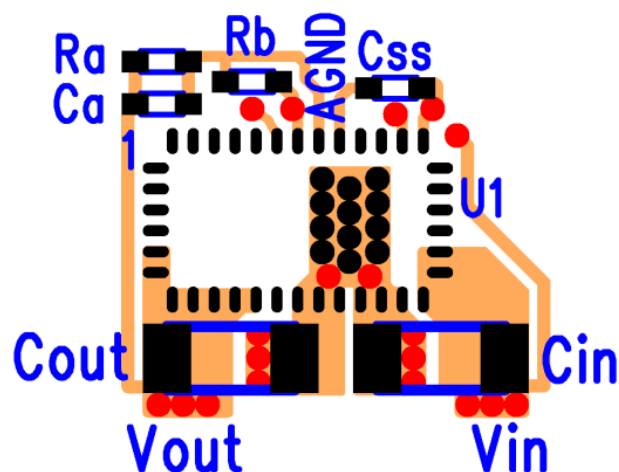
Figure 7 shows critical components and layer 1 traces of a recommended minimum footprint EN6347QI layout with ENABLE tied to  $V_{IN}$  in PWM mode. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Enpirion website [www.enpirion.com](http://www.enpirion.com) for exact dimensions and other layers. Please refer to this Figure while reading the layout recommendations in this section.

**Recommendation 1:** Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN6347QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN6347QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

**Recommendation 2:** Three PGND pins are dedicated to the input circuit, and three to the output circuit. The slit in Figure 7 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

**Recommendation 3:** The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Enpirion website [www.enpirion.com](http://www.enpirion.com).

**Recommendation 4:** The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible.



**Figure 7: Top PCB Layer Critical Components and Copper for Minimum Footprint**

The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figures: 7, 8, and 9.

**Recommendation 5:** Multiple small vias (the same size as the thermal via discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 7. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under  $C_{IN}$  and  $C_{OUT}$ , then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

**Recommendation 6:** AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 7 this connection is made at the input capacitor close to the  $V_{IN}$  connection.

**Recommendation 7:** The layer 1 metal under the device must not be more than shown in Figure 7. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

**Recommendation 8:** The  $V_{OUT}$  sense point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

**Recommendation 9:** Keep  $R_A$ ,  $C_A$ , and  $R_B$  close to the VFB pin (see Figures 6 and 7). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect  $R_B$  directly to the AGND pin instead of going through the GND plane.

## Design Considerations for Lead-Frame Based Modules

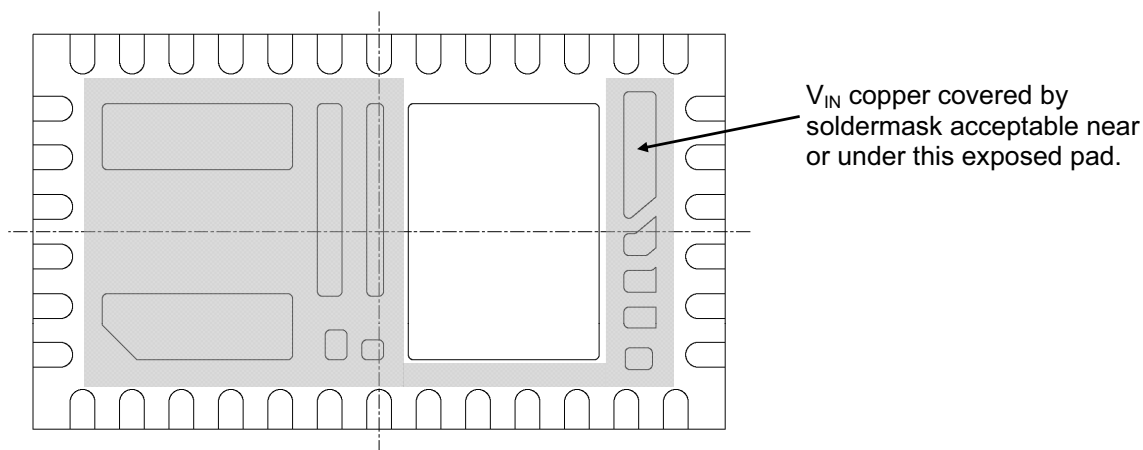
### Exposed Metal on Bottom of Package

Lead frames offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in

several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be soldered to the PC board. The PCB top layer under the EN6347QI should be clear of any metal except for the large thermal pad. The “grayed-out” region in Figure 8 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.



**Figure 8: Lead-Frame Exposed Metal.** Grey area highlights exposed metal below which there should not be any metal (traces, vias, or planes) on the top layer of PCB.

## Recommended PCB Footprint

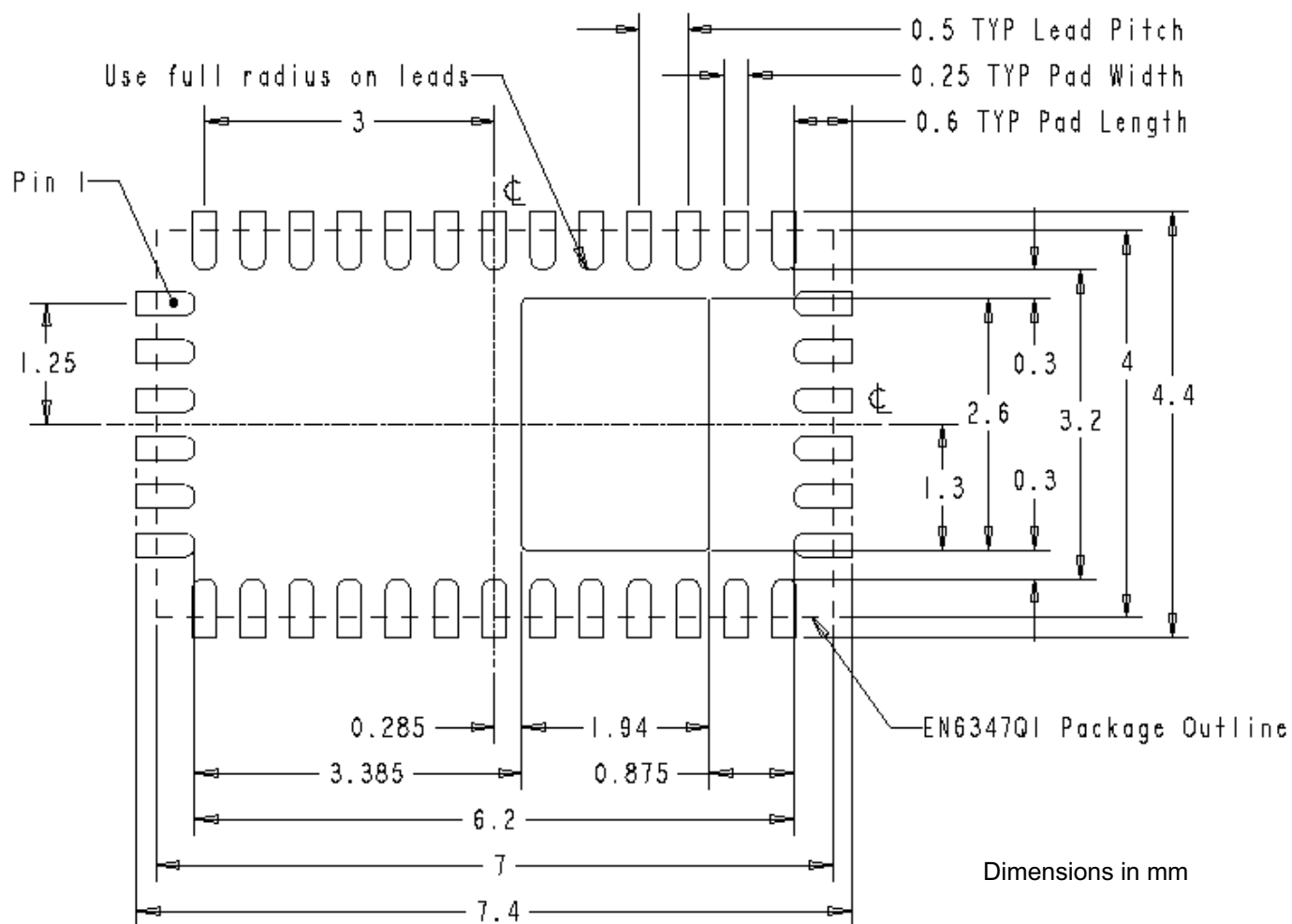


Figure 9: EN6347QI Package PCB Footprint

## Package and Mechanical

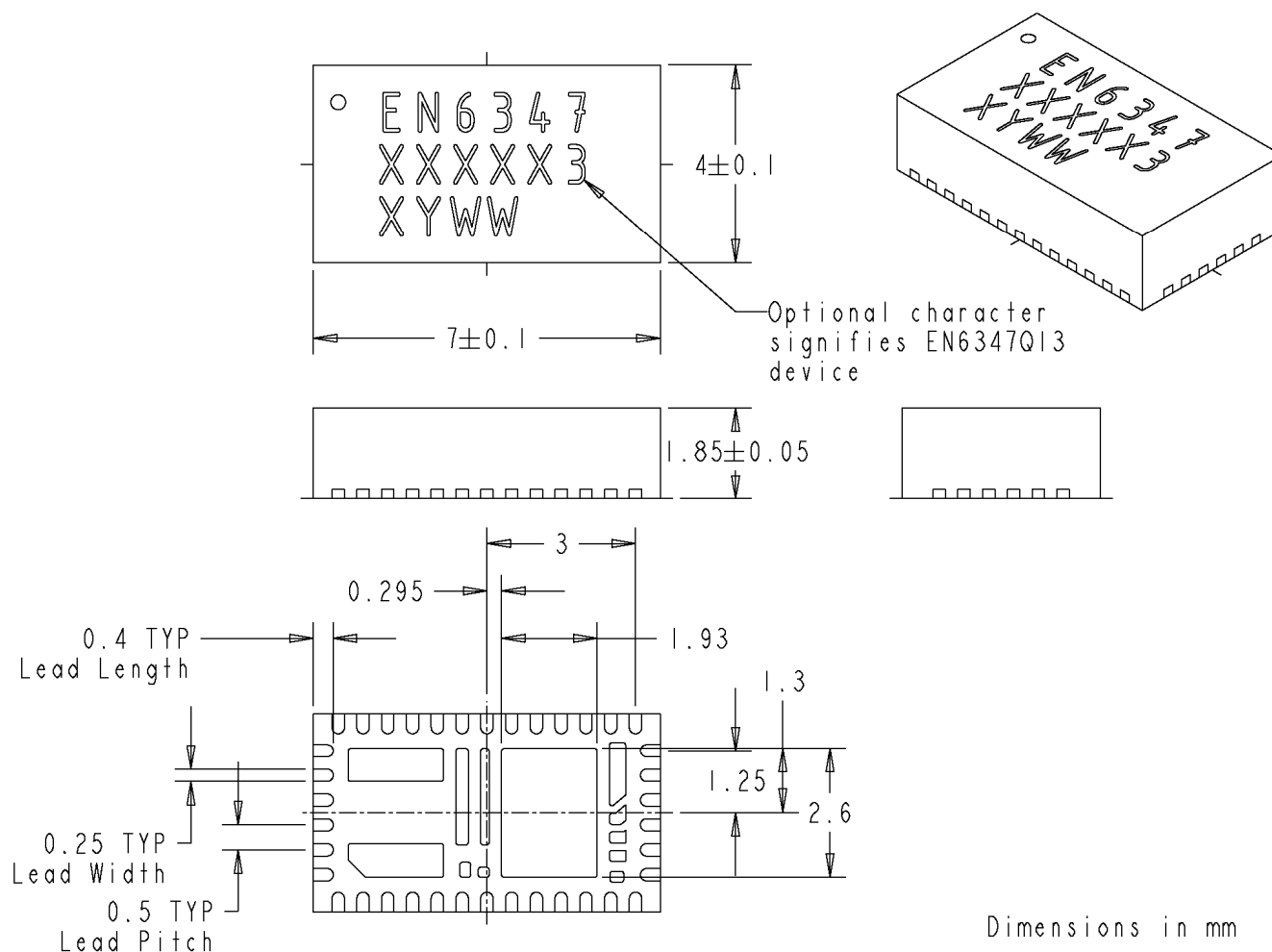


Figure 10: EN6347QI Package Dimensions

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