

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7MPB9307FT/FK

## Low Voltage/Low Power 8-Bit Dual Supply Bus Switch

The TC7MPB9307 is a CMOS 8-bit dual-supply bus switch that can provide an interface between two nodes at different voltage levels.

The TC7MPB9307 can be connected to two independent power supplies.  $V_{CCA}$  supports 1.8-V, 2.5-V and 3.3-V power supplies, whereas  $V_{CCB}$  supports 2.5-V, 3.3-V and 5.0V power supplies.

Bidirectional level-shifting is possible by simply adding external pull-up resistors between the  $A_n/B_n$  data lines and the  $V_{CCA}/V_{CCB}$  supplies. There is no restriction on the relative magnitude of the  $A_n$  and  $B_n$  voltages; both the  $A_n$  and  $B_n$  data lines can be pulled up to arbitrary power supplies.

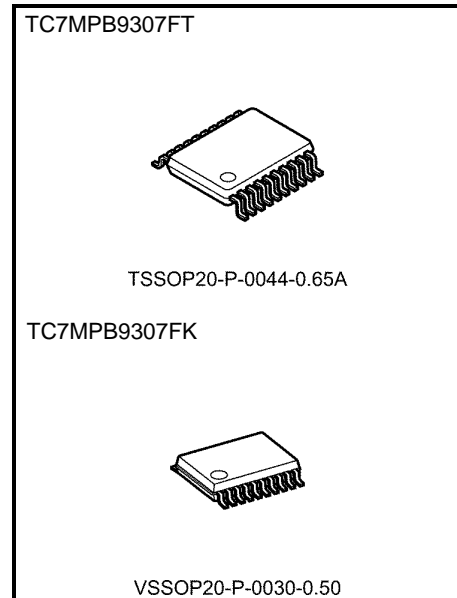
The Output Enable ( $\overline{OE}$ ) input controls the connection or isolation of two bus systems on the  $V_{CCA}$  and  $V_{CCB}$  sides.

The  $\overline{OE}$  input is common for all the eight bits of the data lines; thus the TC7MPB9307 is used as a single eight-bit bus switch. When  $\overline{OE}$  is Low, the switch is on, and  $A_n$  is connected to  $B_n$ . When  $\overline{OE}$  is High, the switch is open.

The TC7MPB9307 supports power-down protection at the  $\overline{OE}$  input, with  $\overline{OE}$  being 5.5-V tolerant.

The channels consist of n-type MOSFETs.

All the inputs provide protection against electrostatic discharge.



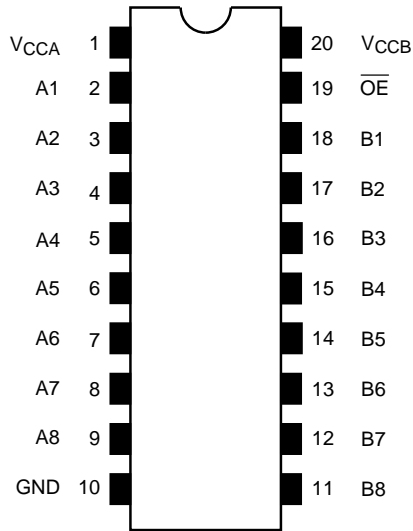
### Weight

TSSOP20-P-0044-0.65A	: 0.08 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

## Features

- Operating voltage: 1.8-V to 2.5-V, 1.8-V to 3.3-V, 1.8-V to 5.0-V, 2.5-V to 3.3-V, 2.3-V to 5.0-V or 3.3-V to 5.0-V bidirectional interface
- Operating voltage:  $V_{CCA} = 1.65$  to 5.0 V,  $V_{CCB} = 2.3$  to 5.5 V
- Low ON-resistance:  $R_{ON} = 5.0 \Omega$  (typ.)  
(ON-resistance test circuit:  $V_{IS} = 0$  V,  $I_{IS} = 30$  mA,  $V_{CCA} = 3.0$  V,  $V_{CCB} = 4.5$  V)
- ESD performance: Machine model  $\geq \pm 200$  V  
Human body model  $\geq \pm 2000$  V
- 5.5-V tolerance and power-down protection at the Output Enable input.
- Packages: TSSOP20, VSSOP(20)

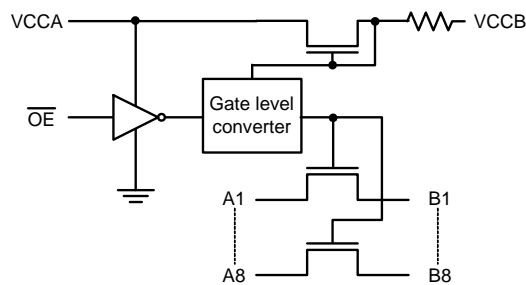
## Pin Assignment (top view)



## Truth Table

Inputs	Function
$\overline{OE}$	
L	A port = B port
H	Disconnect

## Circuit Schematic



**Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>CCA</sub>	-0.5 to 7.0	V
	V <sub>CCB</sub>	-0.5 to 7.0	
Control input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
Switch input/output voltage	V <sub>S</sub>	-0.5 to 7.0	V
Clump diode current	I <sub>IK</sub>	-50	mA
Switch input/output current	I <sub>S</sub>	64	mA
DC V <sub>CC</sub> /ground current per supply pin	I <sub>CCA</sub>	±25	mA
	I <sub>CCB</sub>	±25	
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Operating Ranges (Note 1)**

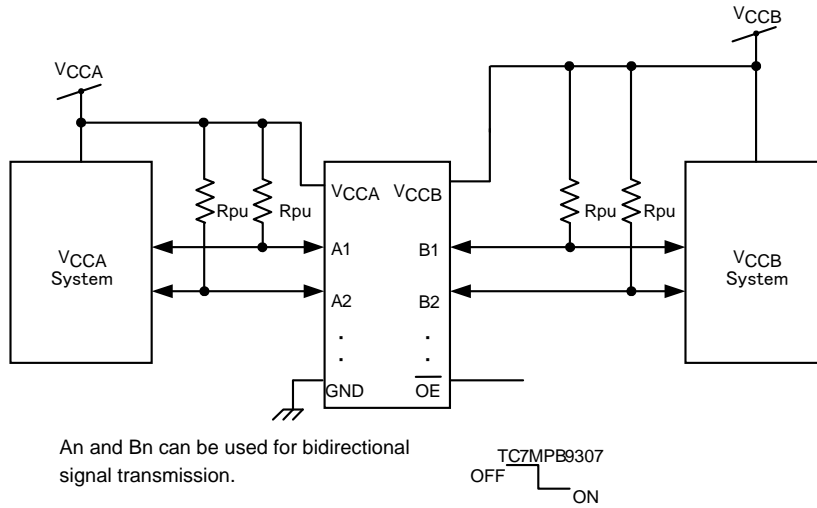
Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V <sub>CCA</sub>	1.65 to 5.0	V
	V <sub>CCB</sub>	2.3 to 5.5	
Control input voltage	V <sub>IN</sub>	0 to 5.5	V
Switch input/output voltage	V <sub>S</sub>	0 to 5.5	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Control input rise and fall times	dt/dv	0 to 10	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs and bus inputs must be tied to either V<sub>CCA</sub> or GND.

Note 2: The V<sub>CCA</sub> voltage must be lower than the V<sub>CCB</sub> voltage.

**Application Circuit**



**Figure 1 Application Circuit Diagram**

The  $V_{CCA}$  voltage must be lower than the  $V_{CCB}$  voltage.

Level-shifting functionality is enabled by adding pull-up resistors from An to  $V_{CCA}$  or  $V_{CCB}$  and from Bn to  $V_{CCB}$  or  $V_{CCA}$ , respectively.

**Electrical Characteristics**

**DC Characteristics (Ta = -40 to 85°C)**

Characteristics		Symbol	Test Condition	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Ta = -40to85°C		Unit
						Min	Max	
Control input voltage	High-level	V <sub>IH</sub>	—	1.65 ≤ V <sub>CCA</sub> < 2.3	V <sub>CCA</sub> to 5.5	0.8 × V <sub>CCA</sub>	—	V
				2.3 ≤ V <sub>CCA</sub> < 5.0	V <sub>CCA</sub> to 5.5	0.7 × V <sub>CCA</sub>	—	
	Low-level	V <sub>IL</sub>	—	1.65 ≤ V <sub>CCA</sub> < 2.3	V <sub>CCA</sub> to 5.5	—	0.2 × V <sub>CCA</sub>	
				2.3 ≤ V <sub>CCA</sub> < 5.0	V <sub>CCA</sub> to 5.5	—	0.3 × V <sub>CCA</sub>	
ON-resistance (Note)	R <sub>ON</sub>	V <sub>IS</sub> = 0V, I <sub>IS</sub> = 30mA (Figure 2)	1.65	2.3	—	16.0	Ω	
			2.3	3.0	—	11.0		
			3.0	4.5	—	8.0		
Power off leakage current	I <sub>OFF</sub>	An,Bn=0 to 5.5V (per circuit)	0	0	—	±1.0	μA	
Switch-off leakage current	I <sub>SZ</sub>	An,Bn=0 to 5.5V $\overline{OE} = V_{CCA}$ , OE=GND	1.65 to 5.0	V <sub>CCA</sub> to 5.5	—	±1.0	μA	
Control input current	I <sub>IN</sub>	$\overline{OE} = 0$ to 5.5V	1.65 to 5.0	V <sub>CCA</sub> to 5.5	—	±1.0	μA	
leakage current form V <sub>CCB</sub> to V <sub>CCA</sub>	I <sub>CCBA</sub>	$\overline{OE} = 0$ or V <sub>CCA</sub> V <sub>CCB</sub> → V <sub>CCA</sub>	3.3	5.0	—	50.0	μA	
Quiescent supply current	I <sub>CCA1</sub>	$\overline{OE} = V_{CCA}$ or GND, I <sub>S</sub> =0A	1.65 to 5.0	V <sub>CCA</sub>	—	10.0	μA	
	I <sub>CCB1</sub>	$\overline{OE} = V_{CCA}$ or GND, I <sub>S</sub> =0A	1.65 to 5.0	V <sub>CCA</sub>	—	10.0		
	I <sub>CCA2</sub>	V <sub>CCA</sub> ≤ $\overline{OE}$ ≤ 5.5 V, I <sub>S</sub> =0A	1.65 to 5.0	V <sub>CCA</sub>	—	±10.0		
	I <sub>CCB2</sub>	V <sub>CCA</sub> ≤ $\overline{OE}$ ≤ 5.5 V, I <sub>S</sub> =0A	1.65 to 5.0	V <sub>CCA</sub>	—	±10.0		

Note: ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

**Level Shift Characteristics (Ta = -40 to 85°C)**

Characteristics	Symbol	Test Condition	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Ta = -40 to 85°C		Unit
					Min	Max	
Input/Output Characteristics (Up Translation) (Note 1)	V <sub>O<sub>HU</sub></sub>	An = V <sub>IN</sub> SW = ON (Figure 7)	1.65	3.0 to 5.5	1.4	—	V
			2.3	4.5 to 5.5	2.05	—	
			3.0	4.5 to 5.5	2.7	—	
Input/Output Characteristics (Down Translation) (Note 2)	V <sub>O<sub>HD</sub></sub>	An = V <sub>CCA</sub> SW = ON (Figure 9)	1.65	3.3 to 5.5	1.3	1.65	V
			2.3	4.5 to 5.5	1.95	2.3	
			3.0	4.5 to 5.5	2.6	3.0	

Note 1: The Input/Output Characateristics for up translation indicate the input voltages required to provide V<sub>CCA</sub> + 0.5 V on the outputs when measured using the test circuitry shown in Figure 7.

Note 2: The Input/Output Characateristics for down translation indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Figure 9.

## AC Characteristics (Ta = -40 to 85°C, Input: tr = tf = 2.0 ns, f=10kHz)

VCCA = 3.3 ± 0.3 V, VCCB = 5.0 ± 0.5 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bus to Bus)	tpLH	Figures 3 and 5 (Note)	—	0.3	ns
Propagation delay time (Bus to Bus)	tpHL	Figures 3 and 5 (Note)	—	1.2	
Output enable time	tpZL	Figures 4 and 6	—	9.0	
Output disable time	tpLZ	Figures 4 and 6	—	11.0	

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

VCCA = 2.5 ± 0.2 V, VCCB = 5.0 ± 0.5 V

Characteristics	記号	Test Condition	Min	Max	Unit
Propagation delay time (Bus to Bus)	tpLH	Figures 3 and 5 (Note)	—	0.35	ns
Propagation delay time (Bus to Bus)	tpHL	Figures 3 and 5 (Note)	—	1.8	
Output enable time	tpZL	Figures 4 and 6	—	13.0	
Output disable time	tpLZ	Figures 4 and 6	—	15.0	

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

VCCA = 2.5 ± 0.2 V, VCCB = 3.3 ± 0.3 V

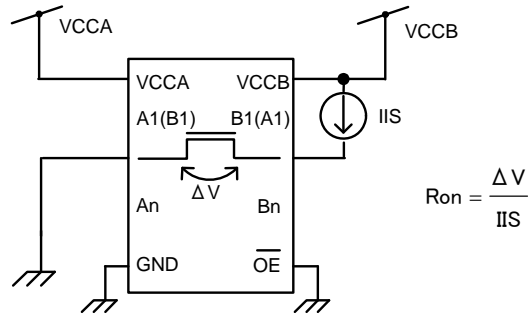
Characteristics	記号	Test Condition	Min	Max	Unit
Propagation delay time (Bus to Bus)	tpLH	Figures 3 and 5 (Note)	—	0.45	ns
Propagation delay time (Bus to Bus)	tpHL	Figures 3 and 5 (Note)	—	2.2	
Output enable time	tpZL	Figures 4 and 6	—	17.0	
Output disable time	tpLZ	Figures 4 and 6	—	19.0	

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	VCCA (V)		Typ.	Unit
			VCCA (V)	VCCB (V)		
Control input capacitance	CIN		3.3	3.3	3	pF
Switch input/output capacitance	CI/O	SW=ON	3.3	3.3	14	
		SW=OFF	3.3	3.3	7	

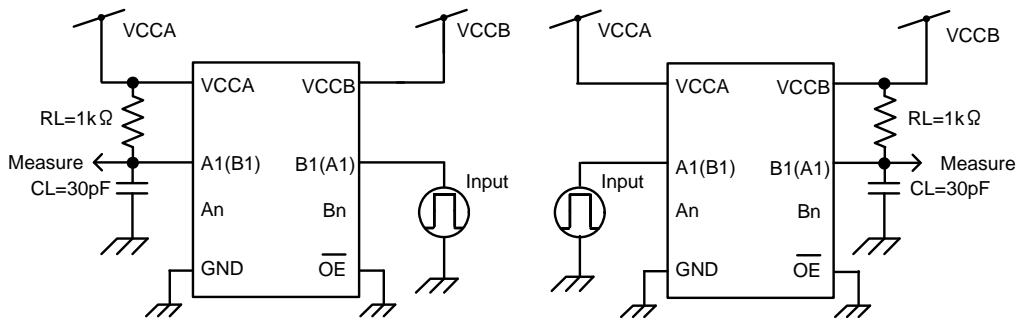
**DC Test Circuit**



**Figure 2 ON-resistance Test Circuits**

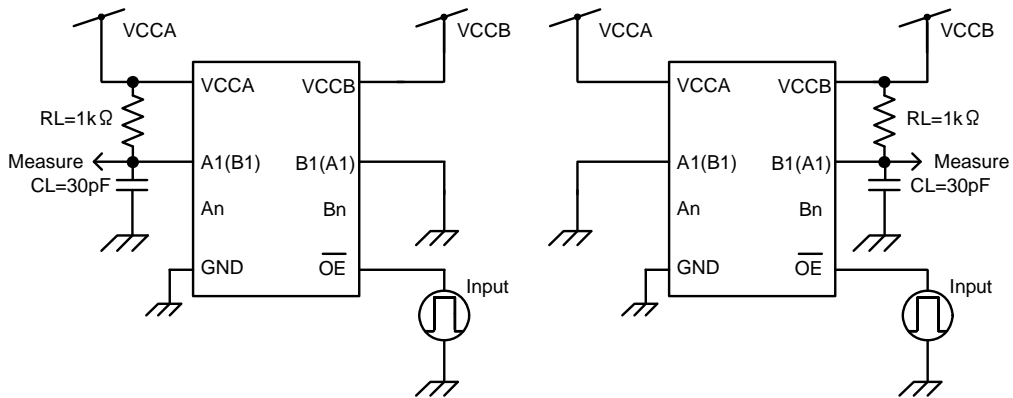
**AC Test Circuits**

• **tpLH,HL**



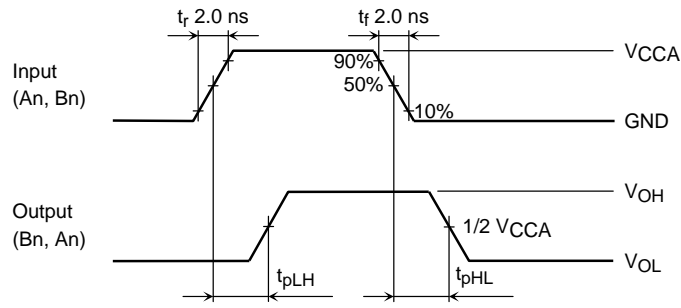
**Figure 3 tpLH, tpHL Test Circuits**

• **tpLZ,ZL**

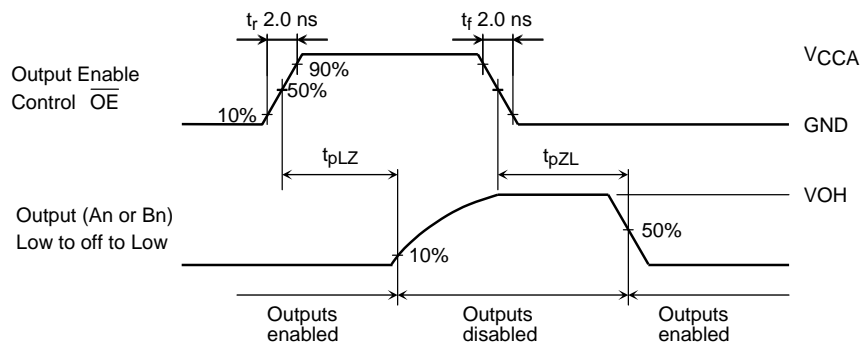


**Figure 4 tpLZ, tpZL Test Circuits**

**AC Waveform**



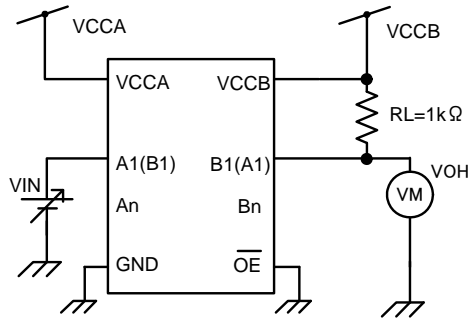
**Figure 5  $t_{pLH}$ ,  $t_{pHL}$**



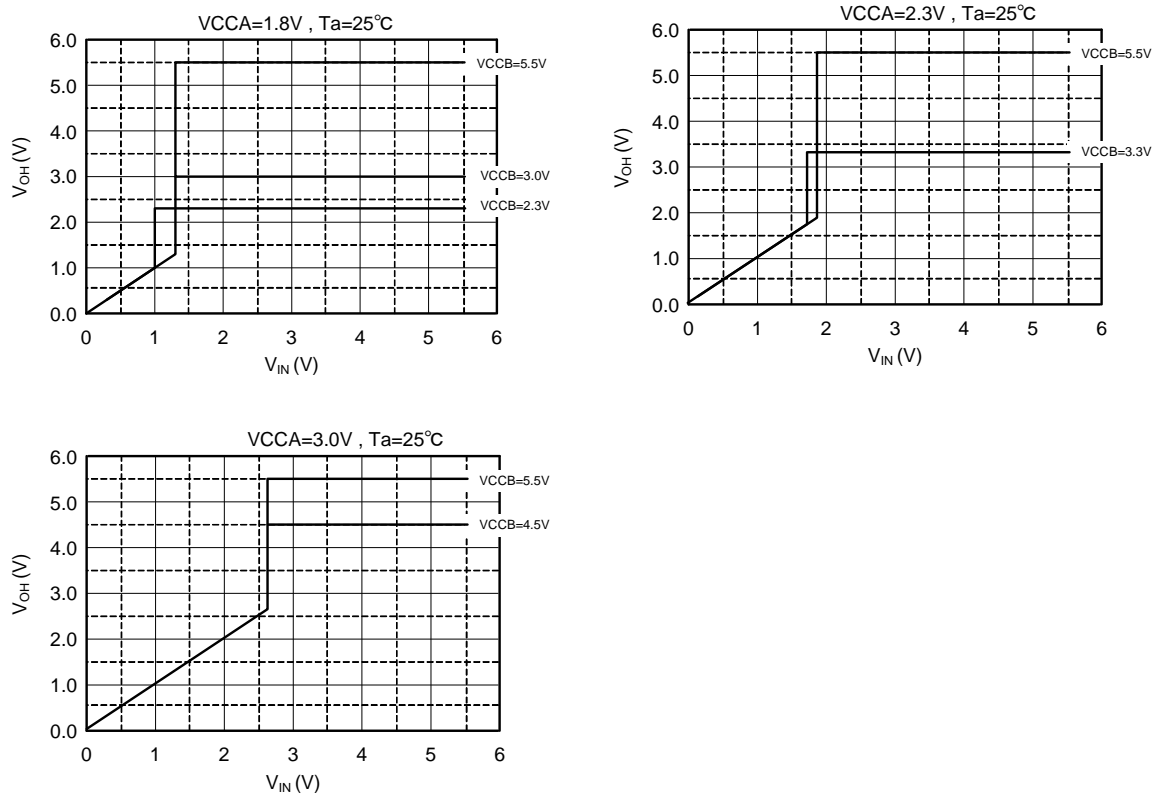
**Figure 6  $t_{pLZ}$ ,  $t_{pZL}$**



**Level Shift Function (Used Pull-up Resistance)**

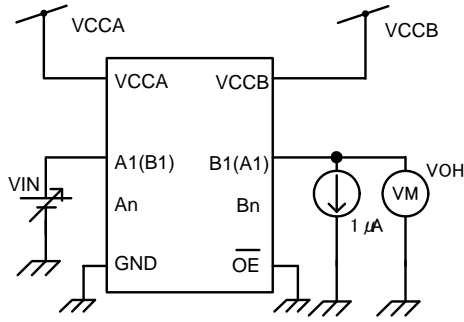


**Figure 7 Test Circuit**

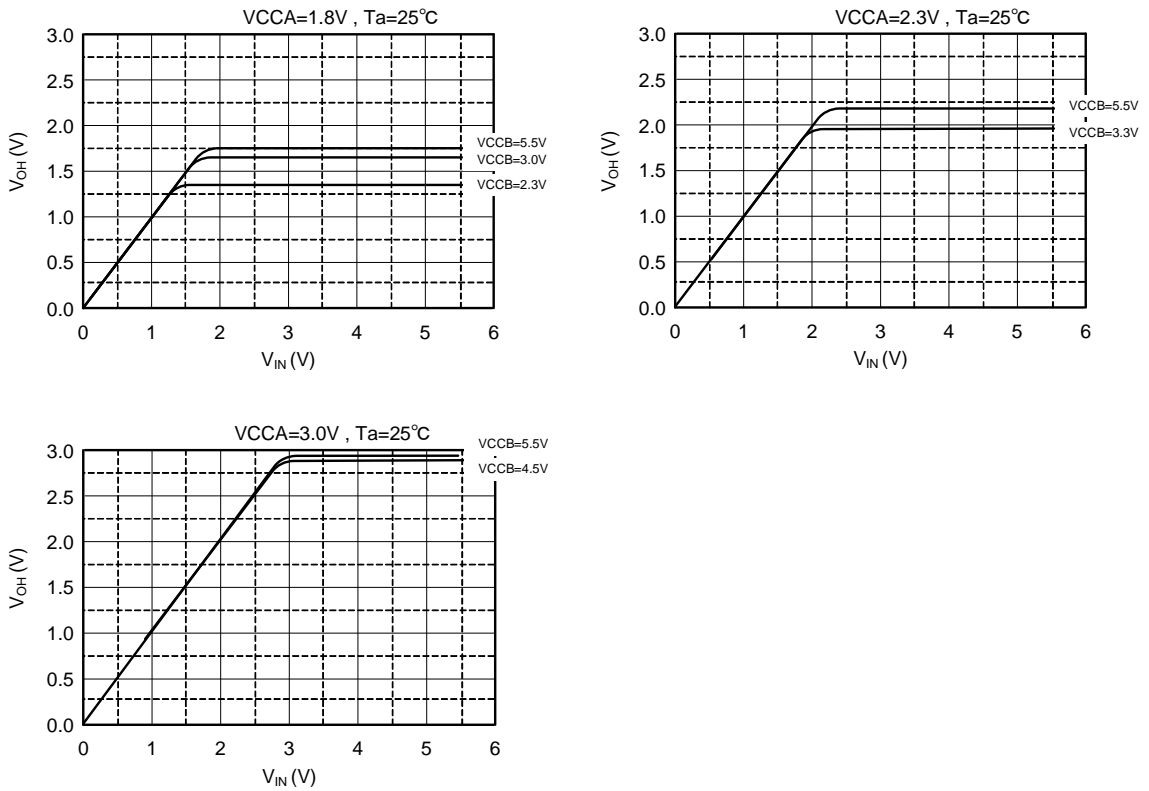


**Figure 8 Input/Output Characteristics (Typ.)**

**Level Shift Function (Unused Pull-up Resistance)**



**Figure 9 Test Circuit**

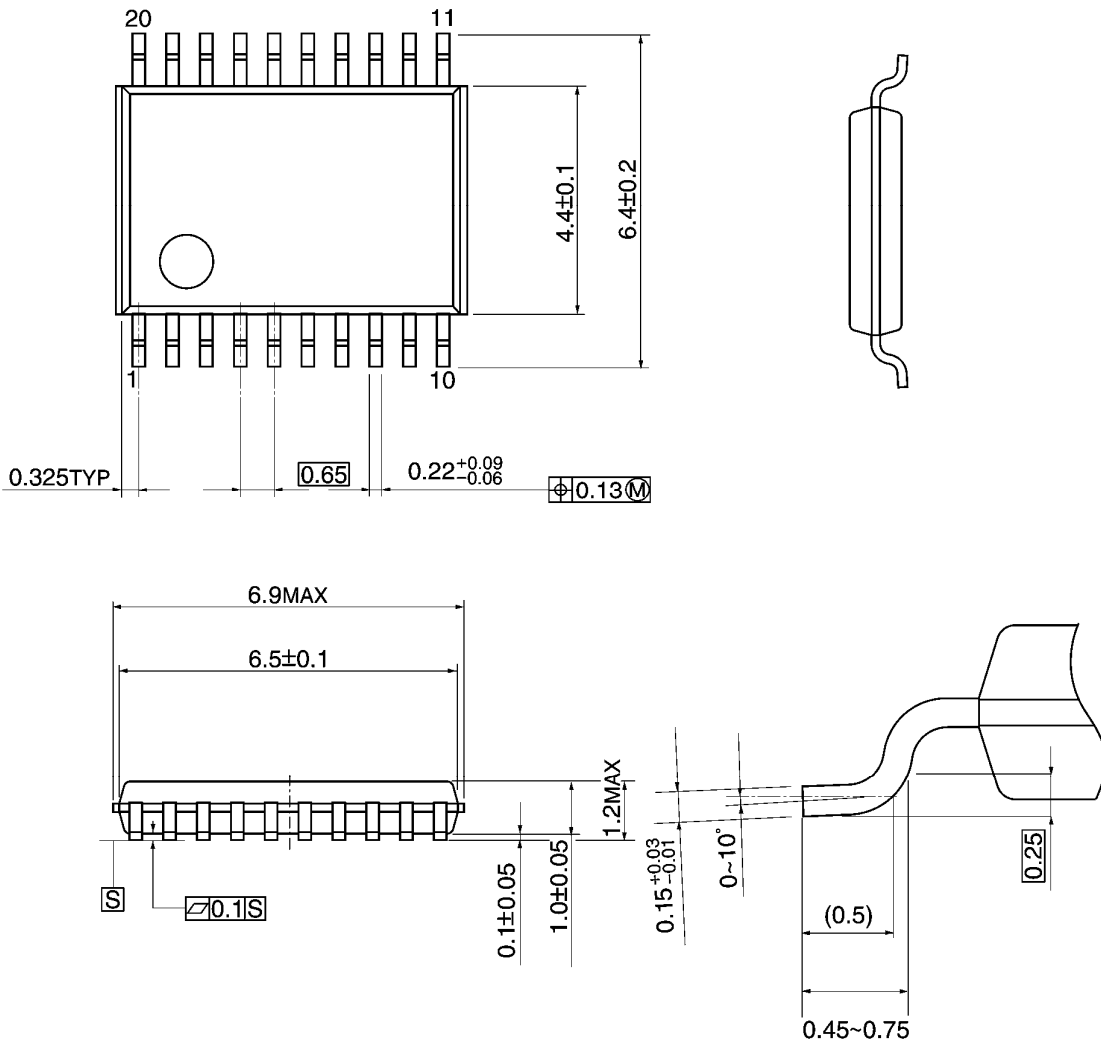


**Figure 10 Input/Output Characteristics (Typ.)**

**Package Dimensions**

TSSOP20-P-0044-0.65A

Unit: mm

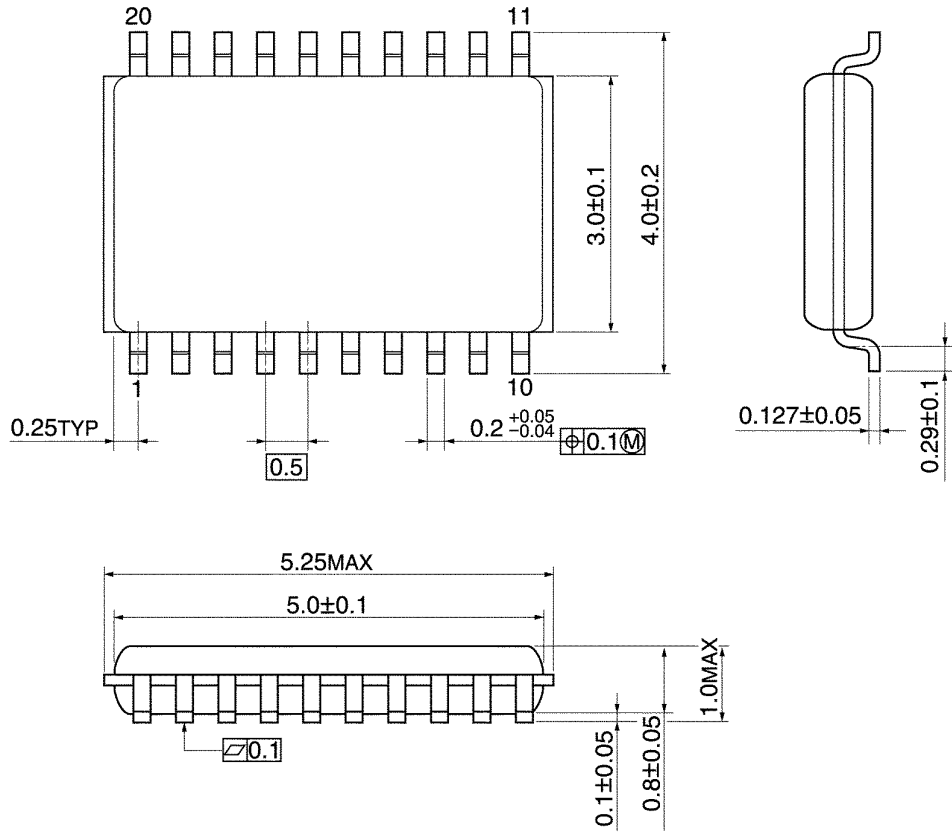


Weight: 0.08 g (typ.)

## Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (Typ.)

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