TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MH595FK

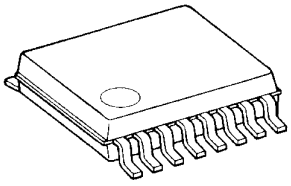
8-Bit Shift Register/Latch (3-State)

The TC7MH595FK is an advanced high speed 8 bit shift register/latch fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

The TC7MH595FK contains an 8 bit static shift register which feeds an 8 bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signals are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3-state, it can be directly connected to 8 bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.



VSSOP16-P-0030-0.50

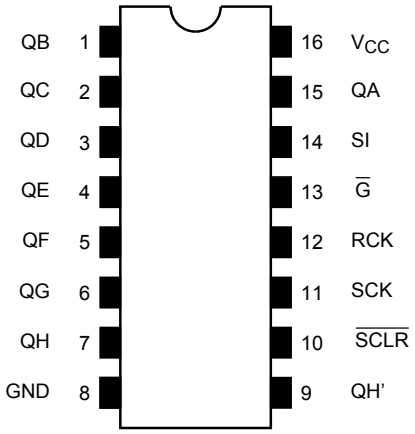
Weight: 0.02 g (typ.)

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

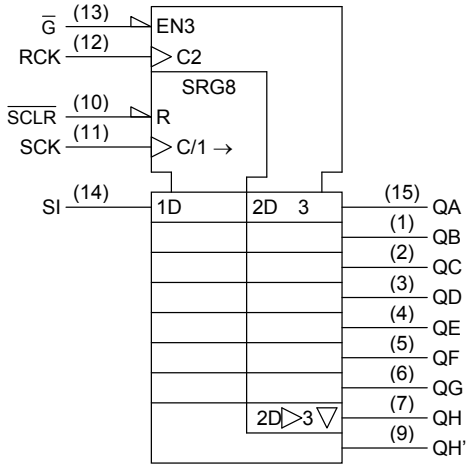
Features

- High speed: f_{max} = 185 MHz (typ.) (V_{CC} = 5 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2~5.5 V
- Low noise: V_{OLP} = 1.0 V (max)
- Pin and function compatible with 74ALS595

Pin Assignment (top view)



IEC Logic Symbol

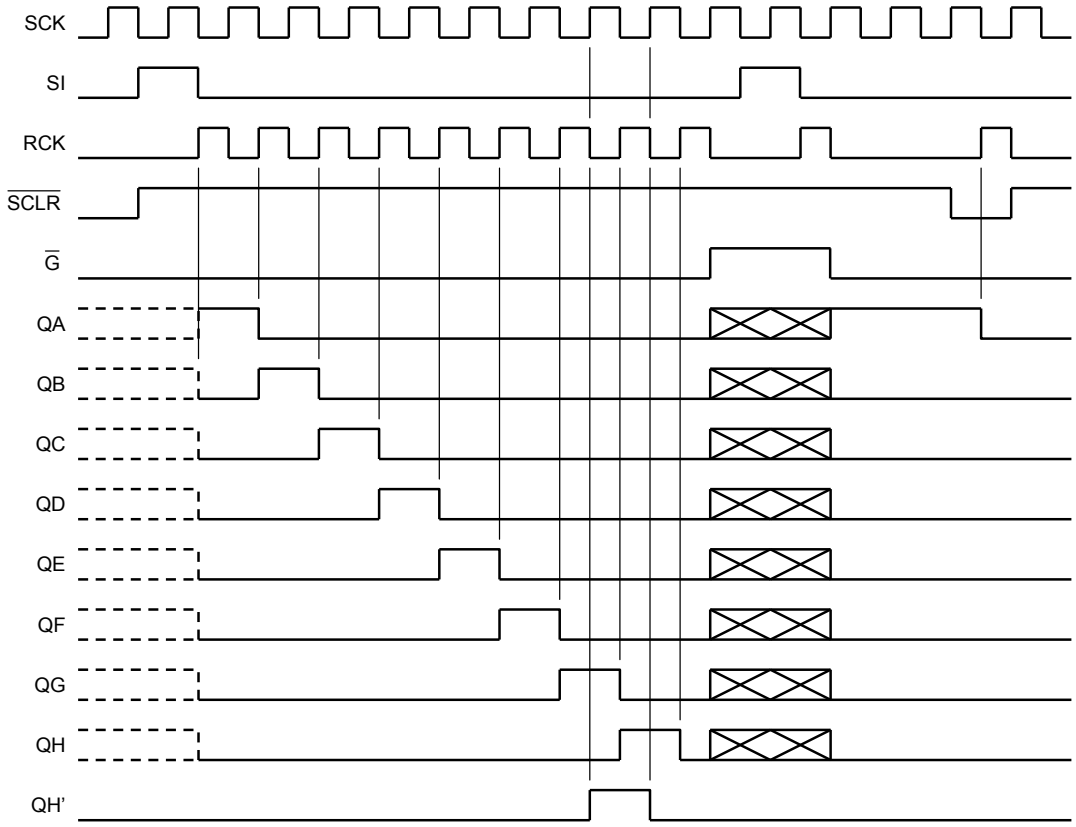


Truth Table

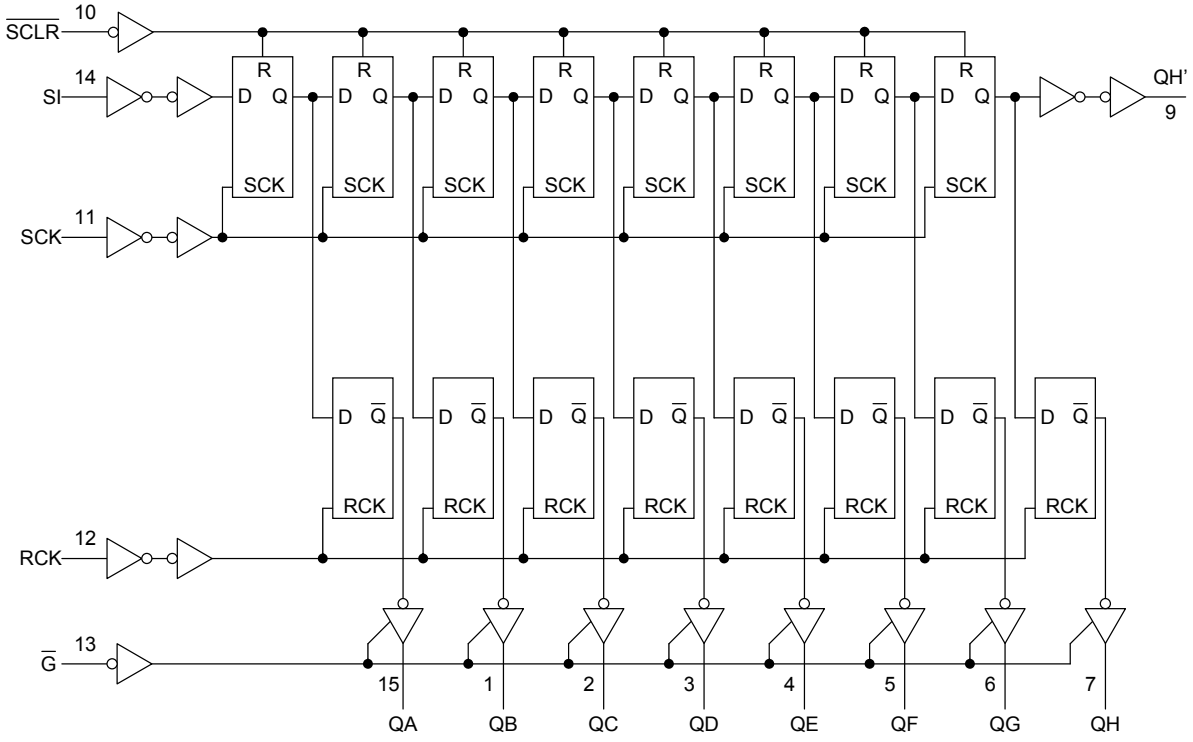
Inputs					Function
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes “L”. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes “H”. Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register stage is not changed.

X: Don’t care

Timing Chart



System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~7.0	V
DC output voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~5.5	V
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3 V)	ns/V
		0~20 (V_{CC} = 5 ± 0.5 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
					V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	High level	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
					3.0~5.5	V_{CC} × 0.7	—	—	V_{CC} × 0.7	—	
	Low level	V_{IL}	—		2.0	—	—	0.50	—	0.50	
					3.0~5.5	—	—	V_{CC} × 0.3	—	V_{CC} × 0.3	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
				I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
				I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
				I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current		I_{IN}	V_{IN} = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA

Timing Requirements (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40~85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (SCK, RCK)	$t_{w\,(H)}$ $t_{w\,(L)}$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width ($\overline{SCLR}$)	$t_{w\,(L)}$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time (SI-SCK)	t_s	—	3.3 ± 0.3	—	3.5	3.5	ns
			5.0 ± 0.5	—	3.0	3.0	
Minimum set-up time (SCK-RCK)	t_s	—	3.3 ± 0.3	—	8.0	8.5	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time ($\overline{SCLR}$-RCK)	t_s	—	3.3 ± 0.3	—	8.0	9.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum hold time (SI-SCK)	t_h	—	3.3 ± 0.3	—	1.5	1.5	ns
			5.0 ± 0.5	—	2.0	2.0	
Minimum hold time (SCK-RCK, $\overline{SCLR}$-RCK)	t_h	—	3.3 ± 0.3	—	0	0	ns
			5.0 ± 0.5	—	0	0	
Minimum removal time ($\overline{SCLR}$)	t_{rem}	—	3.3 ± 0.3	—	3.0	3.0	ns
			5.0 ± 0.5	—	2.5	2.5	

AC Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (SCK-QH')	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	8.8	13.0	1.0	15.0	ns
				50	—	11.3	16.5	1.0	18.5	
			5.0 ± 0.5	15	—	6.2	8.2	1.0	9.4	
				50	—	7.7	10.2	1.0	11.4	
Propagation delay time ($\overline{SCLR}$ -QH')	t_{pHL}	—	3.3 ± 0.3	15	—	8.4	12.8	1.0	13.7	ns
				50	—	10.9	16.3	1.0	17.2	
			5.0 ± 0.5	15	—	5.9	8.0	1.0	9.1	
				50	—	7.4	10.0	1.0	11.1	
Propagation delay time (RCK-Q_n)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.7	11.9	1.0	13.5	ns
				50	—	10.2	15.4	1.0	17.0	
			5.0 ± 0.5	15	—	5.4	7.4	1.0	8.5	
				50	—	6.9	9.4	1.0	10.5	
Output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	3.3 ± 0.3	15	—	7.5	11.5	1.0	13.5	ns
				50	—	9.0	15.0	1.0	17.0	
			5.0 ± 0.5	15	—	4.8	8.6	1.0	10.0	
				50	—	8.3	10.6	1.0	12.0	
Output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	3.3 ± 0.3	50	—	12.1	15.7	1.0	16.2	ns
			5.0 ± 0.5	50	—	7.6	10.3	1.0	11.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	80	150	—	70	—	MHz
				50	55	130	—	50	—	
			5.0 ± 0.5	15	135	185	—	115	—	
				50	95	155	—	85	—	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	6	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note)			—	87	—	—	—	pF

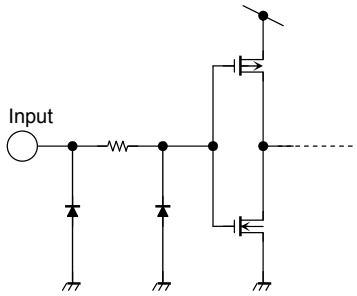
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

Noise Characteristics (Input: $t_r = t_f = 3$ ns)

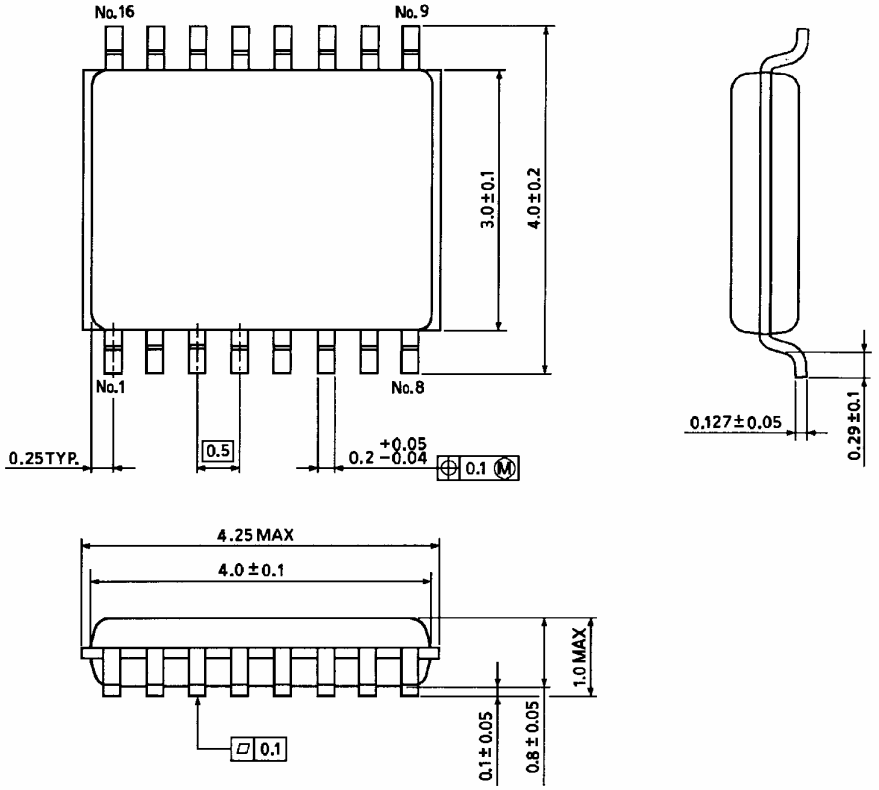
Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.8	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.8	−1.0	V
Minimum high level dynamic input voltage VIH	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage VIL	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Input Equivalent Circuit



Package Dimensions

VSSOP16-P-0030-0.50 Unit : mm



Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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