SIEMENS

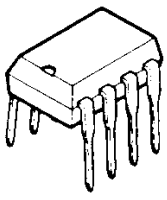
Dimmer IC

SLB 0586

CMOS IC

Features

- Sensor operation - no mechanically moved switching elements
- Operation is also possible from several extensions by means of sensors or push buttons
- Can replace electromechanical wall switches in conventional light installations
- Brightness control with a physiologically approximated linear characteristic
- Very high interference immunity, also against ripple control signals
- Very few peripheral components
- Programming input permits selection of three different functions (MODE A/B/C)
- "Soft" turn-ON with MODE A and C



VPD05025

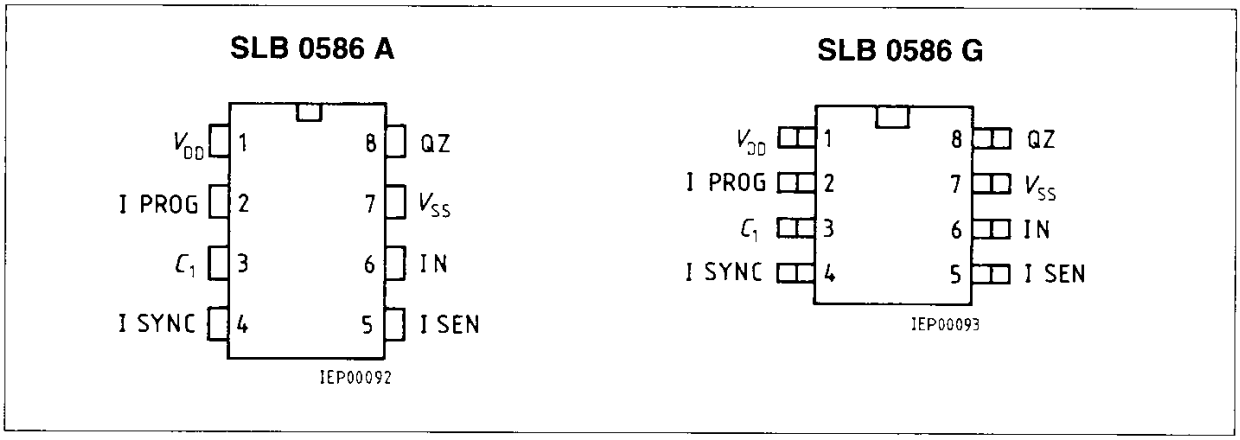
P-DIP-8

VPS05121

P-DSO-8-1

Type	Ordering Code	Package
S SLB 0586 A	Q67000-H8721	P-DIP-8
S SLB 0586 G	Q67000-H8720	P-DSO-8-1 (SMD)

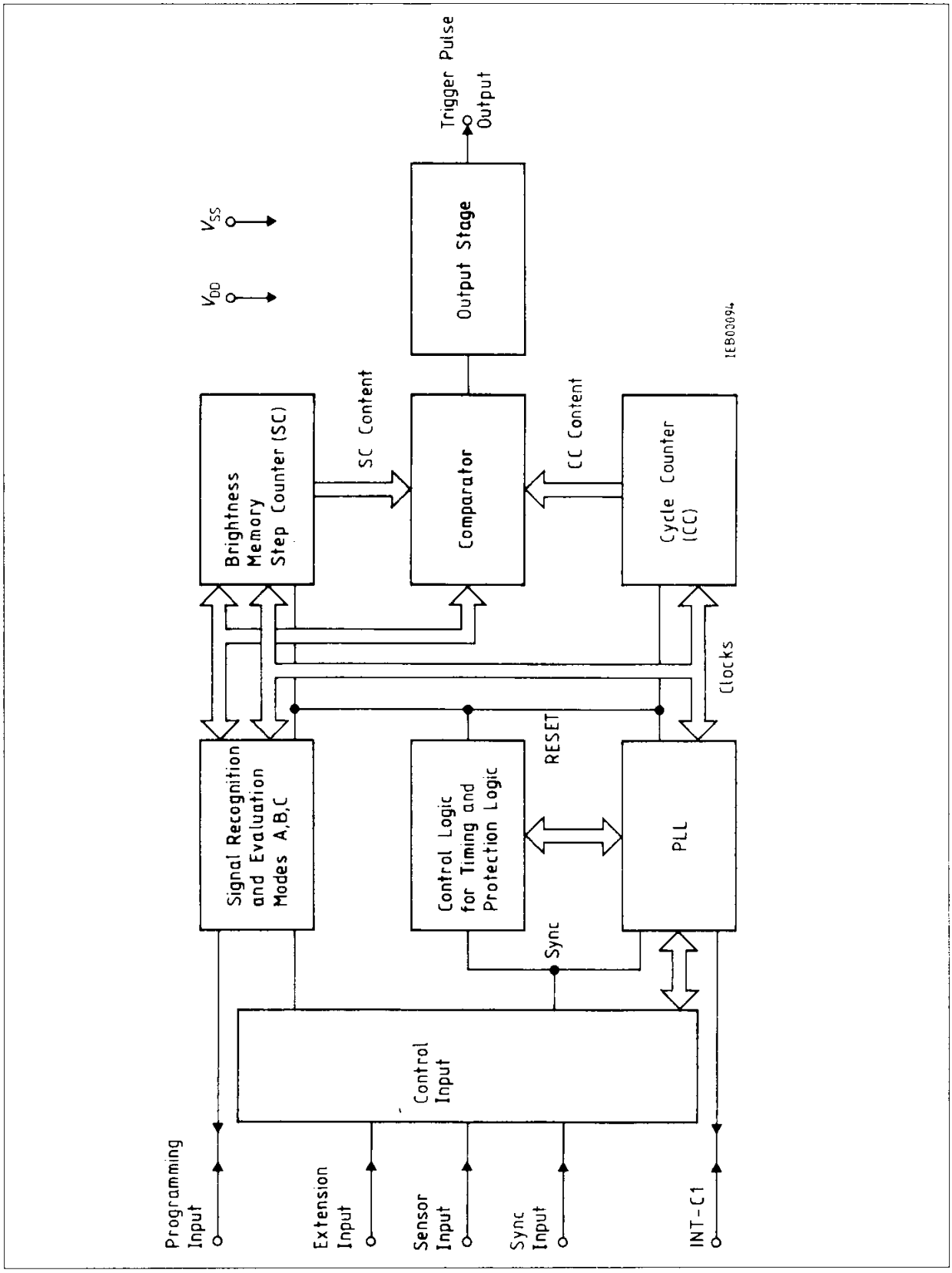
The SLB 0586 A and SLB 0586 G are integrated circuits in CMOS technology that permit the design of digital electronic dimmers. A single sensor or an equivalent extension input are used to turn the dimmer ON and OFF and to set the required brightness.



Pin Configurations
(top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{DD}	Ground
2	I PROG	Programming input
3	C_1	C_1 integrator
4	I SYNC	Sync input
5	I SEN	Sensor input
6	IN	Extension input
7	V_{SS}	Supply voltage
8	QZ	Trigger pulse output



Block Diagram

Functional Description

The SLB 0586 A permits the design of fully electronic dimmers for light bulbs (resistive loads) which are operated via a single sensor.

The integrated circuit replaces mechanical wall switches in conventional light circuit installations. All functions can be selected from several switching points (extensions).

The brightness is set by phase control. Its digital logic is synchronized with the line frequency (**see Block Diagram**).

It is possible to supply the IC via a two-wire connection, as the angle of current flow is limited to a maximum of 152 °C of the half wave.

Operation

The integrated circuit can distinguish the instruction "ON/OFF" and "Dimming" by the duration for which control input is operated i.e. the sensor is touched (**refer to figure 1**).

Turning ON/OFF

Short touching (50 to 400 ms) of the sensor area turns the lamp ON or OFF, depending on its preceding state. The switching process is activated as soon as the sensor is released.

Setting of the Brightness (Dimming)

If the sensor is touched for a longer period (> 400 ms), the angle of current flow will be varied continuously. It runs across its control loop in approximately 7.6 s (e.g. bright-dark-bright) and continues this sequence until the sensor is released.

Easy operation, even in the lower brightness range, is enabled by the following procedure: the phase control angle is controlled such that the lamp brightness varies physiologically-linear with the operating time and pauses for a short period when the minimum brightness is reached.

Using R_2 and C_4 in the application circuit the angle of current flow can be controlled between 40° and 148°.

Control Behavior

The three operating MODES A, B, C, differ in their control behavior. The required MODE is set with the programming input.

MODE A With turn-ON, the maximum brightness level is set; with dimming, control starts from the minimum brightness level. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

MODE B With turn-OFF, the selected brightness is stored and set again when the switch is turned on. Dimming starts at this stored value and the control direction is reversed with repeated dimming.

MODE C With turn-ON, the maximum brightness is set; with dimming, control is started from the minimum brightness. The control direction is reversed with repeated dimming.

Programming of the MODES

MODE A: $V_{I2} = V_{SS}$ (L)

MODE B: V_{I2} = open (tristate)

MODE C: $V_{I2} = V_{DD}$ (H)

V_{I2} = Level at pin 2

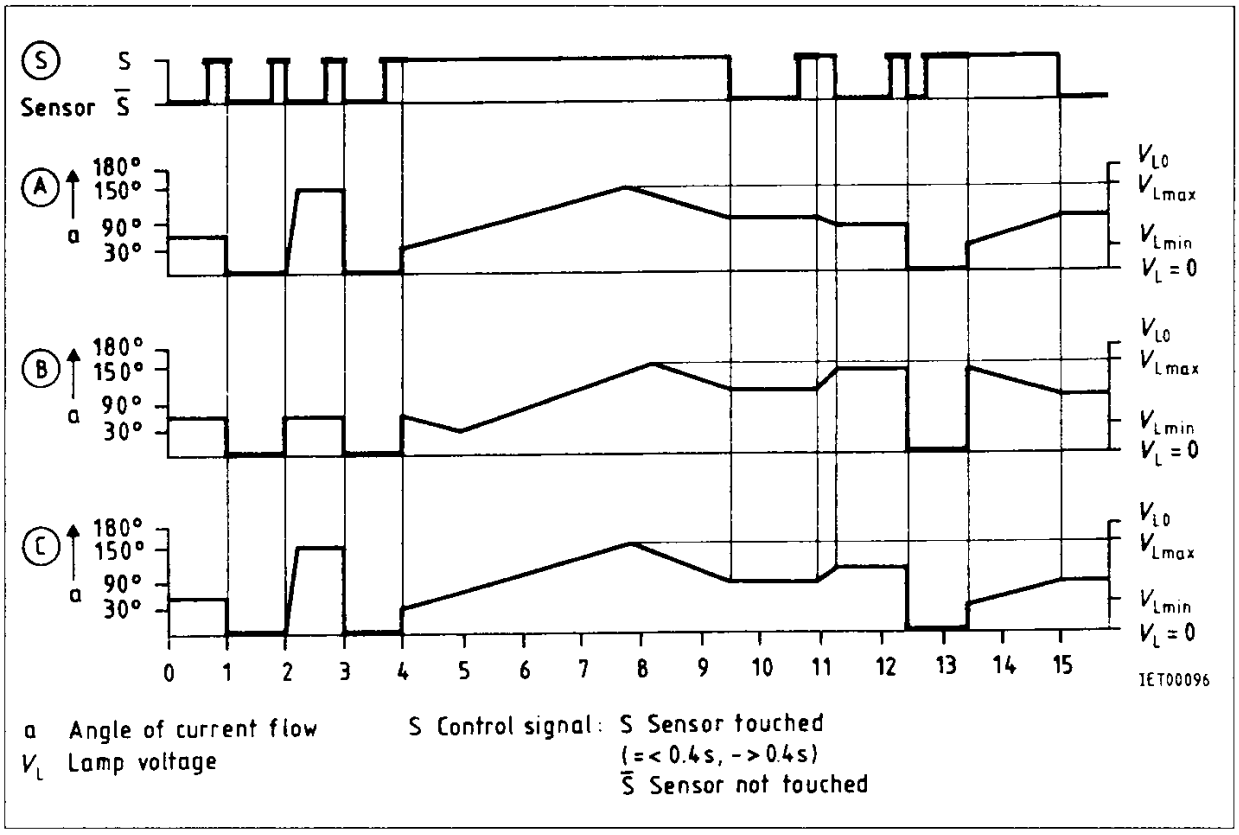


Figure 1
Control Behavior of Operating MODES
(schematic)

MODES A and C permit "soft" turn-ON; i.e. brightness is increased from 0 to maximum within 380 ms.

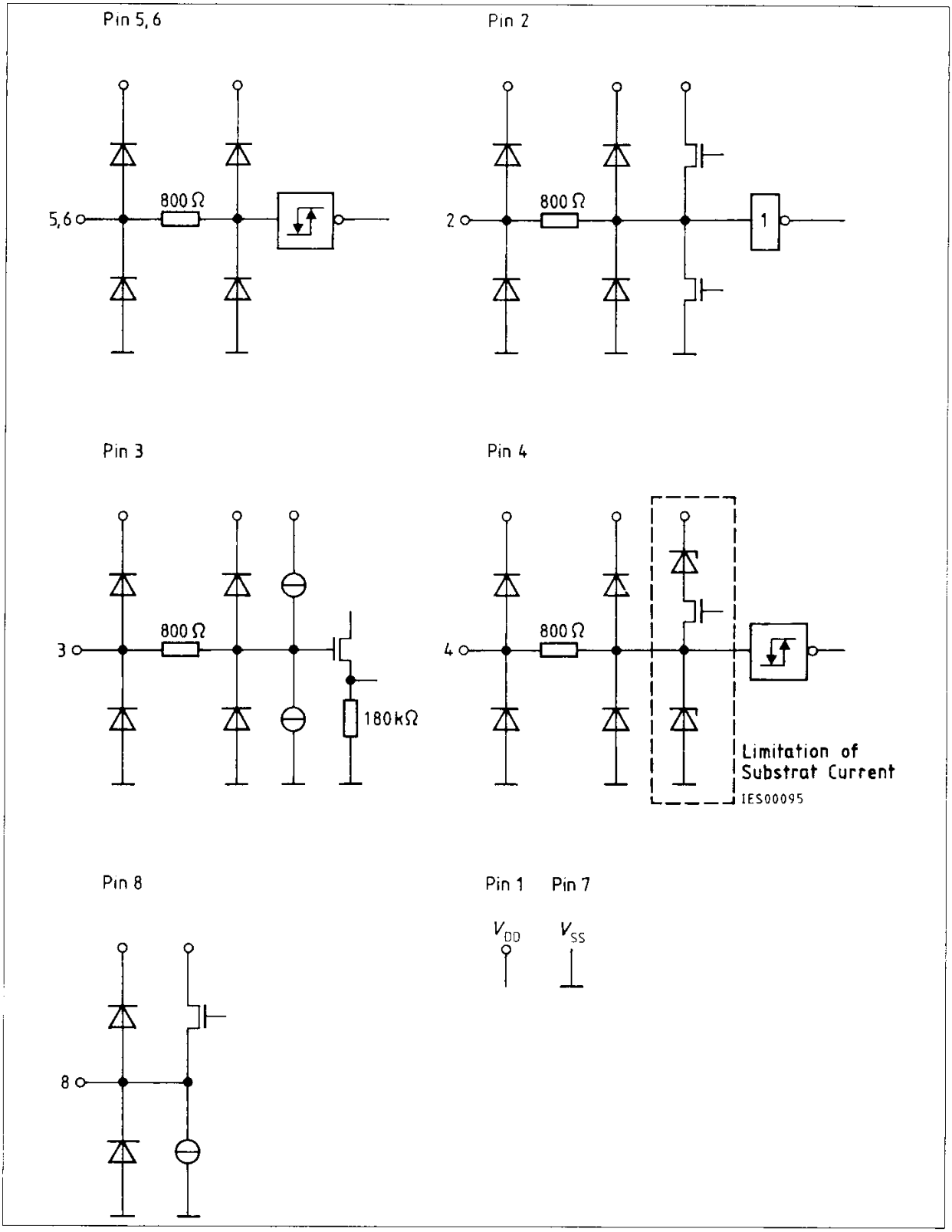


Figure 2

Internal Wiring of Pins

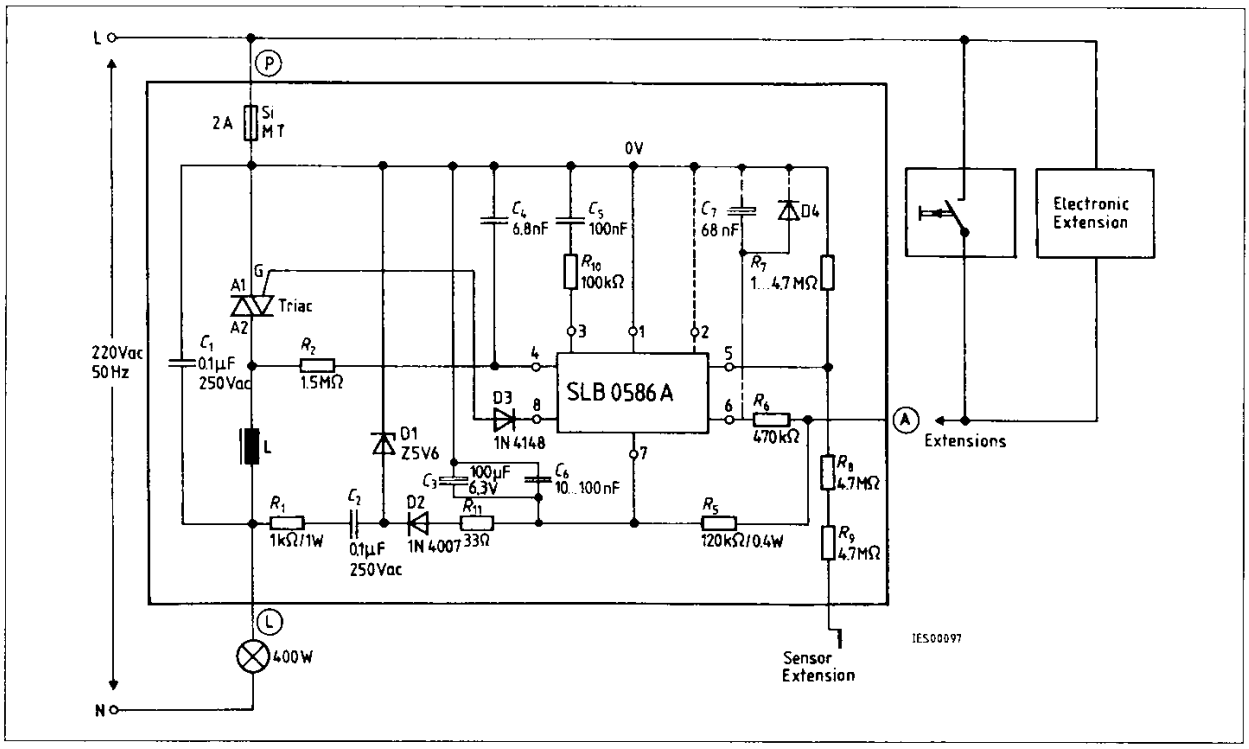


Figure 3
Application Circuit

The suggested circuit design of the SLB 0586 A performs the following functions:

- Current supply for the circuit (R_1, C_2, D1, D2, C_3).
- Filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4). For specific applications C_4 can be increased up to 33 nF, so that the lamp gets darker (**refer to figure 3**).
- Integration unit for internal PLL circuit (C_5, R_{10})
- Protection of the user (R_8, R_9)
- Sensitivity setting of the sensor (R_7)
- Current limitation in the case of reverse polarity of the extension (R_5, R_6).
  Both resistors can be omitted, if no extension is connected. In this case pin 6 must be interconnected with V_{SS} (pin 7).
- D3: Reduction of positive voltages which may arise during the triggered state at the gate of some triacs to values below V_{DD} + 0.3 V by diode forward voltage. If suitable triacs are used, diode D3 can be omitted.
- Dr: The choke and the capacitor C_1 are used for EMI suppression.
  Depending on the application, the EMI suppression is to be dimensioned in acc. with
  VDE 0875/part 1 (general)
  VDE 0550/part 6 (chokes)
  or corresponding to national regulations
  e.g. 1.4...2 mH, Q = 11...24

- The components C_6 10...100 nF ceramic
  C_7 33...68 nF
  D_4 Ge or Schottky diode
  R_{11} 33...68 Ω
  serve to improve interference immunity under special conditions like for example:
  - high-frequency line interferences
  - long extension lines with high earth capacitances
  - supply line resistances in the load circuit
    and can therefore be dropped for normal operating conditions.
- At 110 V/60 Hz line:
  C_2: 150 nF/160 Vac
  R_2: 680 kΩ

Application Notes

1.Synchronization

Interference of the synchronization can be suppressed by setting the C_4 filter capacitor at the sync input between 3.3 and 33 nF. By increasing the C_4 value the range of the controllable conduction angles goes to less minimum brightness. At the same time, the immunity against superimposed interference from the line improves, so that, for example, with C_4 = 33 nF an interference amplitude of 30 V does not cause any synchronization errors in the range of 150 to 1500 Hz.

C_4 (nF)	Conduction angle (°)	Interference amplitude (V)
3.3	151 to 43	20
6.8	148 to 40	↓
10.0	147 to 39	
15.0	144 to 36	
33.0	136 to 28	30

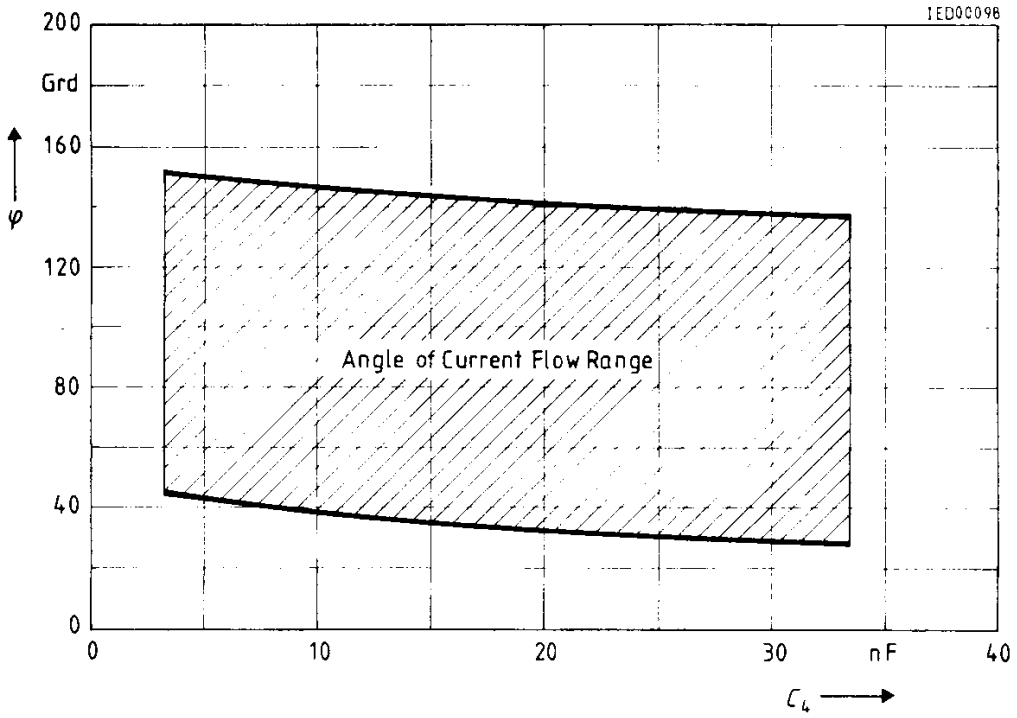
2. PLL Circuit

The PLL circuit at pin 3 can be varied to reach a minimum of flickering and a maximum of noise immunity. The PLL circuit is adjusted to a capacitor value of 100 nF.

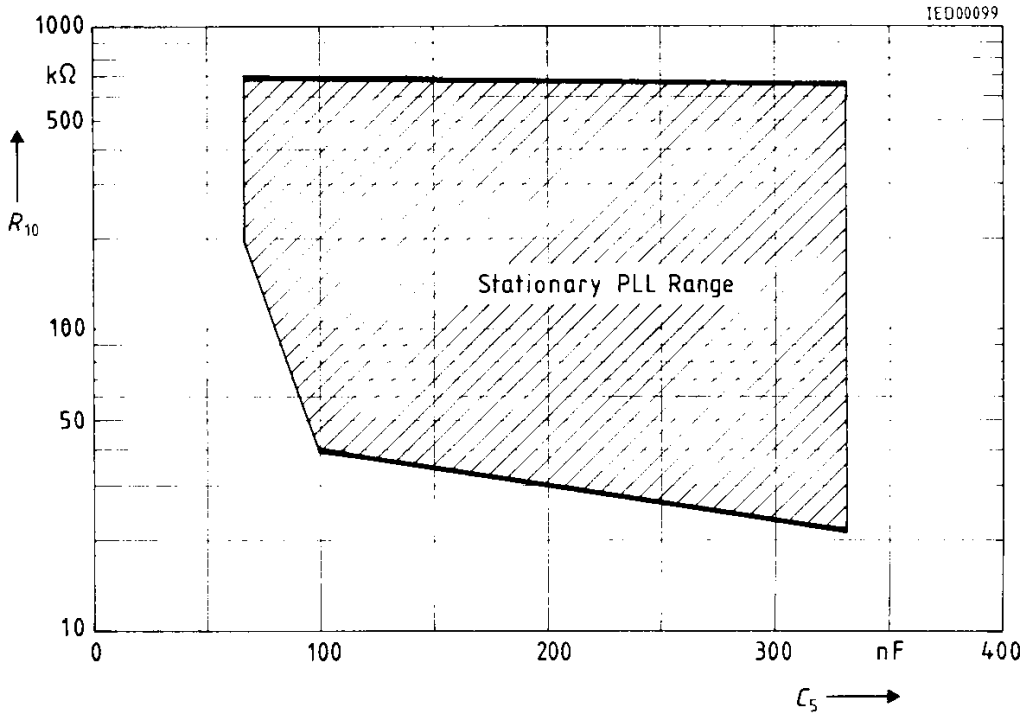
R_{10} can be varied in the range of 22 kΩ to 680 kΩ (**figure 5**). Here higher resistances speed up the response of the PLL circuit.

Hence it is possible to reduce the jitter of the trigger pulse to below 0.5 ms by a low-resistance R_{10} at low interference frequencies (≤ 400 Hz) and a high-resistance R_{10} at high interference frequencies. This will greatly reduce brightness modulations through interferences.

3. Dependence of C_4 and Angle of Current Flow (Figure 4)



4. Range of Value of the RC-Component at Pin 3 for Stationary PLL-Operation (Figure 5)



5. Extensions

All switching and control functions can also be performed from extensions which are connected to the extension input. The main sensor input and the extension inputs have equal priority. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation "H" potential must be applied to the extension input for both half cycles.

Note

The extension input must be connected to V_{SS}, if this input is not required.

Operation of the Control Inputs

Input potential during both half waves of the line phase:

Function	Line Half Wave	Sensor Input	Extension Input		
Operated	positive	L	H		
	negative	0	H		
Not operated	positive	H	L	or	0
	negative	0	0		L

Wireless Remote Control

The connection of a wireless remote control to the extension is very easy. All functions of the SLB 0586 A can be performed with the aid of a single transmission channel.

6. Interference Immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs and additionally allows almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In case of power failure the set switching state with the recommended external circuitry remains stored. After prolonged power failure ($V_{SS} > -3.6$ V) the circuit turns into OFF-state.

The control characteristic of the synchronous oscillator (PLL circuit) is designed such that interference due to ripple control signals may cause slight variations in brightness. However, they will not lead to a malfunction of the dimmer.

7. General Information

All time specifications refer to a line frequency of 50 Hz. In case of a line frequency of 60 Hz, the times are reduced accordingly.

8. Functional Description of Evaluation Logic for Sensor and Extension Inputs

The logic status at the sensor and extension inputs are sampled by latches L1 and L2 using the time slot pattern shown in the timing diagram (**figure 6**).

For operation (ON/OFF or DIMMING) "1" must be present at the D input of FF1 for two consecutive rising edges of the 50 Hz clock pulse of the internal PLL. The flipflops FF1 and FF2, are reset by two logic zeros occurring at the same time at latch outputs L1 and L2.

For operation via the extension input five consecutive sampling values must be "1". The minimum immunity time is therefore approx. 24 ms. Due to the different sampling rates, two sampling values of "1" must follow at the sensor input for an operation to be recognized. In this case the minimum immunity time is approx. 39 ms.

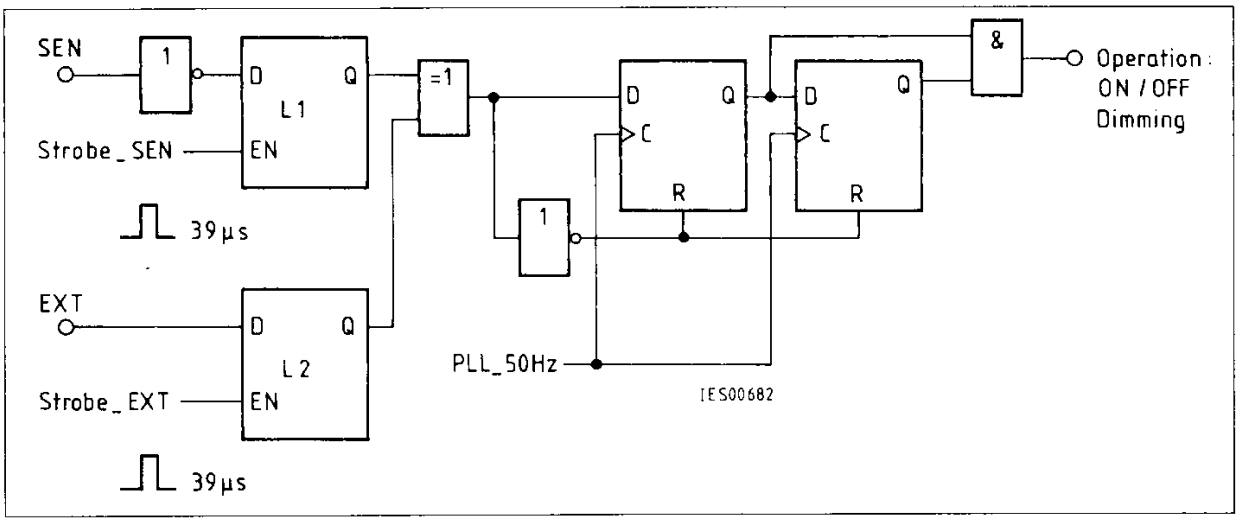


Figure 6

Schematic Circuit Diagram of Evaluation Logic for Sensor and Extension Inputs

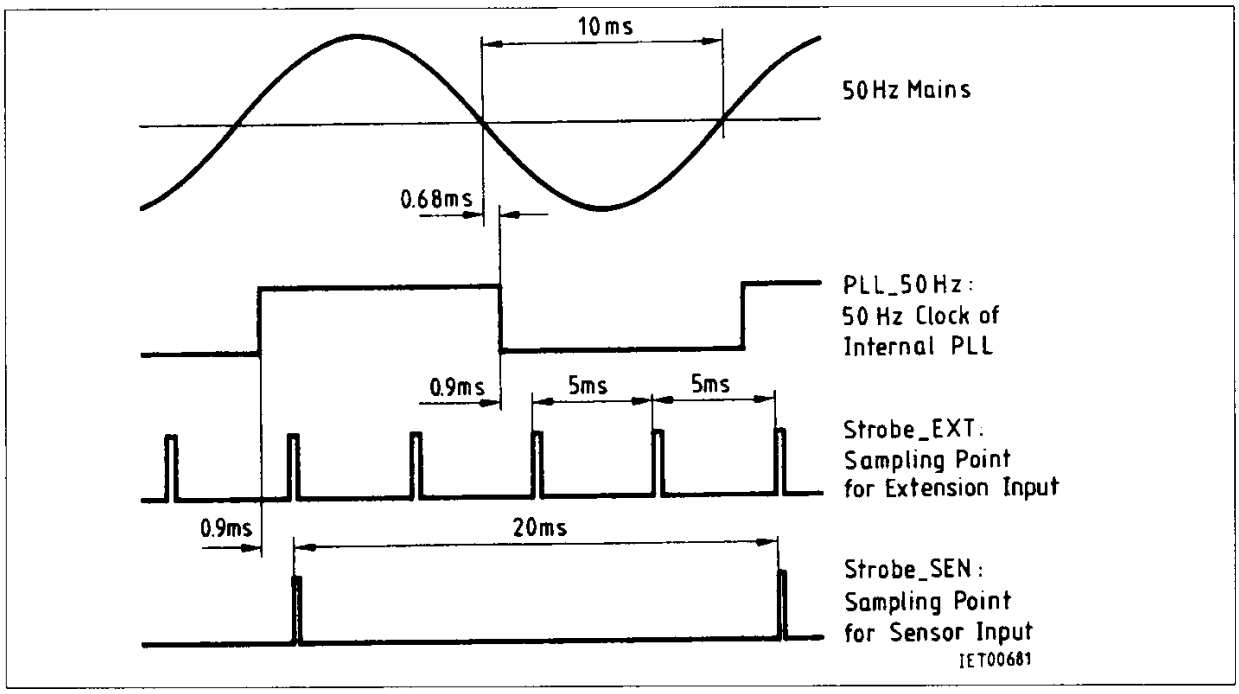


Figure 7

Timing Diagram of Evaluation Logic for Sensor and Extension Inputs

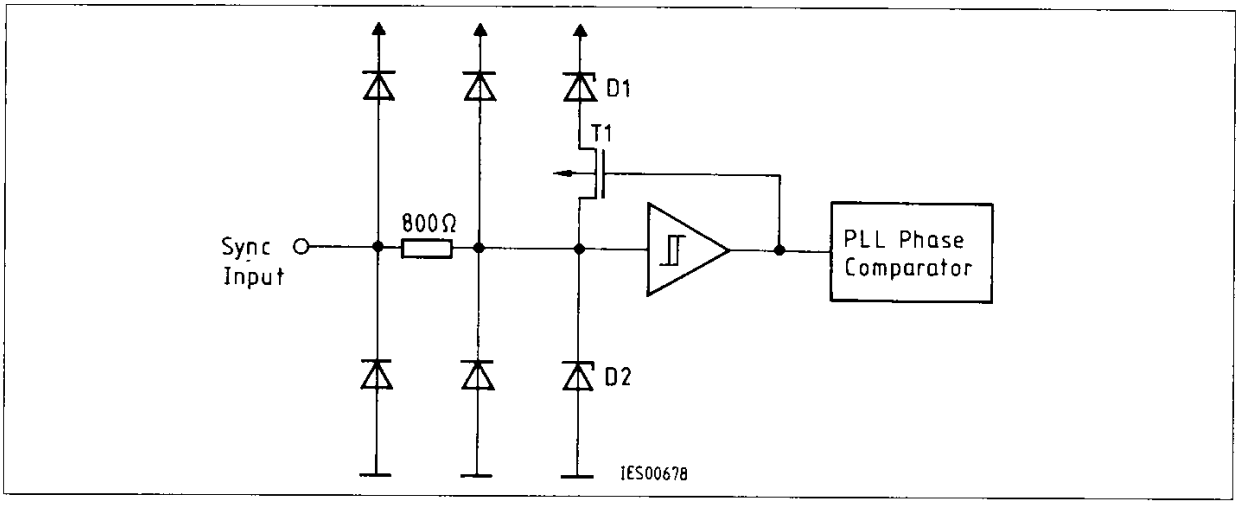


Figure 8

Schematic Circuit Diagram at Synchronous Input

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Functional Description

Diodes D1 and D2 have characteristics similar to Z-diodes and start conducting at about 2.5 V.

In spite of the line voltage at the triac it is ensured - by using R_2 - that the voltages present at the synchronous input of SLB 0586 A remain within the supply voltage level.

To obtain a highly stable trigger point for the phase comparator, T1 becomes conductive only after recognizing the synchronization edge.

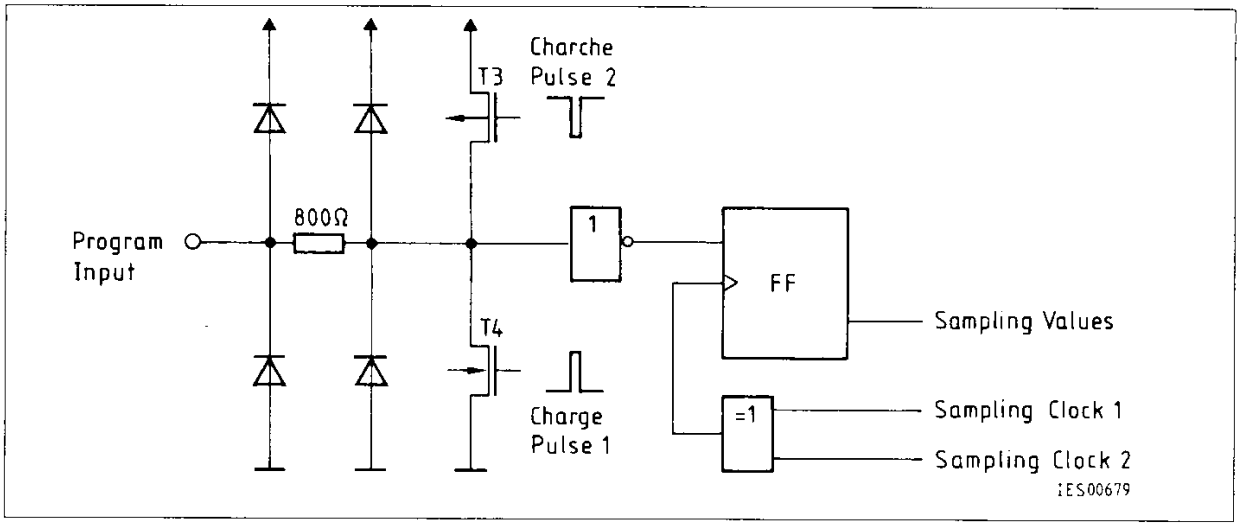

Figure 9

Schematic Circuit Diagram at Programming Input (Pin 2)

Functional Description of Pin 2 (Programming Input)

The SLB 0586 A provides the possibility of differentiating between types A, B, and C by appropriate connection of pin 2.

Depending on the charge pulses shown in **figure 9** transistors T3 and T4 alternate in becoming conductive. The currents flowing during the conductive phase of the transistors are sufficient for a charge reversal of the load capacitance of 7 pF max. present at pin 2.

It is important that no major discharge of the capacitance present at pin 2 occurs from the time of charge reversal until the sampling of the voltage level by the two sampling clocks.

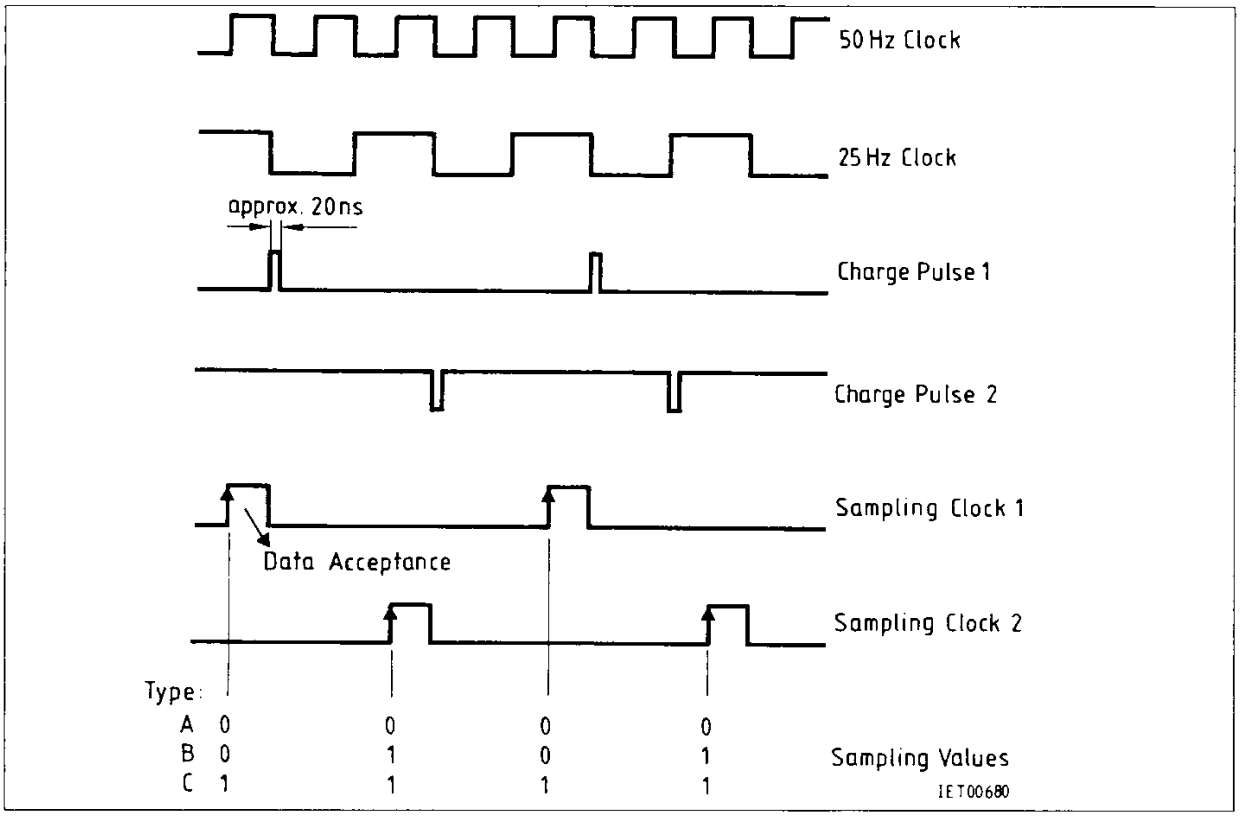

Figure 10

Internal Timing for Differentiating between the three Possible Modes A, B, and C

Absolute Maximum Ratings

V_{DD} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{SS}	– 7.5	0.3	V
Input voltage	V_I	V_{SS} – 0.3	0.3	V
Input current	I_I	– 0.5	0.5	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 55	125	°C
Total power dissipation (T_A = 25 °C)			10	mW

Thermal Resistance

System-air P-DIP-8	$R_{th\ SA}$		135	K/W
System-air P-DSO-8	$R_{th\ SA}$		231	K/W

Operating Range

Supply voltage	V_{SS}	– 5.6	– 4.5	V
Line frequency	f	47.5	63	Hz
Ambient temperature	T_A	0	80	°C

Characteristics

T_A = 25 °C; V_{SS} = – 5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current (Pin 1)	I_{DD}			0.45	mA	f_{sync} = 50 Hz
Sensor Input (pin 5)						
H-input voltage	V_{IH}	1/2 V_{SS}+1.1			V	
L-input voltage	V_{IL}			1/2 V_{SS}-1.1	V	
Input current	I_{IH}		33	37	µA	220 V at sensor input and series resistor
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}		line sine wave			
Frequency with active signal	f		50/60		Hz	synchronized with 50/60 Hz clock at sync input

Characteristics (cont'd)
T_A = 25 °C; V_{SS} = – 5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Extensions (pin 6)						
H-input voltage	V_{IH}	1/2 V_{SS}+1.1			V	
L-input voltage	V_{IL}			1/2 V_{SS}-1.1	V	
Input current	I_{IH} I_{IL}	– 1 0		0 1	µA µA	V_I = 0 V V_I = V_{SS}
Sync Input (pin 4)						
H-input voltage L-input voltage Input current	V_{IH} V_{IL} I_{IH}	1/2 V_{SS}+1.8	 207	 1/2 V_{SS}-1.8	V V µA	with series resistor 1.5 MΩ from 220 V line*)
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}		supply sine wave			
Frequency	f		50/60		Hz	
Programming Input (pin 2)						
Load capacitance through board with tristate	C_L			7	pF	
Integrator (pin 3)						
Application circuit	C_5 R_{10}	68 22	100 100	330 680	nF kΩ	
Output (pin 8)						
L-output current	I_Q	25			mA	V_{QL} = – 3 V
L-pulse width	t_{QL}			39.0 32.6	µs µs	50 Hz supply 60 Hz supply
HL transition time	t_{HLQ}			5	µs	
LH transition time	t_{LHQ}			5	µs	

*) see Application Circuit

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