Data Sheet July 1999 File Number 4617.1

## Radiation Hardened Octal Transparent Latch, Three-State

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCS373T is a Radiation Hardened Octal Transparent Three-State Latch with an active-low output enable. The HCS373T utilizes advanced CMOS/SOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

## Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the HCS373T are contained in SMD 5962-95792.** A "hot-link" is provided from our website for downloading**.**
**www.intersil.com/spacedefense/newsafclasst.asp**

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
**www.intersil.com/quality/manuals.asp**

## Ordering Information

| ORDERING NUMBER | PART NUMBER | TEMP. RANGE ($^oC$) |
|---|---|---|
| 5962R9579201TRC | HCS373DTR | -55 to 125 |
| 5962R9579201TXC | HCS373KTR | -55 to 125 |

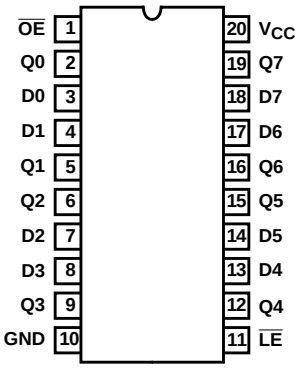
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

## Features

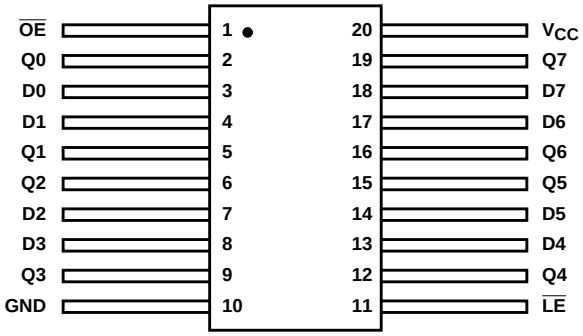
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ($\gamma$) 1 x $10^5$ RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets: >100 MEV-$cm^2$/mg
  - Single Event Upset (SEU) Immunity < 2 x $10^{-9}$ Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened CMOS SOS
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - $V_{IL}$ = 0.3 $V_{CC}$ Max
  - $V_{IH}$ = 0.7 $V_{CC}$ Min
- Input Current Levels Ii ≤ 5mA at $V_{OL}$, $V_{OH}$

## Pinouts

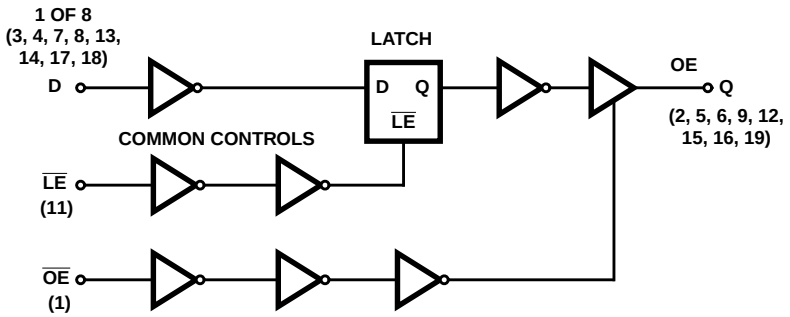
**HCS373DTR (SBDIP), CDIP2-T20**
TOP VIEW




**HCS373KTR (FLATPACK), CDFP4-F20**
TOP VIEW



## Functional Diagram




**TRUTH TABLE**

| $\overline{OE}$ | $\overline{LE}$ | D | Q |
|---|---|---|---|
| L | H | H | H |
| L | H | L | L |
| L | L | I | L |
| L | L | h | H |
| H | X | X | Z |

H = High Level, L = Low Level.

X = Immaterial, Z = High Impedance.

I = Low voltage level prior to the high-to-low latch enable transition.

h = High voltage level prior to the high-to-low latch enable transition.

## Die Characteristics

**DIE DIMENSIONS:**

(2747µm x 2693µm x 533µm ±51.0µm)

108 x 106 x 21mils ±2mil

**METALLIZATION:**

Type: Al Si

Thickness: 11kÅ ±1kÅ

**SUBSTRATE POTENTIAL:**

Unbiased Silicon on Sapphire

**BACKSIDE FINISH:**

Sapphire

**PASSIVATION:**

Type: Silox ($S_iO_2$)

Thickness: 13kÅ ±2.6kÅ

**WORST CASE CURRENT DENSITY:**

< 2.0e5 A/cm$^2$

**TRANSISTOR COUNT:**

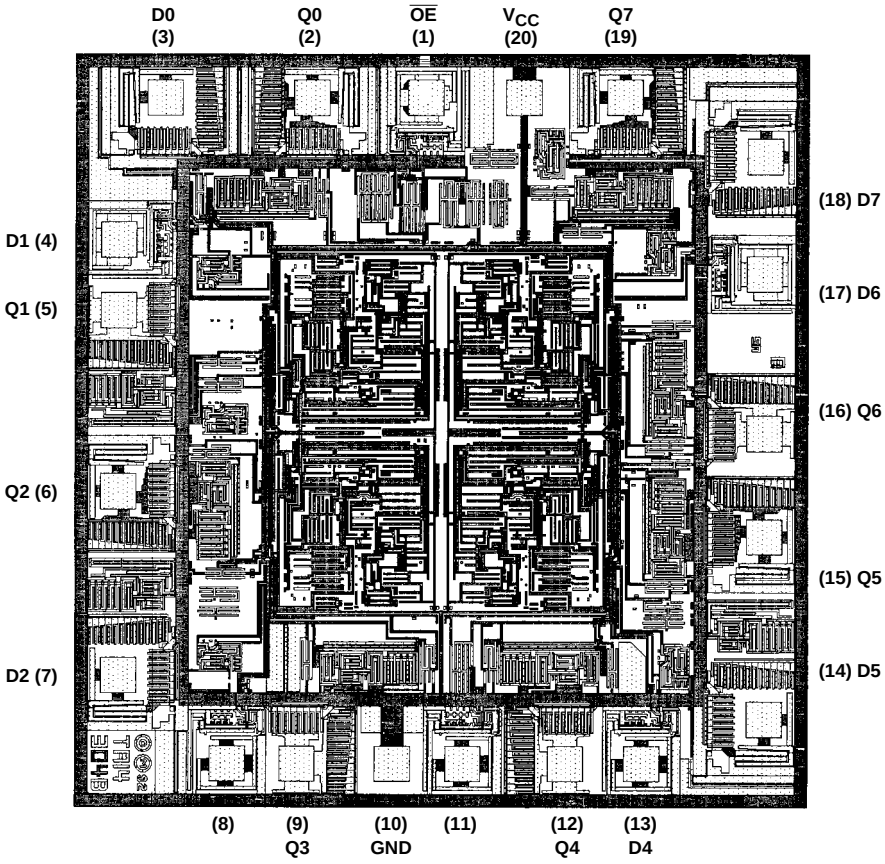
376

**PROCESS:**

CMOS SOS

## Metallization Mask Layout

**HCS373T**




NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCS373 is TA14303A.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.